A 150-nA 13.4-ppm/℃ switched-capacitor CMOS sub-bandgap voltage reference*

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Abstract: A nanopower switched-capacitor CMOS sub-bandgap voltage reference has been implemented using a Chartered 0.35-μm 3.3-V/5-V dual gate mixed-signal CMOS process. The proposed circuit generates a precise sub-bandgap voltage of 1 V. The temperature coefficient of the output voltage is 13.4 ppm/℃ with the temperature varying from –20 to 80 ℃. The proposed circuit operates properly with the supply voltage down to 1.3 V, and consumes 150 nA at room temperature. The line regulation is 0.27%/V. The power supply rejection ratio at 100 Hz and 1 MHz is –39 dB and –51 dB, respectively. The chip area is 0.2 mm^2.

Key words: nanopower; sub-bandgap; switched-capacitor; voltage reference

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1. Introduction

The voltage reference is an important building block in all mixed-signal systems to provide a stable DC voltage that is insensitive to the variations of supply voltage and temperature. In conventional CMOS integrated systems, vertical-BJT-based bandgap references[1, 2] are widely used to generate a precise voltage around 1.25 V. However, with the rapidly increasing scale of modern integrated mixed-signal systems, the demand for each building block operating with low voltage and low power is growing to reduce the system power. As a result, the low-power sub-bandgap voltage reference has been attracting more and more attention in recent years[3–5]. Unfortunately, all of these solutions utilize resistors, which greatly limit their application in ultra-low-power designs. For example, for a voltage difference of 1 V, the resistance would be as large as 100 MΩ to achieve a tiny current of 10 nA, which increases the silicon area to an unacceptable level. Consequently, various nanopower threshold-voltage-based CMOS voltage references have been proposed[6–8]. These solutions successfully avoid the use of resistors, thus greatly reducing the power consumption. However, their output voltages suffer from the variations of process parameters, especially the threshold voltage. Therefore, the yield cannot be high without a trimming procedure. To solve this problem, a switched-capacitor voltage reference is proposed to accomplish the trimming by adjusting the capacitors[9]. However, the current generator exploited in Ref. [9] is based on the large difference in threshold voltage between 5-V and 3.3-V NMOS devices, which is not valid in all standard CMOS technologies. Moreover, the square-wave output voltage is not suitable for most mixed-signal applications.

In this paper, a novel resistorless switched-capacitor CMOS voltage reference is presented. With the proposed structure, a precise sub-bandgap voltage of 1 V is generated. Based on the different temperature characteristics of NMOS devices with different gate oxide thicknesses, well temperature compensation is achieved. Moreover, the output voltage can easily be trimmed without affecting the temperature coefficient. This paper also gives a simple review of the recently reported switched-capacitor voltage reference and describes the detailed operation principle and implementation of the proposed circuit.

2. Recently reported switched-capacitor voltage reference

Figure 1 shows the structure of the switched-capacitor voltage reference proposed by Huang *et al.*[9]. The detailed operation principle has been described in Ref. [9], and only the conclusion is given here for reference. The output voltage of

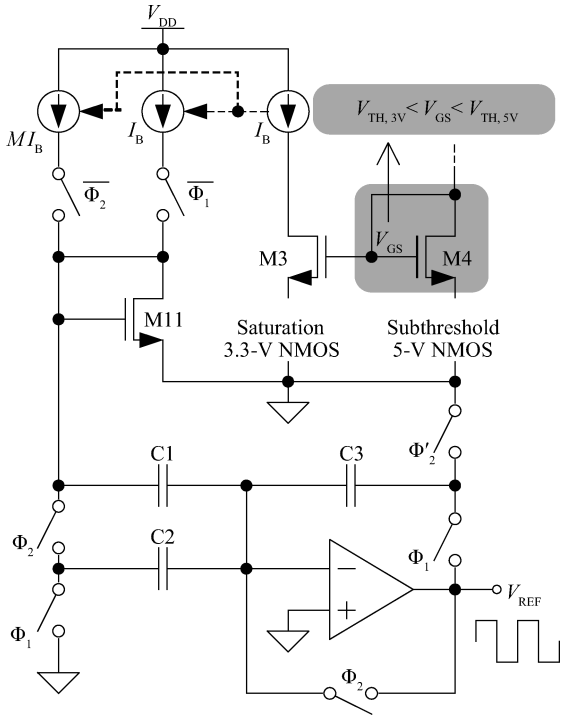

Fig. 1. Recently reported switched-capacitor voltage reference[9].

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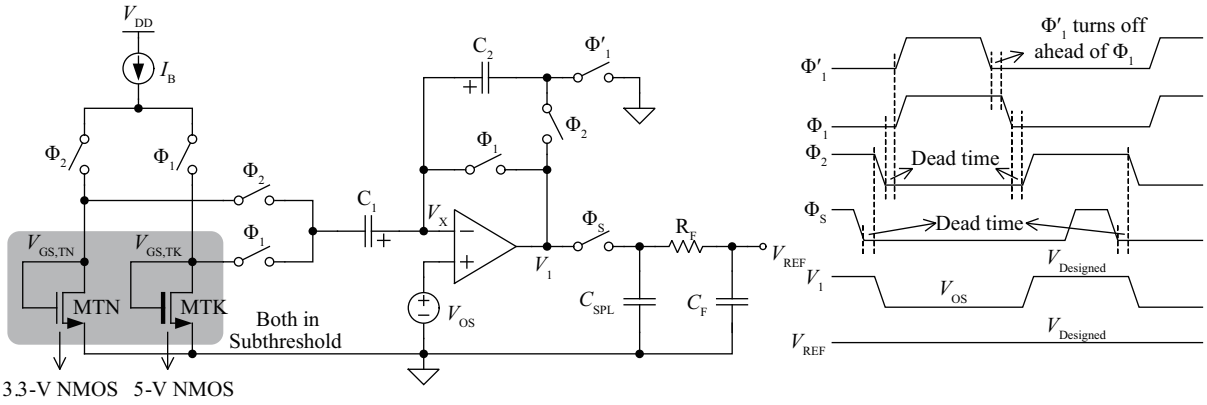

Fig. 2. Structure and timing diagram of the proposed switched-capacitor voltage reference.

the circuit can be expressed as

$$V_{\mathrm{REF}} = \frac{C_2}{C_3} V_{\mathrm{TH,3V}} + \left[\frac{C_1(\sqrt{M}-1) + C_2\sqrt{M}}{C_3(N-1)} \right] m V_{\mathrm{T}} A, \quad (1)$$

where A is the parameter to be designed, and all other parameters have the same definitions as stated in Ref. [9]. By properly choosing C_1 and C_2, temperature compensation can be well achieved. It can also be seen that the output voltage can be trimmed by adjusting these capacitors. There are two problems with this circuit. Firstly, as shown in Fig. 1, the current generator exploited[6] makes M3 operate in the saturation region and M4 in the subthreshold region. This is based on the large difference in threshold voltage between 5-V (M4) and 3.3-V (M3) NMOS devices (0.7 V and 0.498 V, respectively), which is not always applicable in all standard CMOS technologies (0.658 V and 0.605 V, respectively, in this design). Secondly, the desired output voltage is applicable in only one clock phase. That is to say, the output voltage is a square-wave, which is not suitable for most mixed-signal applications.

3. Proposed switched-capacitor voltage reference

The principle of the proposed switched-capacitor voltage reference is based on our observation that the threshold voltages of NMOSFETs with different gate oxide thicknesses in the same CMOS technology exhibit different temperature characteristics[8]. However, the circuit presented in Ref. [8] is susceptible to the variation in threshold voltage, and the output voltage cannot be trimmed. To solve this problem, a novel switched-capacitor voltage reference structure is proposed, as shown in Fig. 2. The circuit consists of a nanoampere bias current (I_B), a 3.3-V thin-gate-oxide NMOSFET (MTN) and a 5-V thick-gate-oxide NMOSFET (MTK) operating in the subthreshold region, an offset-insensitive switched-capacitor difference amplifier, a sampler, and a post-filter. In order to avoid undesired charge leakage, non-overlapping clocks are applied, which can be provided by a standard non-overlapping clock generator[10]. The output voltage can easily be designed to any value by properly choosing the ratio of C_1 with respect to C_2. The detailed operation principle of this circuit is explained below.

3.1. Operation principle

During the Φ_1 phase, the nanoampere bias current I_B flows through the subthreshold-operated MTK, and a gate-source voltage $V_{GS,TK}$ is generated. The buffer-connected amplifier forces V_X to follow V_{OS}, so $V_{GS,TK}$ and V_{OS} are sampled by C_1 and C_2, respectively. Therefore the total charge stored on positive plates of C_1 and C_2 can be written as

$$Q_{\mathrm{Total},\Phi_1} = (V_{\mathrm{OS}} - V_{\mathrm{GS,TK}})C_1 + V_{\mathrm{OS}}C_2. \quad (2)$$

During the Φ_2 phase, the same I_B flows through the subthreshold operated MTN, and another gate-source voltage $V_{GS,TN}$ is generated. The amplifier is now connected as a proportional amplifier. Due to the negative feedback, V_X still equals V_{OS}. The total charge stored on the positive plates of C_1 and C_2 can be written again as

$$Q_{\mathrm{Total},\Phi_2} = (V_{\mathrm{OS}} - V_{\mathrm{GS,TN}})C_1 + (V_{\mathrm{OS}} - V_1)C_2. \quad (3)$$

Since no available path for charge escaping from node V_X exists in the Φ_2 phase, it can be concluded that $Q_{\mathrm{Total},\Phi_1} = Q_{\mathrm{Total},\Phi_2}$. By combining Eqs. (2) and (3), and substituting the subthreshold I–V expression of MOSFET[11], the output voltage after sampling can be expressed as

$$V_{\mathrm{REF}} = \frac{C_1}{C_2}\left(V_{\mathrm{TH,TK}} - V_{\mathrm{TH,TN}} + V_{\mathrm{T}} \ln \frac{t_{\mathrm{ox,TK}} S_{\mathrm{TN}}}{t_{\mathrm{ox,TN}} S_{\mathrm{TK}}} \right), \quad (4)$$

where V_T is the thermal voltage, t_{ox} is the gate oxide thickness of the MOSFET, and S_{TK} (S_{TN}) is the aspect ratio of MTK (MTN). In order to improve the power supply rejection ratio (PSRR) performance at high frequency, a post-filter is applied after the sampler. It can be seen that V_{REF} can easily be set or trimmed to any value by properly adjusting the ratio of C_1 with respect to C_2, which greatly increases the application range and yield of the proposed circuit.

3.2. Temperature compensation

By substituting the expression of V_{TH}[11] into Eq. (4), and differentiating the result with respect to temperature, the temperature dependence of V_{REF} can be found as

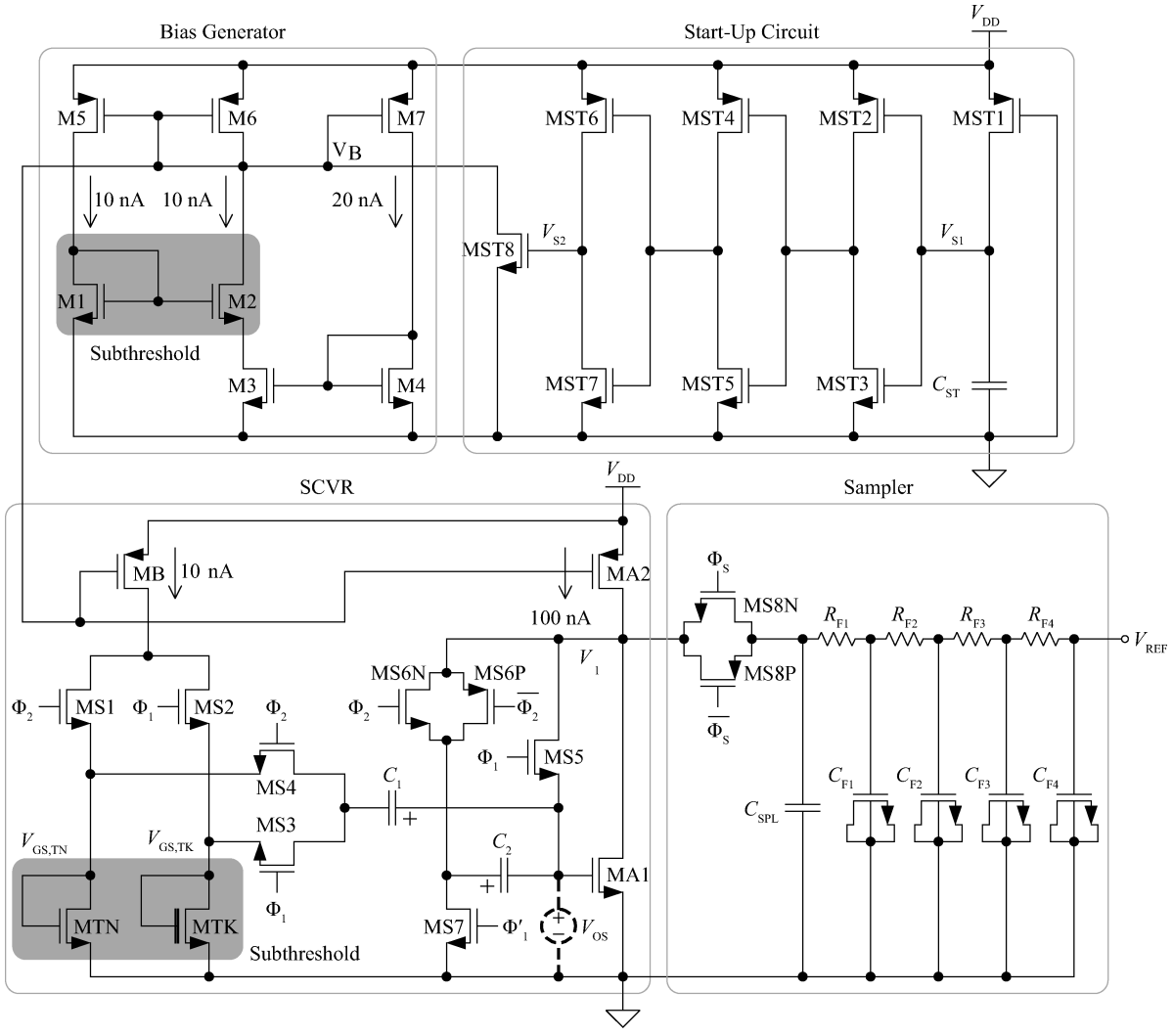

Fig. 3. Transistor level implementation of the proposed circuit.

$$\left.\frac{\mathrm{d}V_{\mathrm{REF}}/\mathrm{d}T}{V_{\mathrm{REF}}}\right|_{T_0} = \frac{1}{\left.(V_{\mathrm{TH,TK}}-V_{\mathrm{TH,TN}})\right|_{T_0} + V_{T_0}\ln\dfrac{t_{\mathrm{ox,TK}}S_{\mathrm{TN}}}{t_{\mathrm{ox,TN}}S_{\mathrm{TK}}}} \times\left[\frac{nk}{q}\ln\frac{t_{\mathrm{ox,TK}}S_{\mathrm{TN}}}{t_{\mathrm{ox,TN}}S_{\mathrm{TK}}} + \sqrt{\frac{2N_A\varepsilon_{\mathrm{si}}q^2}{E_{\mathrm{g}}+2kT_0\ln(N_{\mathrm{A}}/\sqrt{N_{\mathrm{c}}N_{\mathrm{v}}})}} \times\frac{k(t_{\mathrm{ox,TK}}-t_{\mathrm{ox,TN}})}{q\varepsilon_{\mathrm{ox}}}\ln\frac{N_{\mathrm{A}}}{\sqrt{N_{\mathrm{c}}N_{\mathrm{v}}}}\right], \tag{5}$$

where T_0 is the temperature concerned, and all other physical parameters have the same meanings as defined in Ref. [11]. Equating (5) to zero, temperature compensation can be achieved by optimizing $S_{\mathrm{TN}}/S_{\mathrm{TK}}$ as

$$\frac{S_{\mathrm{TN}}}{S_{\mathrm{TK}}} = \frac{t_{\mathrm{ox,TN}}}{t_{\mathrm{ox,TK}}} \times\exp\left(\sqrt{\frac{2N_{\mathrm{A}}\varepsilon_{\mathrm{si}}q^2}{E_{\mathrm{g}}+2kT_0\ln(N_{\mathrm{A}}/\sqrt{N_{\mathrm{c}}N_{\mathrm{v}}})}} \times\frac{t_{\mathrm{ox,TK}}-t_{\mathrm{ox,TN}}}{n\varepsilon_{\mathrm{ox}}}\ln\frac{\sqrt{N_{\mathrm{c}}N_{\mathrm{v}}}}{N_{\mathrm{A}}}\right). \tag{6}$$

As can be seen from Eq. (6), the temperature compensation of V_{REF} is independent of C_1 and C_2. That is to say, no matter what value V_{REF} is designed or trimmed to be, the temperature coefficient will not be influenced at all.

3.3. Circuit implementation

The transistor level realization of the proposed circuit is shown in Fig. 3, where MTK and MTN are 5-V and 3.3-V NMOSFETs, respectively. As shown in Eq. (4), V_{REF} is independent of I_{B}. Consequently, no accurate current generator is required. Thanks to the subthreshold operation of MTK and MTN, only a tiny bias current of 10 nA is sufficient. Therefore, a classical pseudo-constant nanoampere current generator

without resistors is adopted[12], which does not require a large difference in threshold voltage between MTK and MTN. As a result, the proposed circuit is applicable in all standard CMOS technologies. An input clock signal of 1 kHz is applied. Thanks to the low frequency operation, the simulated current draw of the non-overlapping clock generator is only 4 nA. In order to avoid the undesired stable state during power on, a low-power start-up circuit is applied. When the supply voltage steps from zero to V_{DD}, the voltage at the top plate of $C_{ST}(V_{S1})$ is slowly charged up. This ramp signal is shaped by three inverters to generate a narrow pulse signal at V_{S2}, so MST8 is turned on to start the whole circuit. After V_{S1} reaches V_{DD}, V_{S2} is set to zero again to turn off MST8, and no quiescent current is consumed.

The design of the amplifier is not critical here since the offset voltage can be canceled out by the switched-capacitor circuit, as illustrated in Eqs. (2) and (3). Thus a simple common-source amplifier composed of MA1 and MA2 is adopted. It is important, however, to ensure that he gain bandwidth product (GBW) of the amplifier is large enough to reduce the settling error. As a result, a larger bias current of 100 nA is applied. Moreover, the DC gain of the amplifier should be so high that the steady state error will not deteriorate the accuracy of V_{REF}. This is achieved by choosing a large channel length (100 μm) of MA1 and MA2. Simulation results show that the amplifier has a DC gain of 71 dB and a GBW of 170 kHz with a phase margin of 72°, which is sufficient for the 1 kHz switched-capacitor circuit.

As shown in Eq. (4), V_{REF} is determined by the ratio of C_1 with respect to C_2. In modern CMOS technologies, the relative accuracy between capacitors is much higher than their absolute accuracy. Therefore, both C_1 and C_2 consist of an integral number of the same unit cell (5 μm × 5 μm inter-poly capacitor) in this design. For the same consideration, MTK and MTN are also made up of cells with the same dimension (10 μm/4 μm) to improve the stability of the temperature coefficient, as shown in Eq. (6). Though MTK and MTN have different gate oxide thicknesses, this choice still improves their matching property to some extent. In order to guarantee the classic long-channel I–V characteristic of MOSFET, a minimal dimension of 4 μm is chosen for the MOSFET[13]. As a result, the short-channel effects can be ignored.

The accuracy requirement of capacitors and resistors in the post-filter is not strict. In order to save the silicon area, high-resistance ploy resistors with narrow-width and MOS capacitors are applied. It should be pointed that the first-order low-pass filter in Fig. 2 is replaced by a fourth-order counterpart to further suppress the high-frequency noise. In this design, the –3 dB bandwidth of the post-filter is set to be 10 kHz, beyond which the PSRR of V_{REF} will decrease rapidly. The parameters of components in this design are listed in Table 1.

Table 1. Parameters of components in the proposed circuit.

Component	$W/L(\mu m)$	Component	$W/L(\mu m)$
M1	(4 × 10)/4	MTK	(5 × 10)/4
M2	(40 × 10)/4	MA1	2/(10 × 10)
M3	4/(10 × 60)	MA2	4/(10 × 10)
M4	4/(10×100)	C_1	5/5, m = 100
M5–M6	4/(10 × 100)	C_2	5/5, m = 18
M7	(2 × 4)/(10 × 100)	C_{SPL}	5/5, m = 20
MB	4/(10 × 100)	C_{F1-4}	5/5, m = 34
MTN	(69 × 10)/4	R_{F1-4}	1.5/(10 × 80)

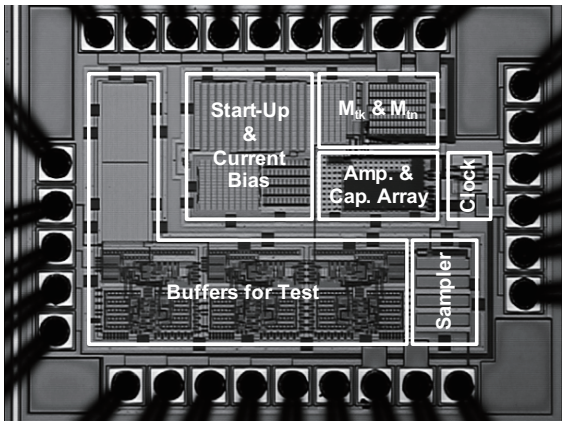

Fig. 4. Die photograph of the proposed circuit.

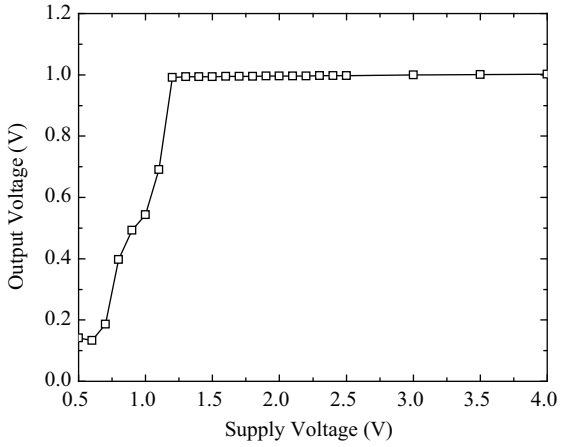

Fig. 5. Measured line regulation of output voltage.

4. Experimental results

The proposed circuit has been fabricated using a Chartered 0.35-μm 3.3-V/5-V dual gate mixed-signal CMOS process ($V_{THN,TK}$ = 0.658 V, $V_{THN,TN}$ = 0.605 V, and $|V_{THP,TN}|$ = 0.837 V, respectively, at 0 ℃). The die photograph is shown in Fig. 4, where three buffers are used for testing. The occupied silicon area without buffers and pads is 0.2 mm^2. This area is mainly restricted by the minimal dimension of MOSFETs, which is set to be 4 μm in this design. Nevertheless, the area is still much smaller than that of the resistor-based voltage reference under the same order of power consumption. As illustrated before, for a 1-V voltage difference, a 100-MΩ resistor is needed to achieve a 10-nA current. In this technology, even the area of one 100-MΩ resistor would be as large as 0.4 mm^2 with a minimal width of 2 μm. For a more accurate resistor, a larger minimal width should be chosen and the area will further increase.

The measured output voltage as a function of supply voltage is shown in Fig. 5. It can be seen that a stable output voltage of 1 V is generated with the supply voltage down to 1.3 V. This minimal supply voltage is mainly restricted by the current generator due to the high threshold voltages in this design. With

Table 2. Performance comparison between this work and Ref. [9].

Parameter	This work	ISSCC 08[9]
Technology	0.35 μm CMOS	0.35 μm CMOS
Supply voltage (V)	1.3–4	1–4
Output voltage (mV)	1000	190.1
Supply current (nA)	142 @ 1.3 V	250 @ 1 V
	157 @ 4 V	560 @ 4 V
Temperature coefficient (ppm/℃)	13.4	16.9
Temperature range (℃)	−20 to 80	−40 to 80
Line regulation (%/V)	0.27	0.76
PSRR (dB)	−39 @ 100 Hz	−41 @ 100 Hz
	−51 @ 1 MHz	−18 @ 1 MHz

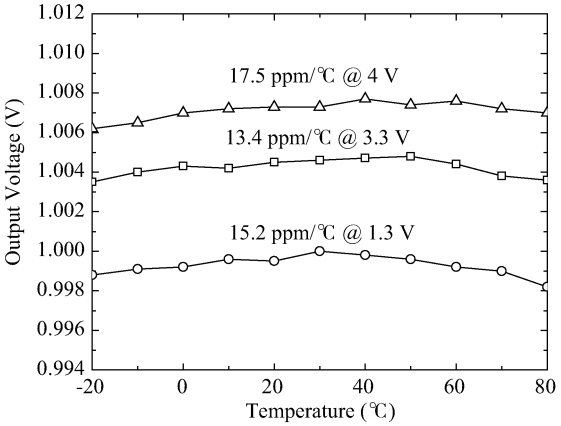

Fig. 6. Measured temperature coefficient of output voltage under different supply voltages.

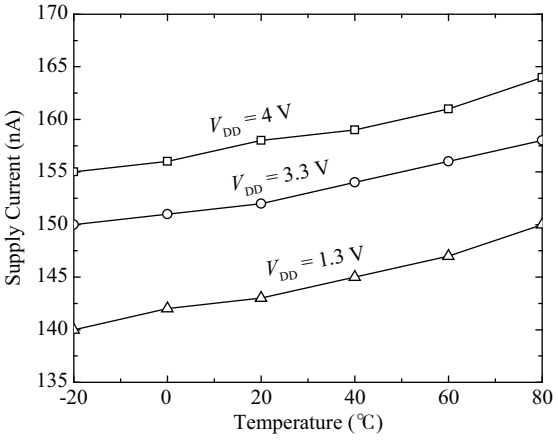

Fig. 7. Measured supply current variation with temperature under different supply voltages.

the supply voltage varying from 1.3 to 4 V, the maximal deviation of output voltage is 7.3 mV at room temperature, which corresponds to a line regulation of 0.27%/V. Figure 6 shows the measured temperature coefficient of the output voltage under three different supply voltages. With the temperature varying from –20 to 80 ℃, the minimal achieved temperature coefficient is 13.4 ppm/℃. The variation in supply current with temperature under different supply voltages is also given in Fig. 7. Thanks to the subthreshold operation of MTK and MTN, nanoampere design is achieved. It can be seen from Fig. 7 that the average current draw at room temperature is only 150 nA.

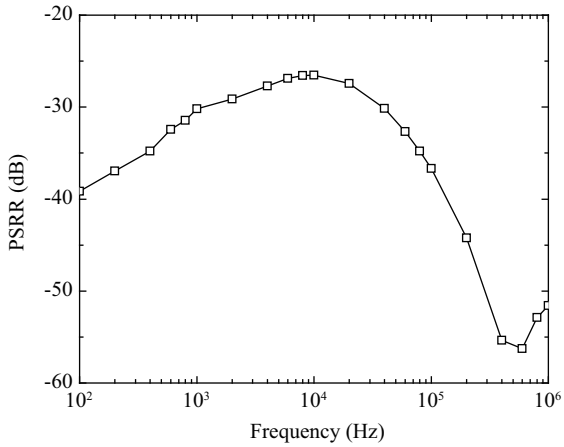

Fig. 8. Measured power supply rejection ratio of output voltage.

The measured PSRR result is shown in Fig. 8. Thanks to the low-pass filter after the sampler, the PSRR begins to decrease at 10 kHz. The measured PSRR at 100 Hz and 1 MHz is –39 and –51 dB, respectively.

As illustrated before, a threshold-voltage-based voltage reference is sensitive to the variations in process parameters, especially the threshold voltage which possibly varies by more than 10% in modern CMOS technologies. Consequently, a low yield occurs without a trimming procedure. In this design, ten chips were tested. The maximum deviation in output voltage is 25 mV (2.5%) under a 3.3 V power supply at room temperature. This problem can be easily solved by trimming the value of C_1 or C_2 during manufacture, as shown in Eq. (4). As a result, the yield will not be a problem any more. The performance comparison between this work and the previous design in Fig. 1[9] is given in Table 2. It can be seen that the proposed circuit achieves perfect temperature compensation and consumes extremely low power. Compared with Ref. [9], the large bias current of MIB is reduced to I_B due to the proposed structure. As a result, the supply current is greatly reduced. Thanks to the post-filter, the PSRR performance is greatly improved at high frequency.

5. Conclusion

A nanopower switched-capacitor CMOS sub-bandgap voltage reference is presented. A precise output voltage of 1 V is generated with the supply voltage down to 1.3 V, and the current draw is 150 nA. The temperature coefficient of

output voltage is 13.4 ppm/℃ with the temperature varying from –20 to 80 ℃. The line regulation is 0.27%V. The power supply rejection ratio at 100 Hz and 1 MHz is –39 dB and –51 dB, respectively. The circuit has been fabricated with a Chartered 0.35-μm 3.3-V/5-V dual gate mixed-signal CMOS process. The chip area is 0.2 mm^2.

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