Fabrication and characterization of high performance AlGaN/GaN HEMTs on sapphire with silicon nitride passivation

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Abstract: AlGaN/GaN high electron mobility transistors (HEMTs) with high performance were fabricated and characterized. A variety of techniques were used to improve device performance, such as AlN interlayer, silicon nitride passivation, high aspect ratio T-shaped gate, low resistance ohmic contact and short drain–source distance. DC and RF performances of as-fabricated HEMTs were characterized by utilizing a semiconductor characterization system and a vector network analyzer, respectively. As-fabricated devices exhibited a maximum drain current density of 1.41 A/mm and a maximum peak extrinsic transconductance of 317 mS/mm. The obtained current density is larger than those reported in the literature to date, implemented with a domestic wafer and processes. Furthermore, a unity current gain cut-off frequency of 74.3 GHz and a maximum oscillation frequency of 112.4 GHz were obtained on a device with an 80 nm gate length.

Key words: GaN; HEMT; T-gate; AlN interlayer; SiN passivation; current density
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1. Introduction

In recent years, wide-band-gap gallium nitride (GaN) has attracted many researchers' interest, owing to its high breakdown fields (3.3×10^6 V/cm), high sheet charge density (larger than 1×10^{13} cm^{-2}), high peak electron velocities (3×10^7 cm/s) and electron saturation velocities (1.5×10^7 cm/s). All of these make GaN-based high electron mobility transistors (HEMTs) potential candidates for high-power and high-frequency applications.

However, there are several barriers to progress in the fabrication of high performance AlGaN/GaN HEMT devices, such as parasitic resistance and capacitance, the quality of ohmic contact, surface states and the current collapse effect. Many efforts have been made to alleviate these issues, but none of them alone could lead to the optimal performance of the device, therefore a combination of them is needed. In this work, we present the fabrication and characterization of high performance AlGaN/GaN HEMTs on sapphire substrate. A variety of techniques, comprising an AlN interlayer, silicon nitride (SiN) passivation, high aspect ratio T-shaped gate, low resistance ohmic contact and short drain–source distance, are integrated to improve device DC and RF performance. Devices that we fabricated exhibit a maximum drain current density of 1.41 A/mm and a maximum peak extrinsic transconductance of 317 mS/mm. In addition, a unity current gain cut-off frequency (f_T) of 74.3 GHz and a maximum oscillation frequency (f_{MAX}) of 112.4 GHz are obtained on an 80 nm gate length device. As far as we know, 2.1 A/mm maximum drain current density[1] and 160 GHz unity current gain cut off frequency[2] in AlGaN/GaN HEMTs on sapphire have been reported abroad, and the best domestic results are 1.07 A/mm[3] and 77 GHz[4], respectively. The current density that we obtained is larger than the best domestic result and the f_T is close to it.

2. Device fabrication

AlGaN/GaN heterostructures were grown by metal organic chemical vapor deposition (MOCVD) on a 2-inch sapphire substrate. The active layers of our device consist of a 25 nm undoped AlGaN layer, a 1 nm AlN layer and a 3.5 μm undoped GaN layer. Figure 1 shows a schematic diagram of

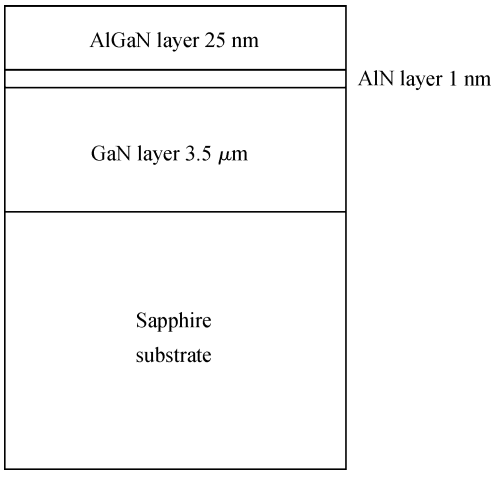

Fig. 1. A schematic material structure of AlGaN/GaN HEMTs on a sapphire substrate.

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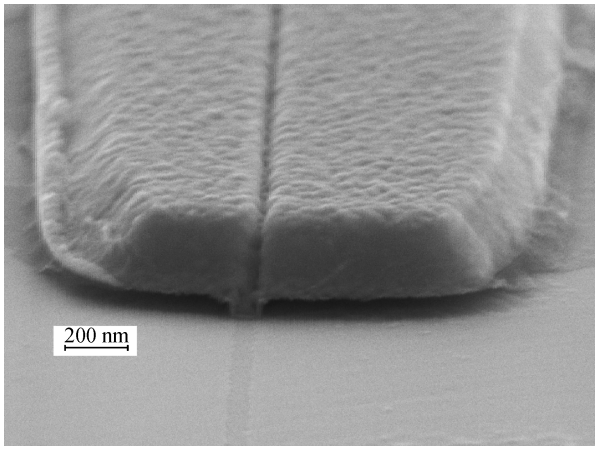

Fig. 2. SEM image of a T-shaped gate with an 80 nm gate length.

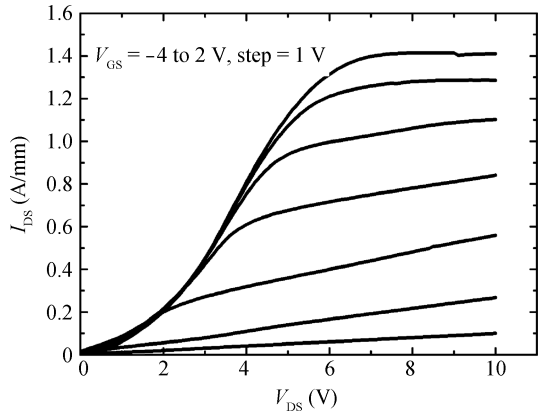

Fig. 3. I–V characteristics of an AlGaN/GaN HEMT device with an 80 nm gate length.

the material structure.

The fabrication of the device began with mesa isolation, which was realized by inductively coupled plasma reactive ion etching (ICP-RIE) in a Cl_2/Ar-based plasma atmosphere. The ohmic contacts were formed by e-beam evaporation of Ti/Al/Ni/Au (30/90/50/20 nm) onto drain–source areas, followed by annealing at 835 ℃ for 35 s in a N_2 ambient. A source–drain spacing L_{SD} of 2.5 μm was used to reduce the source and drain resistance. The specific contact resistance was evaluated to be 4.8×10^{-5} Ω·cm^2 by using the transmission line model (TLM) method. Subsequently, a 50-nm-thick layer of silicon nitride, deposited by plasma enhanced chemical vapor deposition (PECVD), was used for surface passivation. Two-step e-beam lithography was adopted for the definition of the gate. The first exposure defined the foot of the gate on resist, which was subsequently transferred to the silicon nitride layer by dry etch, and the second exposure defined the head of the gate. Eventually, a Ni/Au (20/200 nm) gate with 80 nm length was formed by e-beam evaporation and a lift-off process. To reduce gate resistance and gate capacitance, the length of the gate's head and the aspect ratio of the T-shaped gate were designed to be 1 μm and 10, respectively. Figure 2 shows a SEM image of a T-shaped gate with an 80 nm gate length fabricated with this method.

3. Results and discussion

DC characteristics were measured by using a Keithley 4200-SCS/F semiconductor characterization system. Figure 3 shows the drain–source I–V characteristics of a device with a 10 μm gate width. The maximum drain current density was 1.41 A/mm at $V_{GS} = 2$ V. Figure 4 shows the transfer characteristic at $V_{DS} = 7$ V. The maximum extrinsic transconductance was 317 mS/mm. To the best of our knowledge, this is the largest drain–source current device so far implemented with a domestic wafer and processes. To maximize the saturated drain current density, the resistivity of the device channel needs to be minimized. This means that the sheet carrier concentration and electron mobility in the channel must be maximized. The thin AlN interlayer used here produces a large effective ΔE_C between AlGaN and GaN at both sides of AlN, which increased the electron mobility and the two dimensional electron gas (2DEG) concentration[5]. This structure offers a 2DEG with a total charge density of 1.08×10^{13} cm^{-2} and an electron mobility of 1941 cm^2/(V·s), both of which are measured on unpassivated samples by using the van der Pauw method at room temperature. The corresponding 2DEG sheet resistance was 297 Ω/□. The SiN passivation layer, which compensates surface states and defects and prevents them from trapping carriers, further increases the electron concentration in 2DEG[6]. The drain current density obtained now is about 43.9% higher than the result that we obtained before[7]. Therefore, we consider that this improvement is mainly attributed to the introduction of the AlN interlayer and the SiN passivation layer, which results in a higher electrical conductivity channel. Meanwhile, due to the low aspect ratio between the gate length and the AlGaN barrier layer, the pinch-off characteristic of the device was not satisfying, which was categorized to short-channel effect. As part of our ongoing work, we are currently developing gate-recess technology to suppress the short-channel effect so as to improve the pinch-off characteristic.

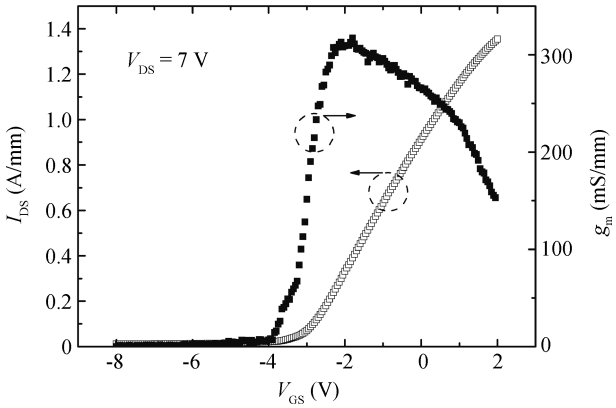

Fig. 4. Transfer characteristics of an AlGaN/GaN HEMT with an 80 nm gate length.

On-wafer small-signal RF performances of devices were characterized with an HP8720D vector network analyzer, which swept from 0.05 to 20 GHz in 0.05 GHz steps. The current gain $|h_{21}|$ and the maximum stable gain/maximum available gain (MSG/MAG) of devices were derived from measured S-parameters as a function of frequency. The small signal char-

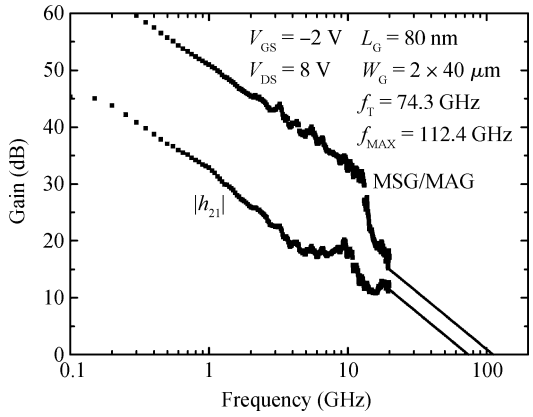

Fig. 5. Small signal characteristics of an AlGaN/GaN HEMT device with an 80 nm gate length and a 2 × 40 μm gate width.

acteristic of the device with an 80 nm gate length and 2 × 40 μm gate width is shown in Fig. 5. A cut-off frequency f_T of 74.3 GHz was obtained by extrapolating $|h_{21}|$ with a slope of –20 dB/decade at $V_{GS} = -2$ V and $V_{DS} = 8$ V. Similarly, a maximum oscillation frequency f_{MAX} of 112.4 GHz was obtained by extrapolating MSG/MAG with a slope of –20 dB/decade. These results are slightly better than our previous results[7], where the gate length was 180 nm. Obviously, the RF performance of our device is limited by other factors. The f_T is mainly affected by gate length, source and drain parasitic resistance, gate–drain parasitic capacitance, etc. The expression for the relationship between f_{MAX} and f_T is

$$f_{MAX}/f_T = \sqrt{R_{ds}/(R_g + R_{ch})}\Big/2, \quad (1)$$

where R_{ds} is the output resistance, R_g is the gate resistance, and R_{ch} is the channel resistance. On the one hand, in order to improve f_T, the high aspect-ratio T-shaped gate was used to minimize the gate length to 80 nm, and low resistance ohmic contact and short drain–source distance were used to lower the source and drain parasitic resistance. Meanwhile, R_g was lowered by using a high aspect-ratio T-shaped gate, and R_{ch} was lowered by introducing an AlN interlayer and a SiN passivation layer. A higher f_{MAX} was expected. On the other hand, the SiN passivation layer greatly increases parasitic capacitance, which could significantly reduce the high frequency performance of the device. For instance, an 86 GHz f_T and 115 GHz f_{MAX} device with SiN passivation has been reported[8], and after etching away the SiN passivation layer, the f_T and f_{MAX} of the same device became 124 GHz and 230 GHz, respectively. In addition, the short-channel effect lowers R_{ds}, resulting in high frequency performance degradation. Briefly, the f_T and f_{MAX} could not be greatly improved only by reducing the gate from 180 to 80 nm, and all factors must be balanced.

4. Conclusion

In summary, we have fabricated and characterized AlGaN/GaN HEMTs (L_G = 80 nm) with SiN passivation on a sapphire substrate. By integrating several techniques, such as AlN interlayer, SiN passivation, high aspect ratio T-gate, low resistance ohmic contact and short drain–source distance, improved DC and RF performances have been achieved. The maximum drain current density and maximum peak extrinsic transconductance obtained were 1.41 A/mm and 317 mS/mm, respectively. This is the largest drain–source current device to date implemented with a domestic wafer and processes. The short channel effect could be eliminated by employing gate recess technology in future. On the same wafer, a unity current gain cut-off frequency of 74.3 GHz and a maximum oscillation frequency of 112.4 GHz were obtained. Further experimentation on balancing all of the factors affecting the f_T and f_{MAX} could be helpful to further improve device RF performances.

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