

Study of hybrid orientation structure wafer*

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Abstract: Two types of 5 μm thick hybrid orientation structure wafers, which were integrated by (110) or (100) orientation silicon wafers as the substrate, have been investigated for 15–40 V voltage ICs and MEMS sensor applications. They have been obtained mainly by SOI wafer bonding and a non-selective epitaxy technique, and have been presented in China for the first time. The thickness of BOX SiO_2 buried in wafer is 220 nm. It has been found that the quality of hybrid orientation structure with (100) wafer substrate is better than that with (110) wafer substrate by “Sirtl defect etching of HOSW”.

Key words: HOT; SOI; (110) crystal orientation; 15–40 V ICs; MEMS sensor

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1. Introduction

It is well known that CMOS ICs are usually made from (100) crystal orientation silicon wafer, and NMOS carrier mobility is about 2–3 times greater than PMOS carrier mobility, but most people might forget that hole mobility in (110) orientation silicon wafer is about 2 times larger than that in (100) wafer, which was found by Sato *et al.*^[1] in 1969. Many new technologies, such as strained silicon, have been developed as the design rule in CMOS technology scales down to the 45 nm node and beyond, and high hole mobility in (110) orientation wafer have been recognized again. Then, hybrid orientation technology (HOT), where NMOS transistors are fabricated on (100) wafer but PMOS transistors are fabricated on (110) wafer, was exploited^[2–9]. HOT improves PMOS transistor performance, maintains NMOS transistor performance and, in the meantime, reduces the mismatch of PMOS and NMOS transistor characteristics. In addition, (110) wafer has a larger piezoresistive coefficient than (111) and (100) wafer, which is widely used for MEMS sensors. Most of the HOT active layer thickness is usually much thinner (45–100 nm) and was used in 90 nm CMOS node or less outside China^[3,7], which is different from the thickness that we use.

2. Process flow

The process flow of the hybrid orientation structure wafer (HOSW) experiment is shown in Fig. 1. Both (110) and (100) wafers are 100 mm in diameter. The (110) wafer is n-type, whose resistivity is 10–20 $\Omega\cdot\text{cm}$, whereas (100) wafer is also n-type, whose resistivity is 7–10 $\Omega\cdot\text{cm}$.

First, we must obtain hybrid orientation SOI wafer. These SOI wafers are made by a conventional wafer bonding, grinding and SOI polishing process flow, and the wafer is different from the top Si layer in orientation. The (110) and (100) wafers were used as a handle wafer or a top Si layer, respectively. The

buried BOX thermal SiO_2 is about 220 nm thick and the top Si layer thickness is about 3.3–3.62 μm (Fig. 1(a)). A micrograph of hybrid orientation SOI wafer is shown in Fig. 2. There

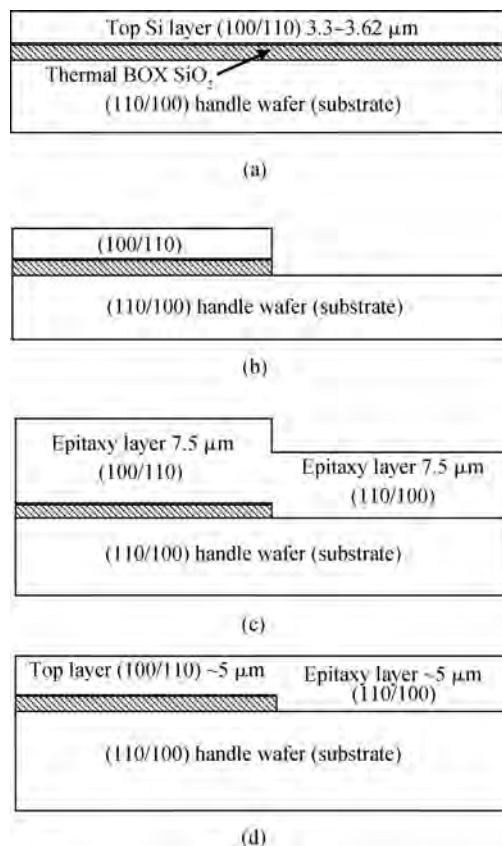


Fig. 1. HOSW process flow. (a) Formation of (110/100) or (100/110) hybrid orientation SOI. (b) A part of the top Si layer and BOX SiO_2 etching. (c) Non-selective epitaxy. (d) Silicon epitaxial layer CMP.

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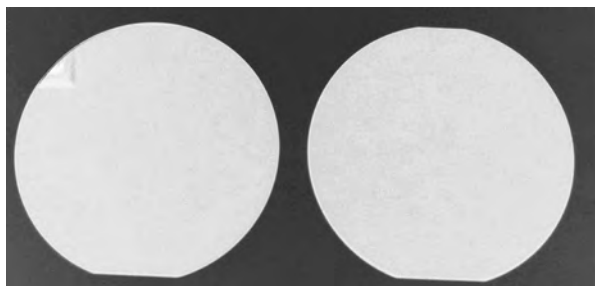


Fig. 2. Photo of hybrid orientation SOI wafer. The left SOI handle wafer orientation is (110) and the top Si layer is (100), and the right one is (100) and (110), respectively.

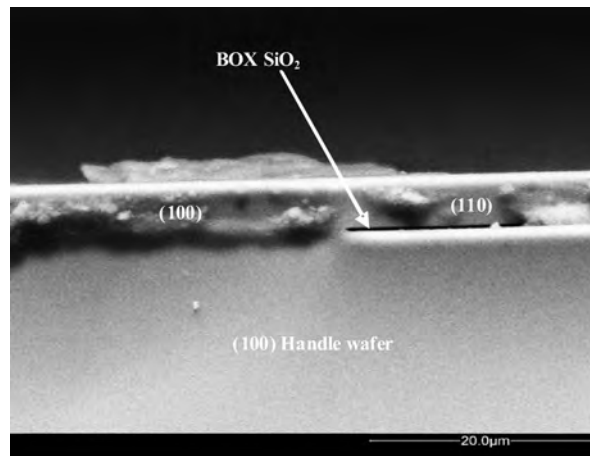


Fig. 4. Cross section of (100) HOSW.

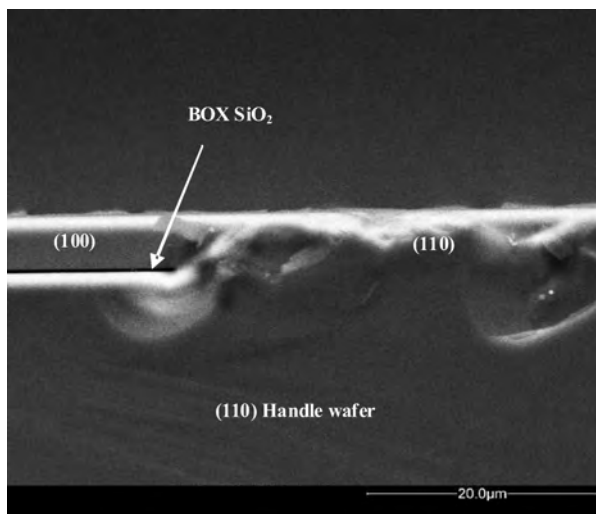


Fig. 3. Cross section of (110) HOSW.

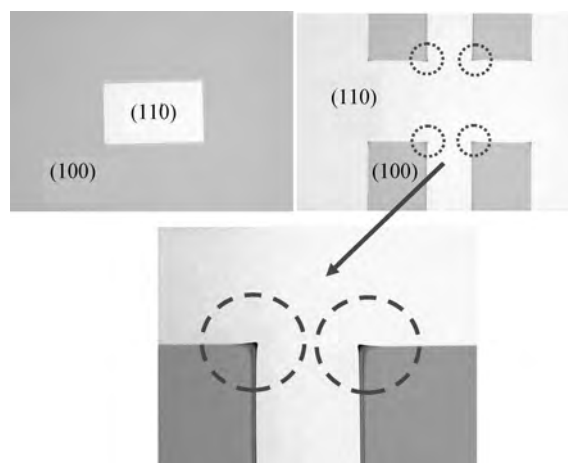


Fig. 5. Micrograph of HOSW surface.

is no defect in the upper left corner of the left-hand SOI wafer in Fig. 2 but there is a mirror reflection pattern.

Second, after the photolithographic process, a part of the top Si layer and BOX SiO₂ was etched, as shown in Fig. 1(b). Then a 7.5 µm thick non-selective epitaxial layer was deposited (Fig. 1 (c)).

Third, a roughly 5 µm thick silicon epitaxial layer was removed from the epitaxial wafer by CMP (Fig. 1 (d)). Then HOSW was carried out.

3. Results and discussion

3.1. Cross section of hybrid orientation structure

Figure 3 shows a cross section of the hybrid orientation structure with (110) handle wafer ((110) HOSW), and Figure 4 is a cross section of the hybrid orientation structure with (100) handle wafer ((100) HOSW). From Fig. 4, it can be seen that there is no distinct step across (110)/(100) on wafer surface. The top Si layer on BOX SiO₂ is about 5 µm thick and BOX SiO₂ thickness is about 0.22 µm.

3.2. Surface shape and defect indication

Both (110) and (100) handle wafer hybrid orientation structures had a thermal oxide, which formed in 950 °C vapor ambience, the oxide on the (100) surface is 98 nm thick, and the

oxide on the (110) surface is 136 nm thick. Figure 5 shows a micrograph of the hybrid orientation structure surface. In Fig. 5, the top left image is a (110) handle wafer hybrid orientation structure, where orientations inside and outside the rectangular pattern area are (110) and (100), respectively. However, the top right image is (100) handle wafer, where the orientations in and out of the rectangular pattern are (100) and (110), respectively. It can be seen clearly that there are many special sharp-angled corners (shown as dashed circles in the bottom image of Fig. 5) on (100) HOSW, but there are no such corners on (110) HOSW.

A photolithographic layout schematic on wafer is shown in Fig. 6. All of the patterns in the layout are rectangular.

To know what the surface quality of HOSW like, the wafer has been smashed by natural cleavage fracture. We put a suitable sized fragment into “Sirtl” etching solution (CrO₃ : H₂O : HF = 50 g : 100 mL : 100 mL) for about 2 min and then took it out to take a micrograph. It was found that (110) HOSW had some different behavior from (100) HOSW. First, the cleavage plane angle was about 60° in (110) HOSW (see Fig. 7), but it was 90° in (100) HOSW (see Fig. 8).

Second, there were some line defects on the surface of (110) HOSW, indicated by dashed ellipses in Fig. 7. There were almost no defects on (100) HOSW except for some along the edge of the fragment, as shown on the right part of Fig. 8. These

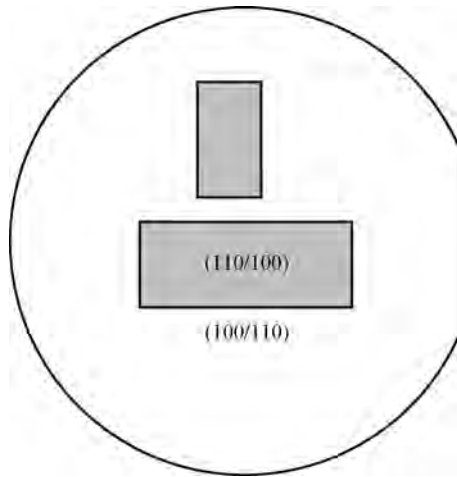


Fig. 6. Layout schematic on wafer.

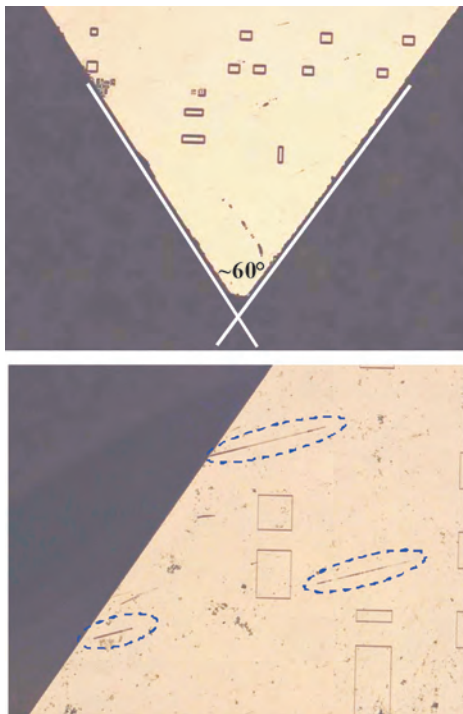


Fig. 7. Surface micrograph after (110) HOSW cleavage.

defects along the edge were probably caused by cleavage fracture mechanical stress.

4. Conclusions

Two types of $5\ \mu\text{m}$ thick hybrid orientation structures were realized mainly by SOI wafer bonding, non-selective epitaxy and CMP, and they have been presented in China for the first time. "Sirtl defect etching" of HOSW indicated that the quality of hybrid orientation structure with (100) wafer substrate is better than that with (110) substrate.

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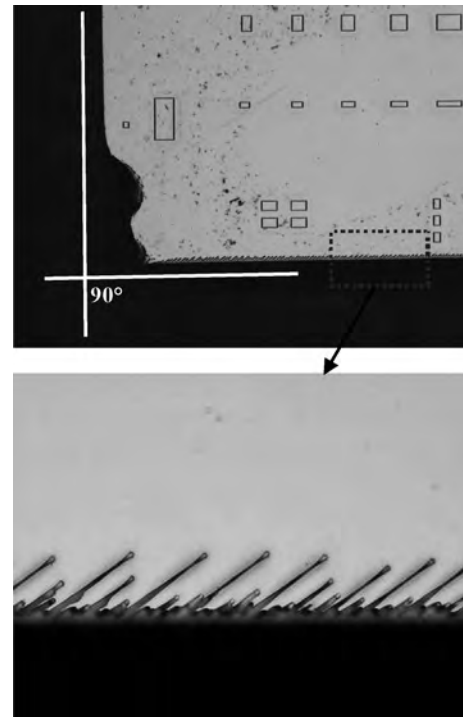


Fig. 8. Surface micrograph after (100) HOSW cleavage.

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References

- [1] Sato T, Takeishi Y, Hara H. Effects of crystallographic orientation on mobility, surface state density, and noise in p-type inversion layers on oxidized silicon surfaces. *Jpn J Appl Phys*, 1969, 8(5): 588
- [2] Fischetti M, Ren Z, Solomon P, et al. Six-band kp calculation of the hole mobility in silicon inversion layers: dependence on surface orientation, strain, and silicon thickness. *J Appl Phys*, 2003, 94(2): 1079
- [3] Yang M, Jeong L, Shi K, et al. High performance CMOS fabricated on hybrid substrate with different crystal orientations. *International Electron Devices Meeting*, 2003: 453
- [4] Nakamura H, Ezaki T, Iwamoto T, et al. Effects of selecting channel direction in improving performance of sub-100nm MOSFETs fabricated on (110) surface Si substrate. *Jpn J Appl Phys*, 2004, 43(4B): 1723
- [5] Mizuno T, Sugiyama N, Tezuka T, et al. (110)-surface strained-SOI CMOS technology. *IEEE Trans Electron Devices*, 2005, 52(3): 367
- [6] Stathis J H, Bolam R, Yang M, et al. Interface state generation in pFETs with ultra-thin oxide and oxynitride on (100) and (110) Si substrates. *Microelectron Eng*, 2005, 80(1): 126
- [7] Sung C Y, Yin H, Ng H Y. High performance CMOS bulk technology using direct silicon bond (DSB) mixed crystal orientation substrates. *International Electron Devices Meeting*, 2005: 225
- [8] Yang M, Chan V W C, Chan K K, et al. Hybrid-orientation technology (HOT): opportunities and challenges. *IEEE Trans Electron Devices*, 2006, 53(5): 965
- [9] Krishnamohan T, Kim D, Thanh V D. Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive currents and $\ll 60\ \text{mV/dec}$ subthreshold slope. *International Electron Devices Meeting*, 2008: 1