A CMOS G_m–C complex filter with on-chip automatic tuning for wireless sensor network application*

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Abstract: A G_m–C complex filter with on-chip automatic tuning for wireless sensor networks is designed and implemented using 0.18 μm CMOS process. This filter is synthesized from a low-pass 5th-order Chebyshev RLC ladder filter prototype by means of capacitors and fully balanced transconductors. A conventional phase-locked loop is used to realize the on-chip automatic tuning for both center frequency and bandwidth control. The filter is centered at 2 MHz with a bandwidth of 2.4 MHz. The measured results show that the filter provides more than 45 dB image rejection while the ripple in the pass-band is less than 1.2 dB. The complete filter including on-chip tuning circuit consumes 4.9 mA with 1.8 V single supply voltage.

Key words: complex filter; G_m–C; transconductor; automatic tuning; wireless sensor networks

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1. Introduction

Today, most receivers work with an intermediate frequency (IF). Zero-IF and low-IF topology are popular as a low-cost full chip solution can be obtained[1]. In recent years, the zero-IF receiver has been introduced in several applications, but its baseband operation results in filter saturation and distortion, both caused by DC-offsets and self-mixing at the inputs of the mixers. Thus, zero-IF requires DC-offset removal or a cancellation scheme. This further complicates the design and increases the current consumption. However, a low-IF receiver can be applied with a high degree of integration and better performance at the same time[2, 3]. In low-IF topology, the RF signal is converted to a low IF. This topology avoids the DC-offset problem but leads to the disadvantage of higher image signal suppression being required.

One solution is to use a complex (polyphase) bandpass filter. Figure 1 shows the front-end topology of a low-IF receiver. The RF signal is amplified and down-converted to IF by the LNA and mixers. Then, the channel selection is performed by an active complex filter. This filter can effectively attenuate the image signal and the folded-back strong interference after down-conversion. An image rejection of 40 dB, which is easily achievable with an integrated design, is sufficient for a low-IF WSN receiver[4–7].

In general, active-RC and G_m–C topologies are proven to be simple and effective for implementing continuous-time filters on a single CMOS chip. To achieve an accurate frequency response, an automatic tuning scheme is needed to ensure that the frequency response is insensitive to fabrication process tolerances, operating temperature variations and aging. In active-RC architecture, the automatic tuning is often done by the switched capacitor array and a digital logic circuit[8–12], which results in less accurate tunability. While in G_m–C architecture, the automatic tuning is often implemented by means of phase-locked loop (PLL)[13–15], which in theory can realize a precise frequency response.

2. Complex filter principle

To understand the ability of complex filters to reject the image signal, a complex representation of the receiver block diagram is shown in Fig. 2. We assume that only the desired signal $x_{sig}\cos(\omega_{LO}+\omega_{IF})t$ and the image signal $x_{image}\cos(\omega_{LO}-\omega_{IF})t$ are presented at the mixer input. Generally, the image signal x_{image} may be much larger than the desired signal x_{sig}. After the mixer and the complex filter, the output is $A_{mixer}x_{sig}e^{j\omega_{IF}t}/2$, where A_{mixer} is the voltage gain of the mixer.

Figure 3 illustrates the complex mixing and filtering operation. Note that after down conversion, the $2\omega_{IF}$ frequency separation between the signal and image is still preserved. Then the complex filter passes the desired signal at ω_{IF}, while attenuating the signal at $-\omega_{IF}$. Since the filter has a unsymmetrical frequency response around the jω axis, its time-domain response is complex (hence the name "complex filter")[16].

These complex operations are performed in practice as follows. Multiplication of the real RF signal by $e^{j\omega_{LO}t}$ is performed

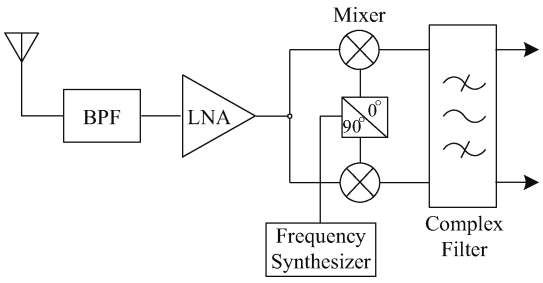

Fig. 1. Front-end topology of a low-IF receiver.

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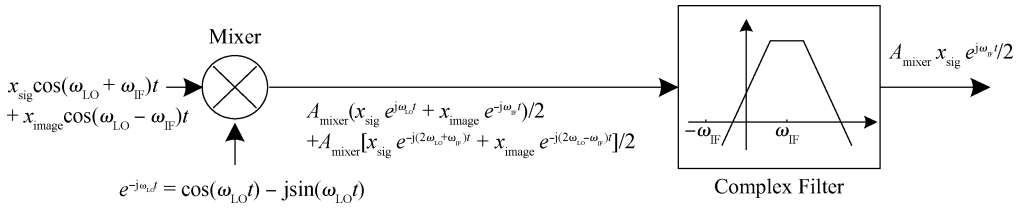


Fig. 2. Receiver image rejection architecture in the complex domain.

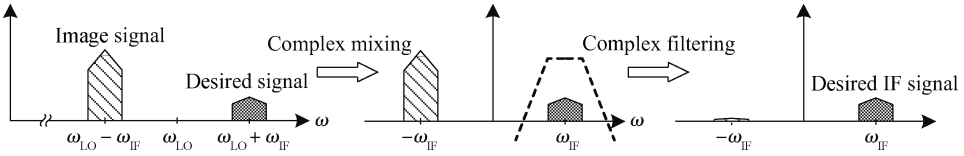


Fig. 3. Frequency translation of complex mixing and complex filtering.

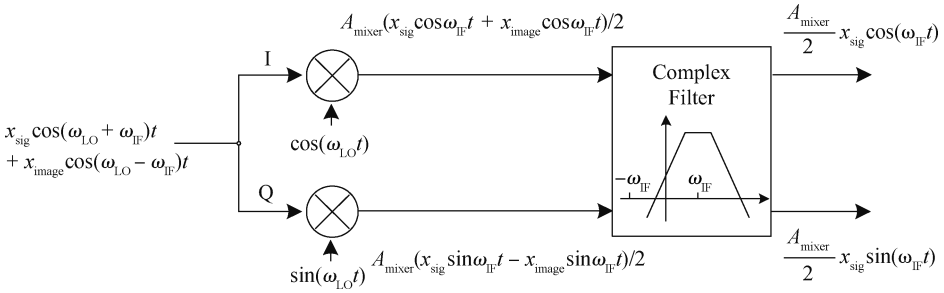


Fig. 4. Practical implementation of the receiver image rejection architecture in Fig. 2.

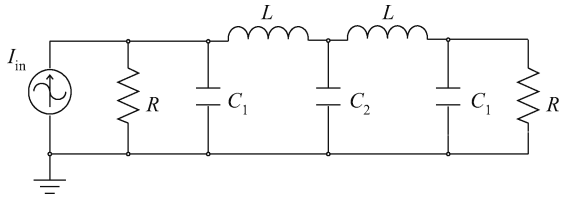


Fig. 5. RLC ladder prototype.

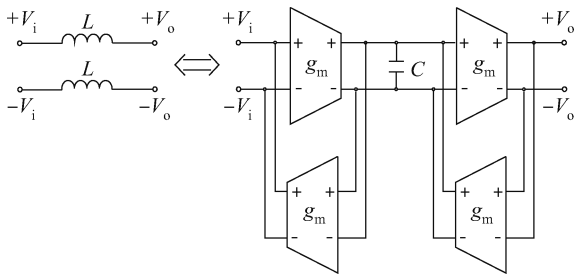


Fig. 6. A differential G_m–C inductor.

in practice using a complex (quadrature) mixer, which consists of two mixers whose LO inputs are in quadrature phase, the desired signal at the mixer output is located at the positive IF frequency while the image signal is located at the negative IF frequency. Practical implementation in a real domain is shown in Fig. 4.

3. Architecture design of complex filter

The method used to synthesize this complex filter is based on the classical simulation of signals in a double terminated reactance ladder prototype. A general advantage of this approach is that the resulting circuit has low pass-band sensitivity to element value variations just like in the ladder prototype[17].

The design is carried out in three steps. First, a low-pass ladder prototype is represented. Then, by replacing the inductors and resistors in the prototype with transconductors and capacitors, a fully-balanced low-pass filter containing only transconductors and capacitors is derived. Finally, using linear frequency transformation by transconductor pairs, the desired complex filter is derived from the low-pass filter.

A 5th-order Chebyshev low-pass response is chosen, and whose corresponding ladder is shown in Fig. 5. Then, the inductor L and resistor R in the prototype are replaced with transconductors and capacitors to obtain an active low-pass filter. A resistor can be directly implemented by a transconductor. Figure 6 shows how a differential active inductor is implemented by a transconductor and capacitance. It can be calculated that the equivalent value of the differential inductor is

$$L=\frac{2C}{g_m^2}. \tag{1}$$

The transfer function of a complex filter is obtained by frequency translating the transfer function of a prototype low-pass filter, as shown in Fig. 7. In this case, the pass band is located at the positive frequency, while the stop band extends to all of the negative frequency. The frequency transformation

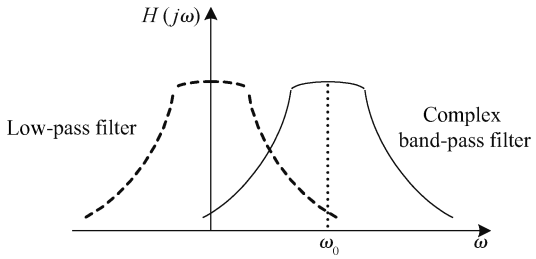


Fig. 7. Transfer function for a low-pass filter and the derived complex band-pass filter.

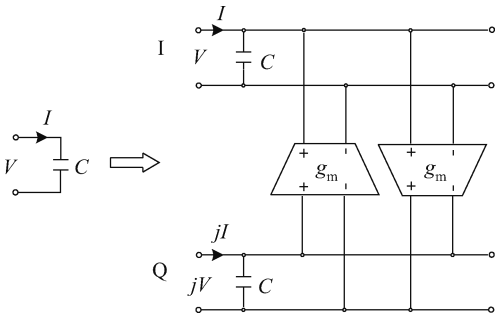


Fig. 8. Linear frequency transformation for a differential capacitance.

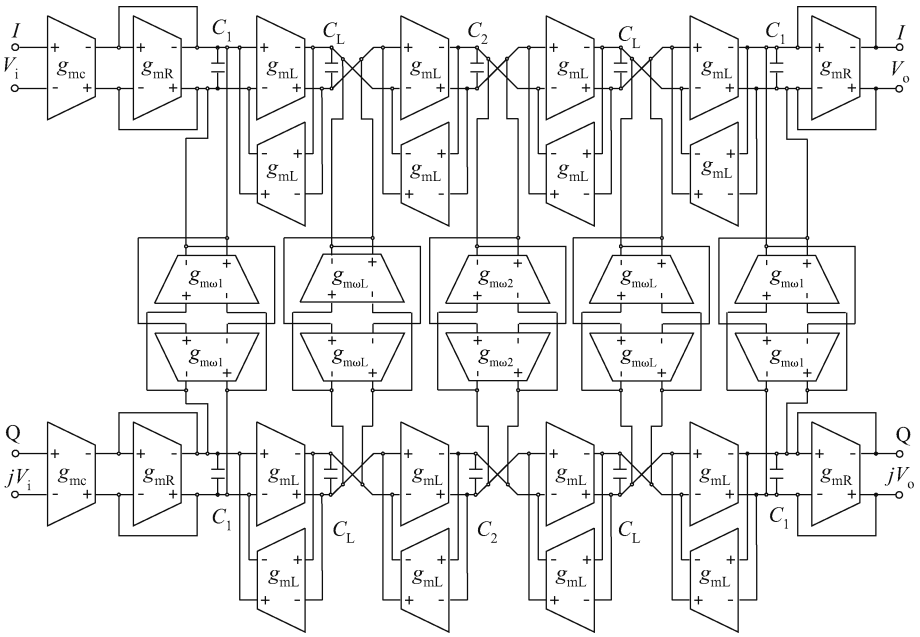


Fig. 9. Complete balanced differential G_m–C complex filter.

$$H(j\omega) \rightarrow H(j(\omega - \omega_0)), \tag{2}$$

can be straightforwardly used to derive the structure of a complex filter based on G_m–C technique, since Equation (2) can be applied to each reactive component in the active low-pass filter[18]. Focusing on a capacitance C, Equation (2) becomes

$$j\omega C \rightarrow j\omega C - j\omega_0 C, \tag{3}$$

where $\omega_0 C$ is a conductance with a frequency-independent value. Figure 8 shows the linear frequency transformation for a differential capacitance and it can be calculated that

$$\omega_0 = \frac{g_m}{2C}. \tag{4}$$

The complete balanced differential G_m–C complex filter is synthesized as shown in Fig. 9 where the transconductor g_{mc} is used to convert input voltage to current.

4. Tunable linear transconductor design

G_m–C technique is chosen to offer high speed capability and continuous tenability, but the problems due to poor linearity compared with the active-RC technique must be overcome. Many techniques have been proposed in the literature to improve linearity performance. Among these approaches, the simplest and perhaps most widely adopted is that based on resistive source degeneration.

The schematic diagram of a fully balanced folded cascode transconductance amplifier with a CMFB circuit is depicted in Fig. 10. Transistors M1 and M1' form the input differential pair, whose transfer characteristic is linearized by the voltage-controlled degenerating "resistors" M2 and M2' working in the triode region. The small signal transconductance of this amplifier is

$$G_m = \frac{g_{M1}}{1 + g_{M1} R_{M2}/4}, \tag{5}$$

where g_{M1} is the transconductance of transistors M1 and M1' and R_{M2} is the equivalent resistance of M2 and M2' as Equation (6) shows.

$$R_{M2} = \frac{1}{\mu_n C_{ox} \dfrac{W}{L}(V_{GS2} - V_{TH2})}. \tag{6}$$

Transconductance tunability is a feature required to com-

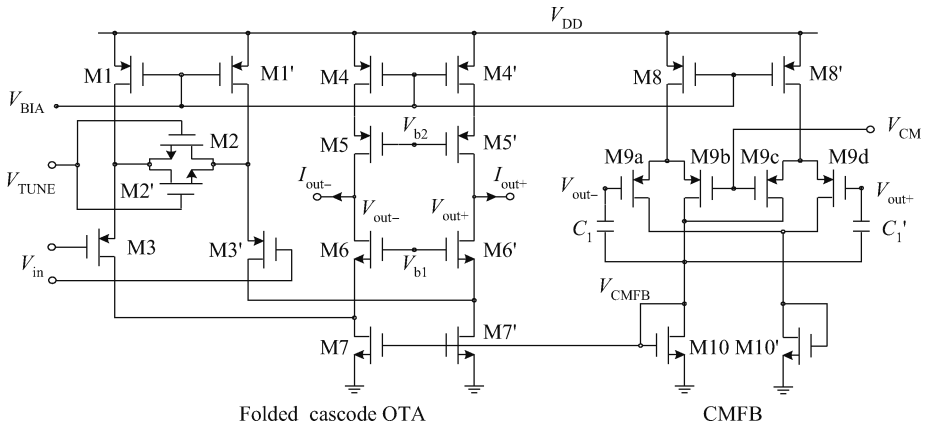


Fig. 10. Linearized differential transconductance amplifier.

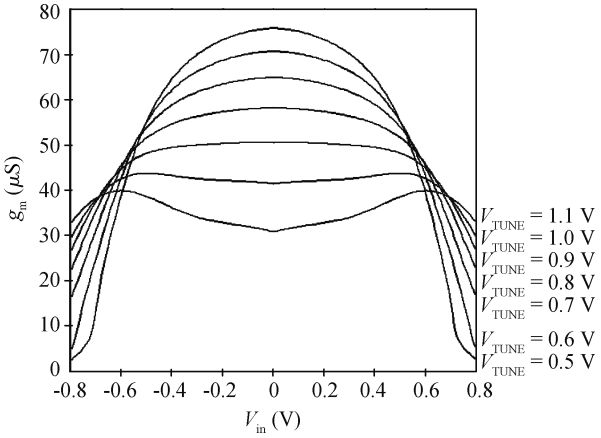


Fig. 11. Transconductance g_m of a transconductor used in the filter with different V_{TUNE}.

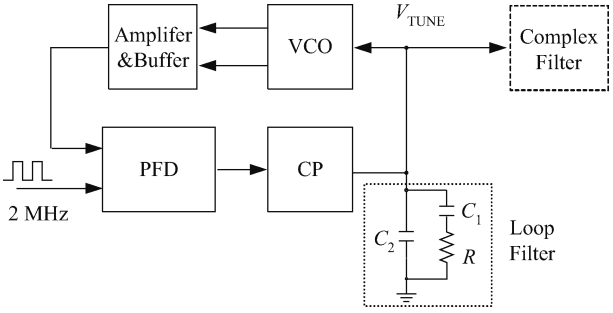


Fig. 12. PLL used for frequency tuning.

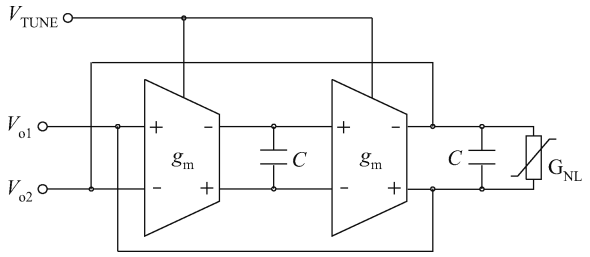


Fig. 13. Second-order ring VCO.

pensate for process variations and operating temperature variations to guarantee that the center frequency and bandwidth will have the desired value. Since transistors M2 and M2' in the triode region are used as source degeneration devices, their equivalent resistance can be readily modified. According to Eqs. (5) and (6), transconductance tunability can be easily realized by tuning the gate voltage V_{TUNE} generated by the PLL, which will be described and proposed in Section 5.

Figure 11 shows the transconductance g_m of a transconductor used in the filter with different tuning voltage V_{TUNE}.

5. Automatic tuning technique

In order for an active filter to achieve an accurate frequency response, automatic tuning is important. In this design, the phase-locked loop shown in Fig. 12 is used for both center frequency and bandwidth tuning. A reference frequency of 2 MHz is set to match the center frequency of the filter. Phase frequency detector (PFD) and charge pump (CP) circuits are designed with a traditional structure scheme and the loop filter is composed of off-chip resistors and capacitors.

The voltage-controlled oscillator (VCO) is phase locked to a reference clock and the filter uses the same control voltage V_{TUNE}. The main problem is the implementation of the VCO that can be well-matched to the filter to be tuned. The second-order ring VCO shown in Fig. 13 is designed using the same unit transconductance elements, capacitors and layout disposition. It can be calculated that

$$g_m v_{o1} \frac{1}{s2C}(-g_m)\frac{1}{s2C} = v_{o1}, \tag{7}$$

so the oscillating frequency of the VCO is

$$\omega_{OSC} = \frac{g_m}{2C}, \tag{8}$$

which is the same as Eq. (4).

Another key issue to be carefully considered is regulation of the oscillation amplitude. As shown in Fig. 11, although the transconductor is linearized by source degeneration, there is a limited linear region around zero input voltage among the whole input range. To avoid tuning error, the oscillation amplitude must be controlled within a proper range.

A nonlinear conductance G_{NL} as shown in Fig. 13 is used for amplitude regulation in the VCO[14]. It plays two roles for

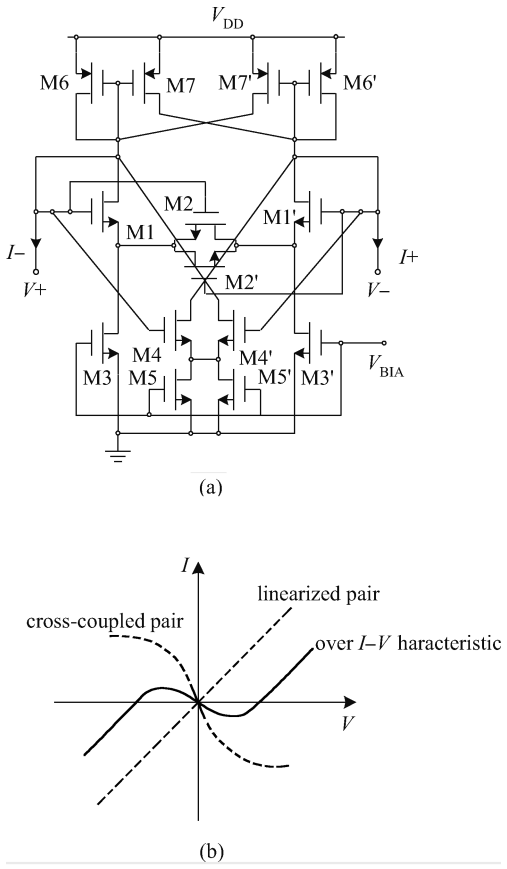


Fig. 14. Nonlinear conductance. (a) Schematic diagram. (b) I–V characteristic.

the oscillator. First, for small signals, it is equivalent to a negative conductance and, therefore, will ensure start-up of the oscillation. Then, after the start-up, the G_{NL} will effectively control the oscillation to reach stable amplitude within the linear range of the transconductor to avoid tuning error.

Figure 14(a) shows the schematic diagram of the nonlinear conductance G_{NL}, the cross-coupled MOS differential pair M4, M4' biased by current sources M5, M5' is added to a linearized transconductance stage M1, M1', M2, M2'. This circuit results in the special I–V characteristic shown in Figure 14(b), which will ensure a well-controlled oscillation amplitude.

6. Experimental results

The filter described above, including the automatic tuning circuit, has been implemented in the TSMC 0.18 μm CMOS process. Figure 15 is a photomicrograph of the complete circuit and its area is 1.18 × 1.16 mm^2. Buffers using PMOS source followers have been added on the chip for measurement purposes. The filter operates from 1.8 V power supply and the current consumption of the complete filter circuit excluding the buffers is 4.9 mA.

To test the filter frequency characteristics, Agilent E4438C is used to generate input quadrature sinusoidal signals. The measured output spectrum of the filter with 2 MHz and 4 MHz input signals with the same magnitude of 50 mV is shown in Fig. 16. It can be calculated that the output signal magnitude is 14.32 mV and 0.35 mV, so the voltage gain at

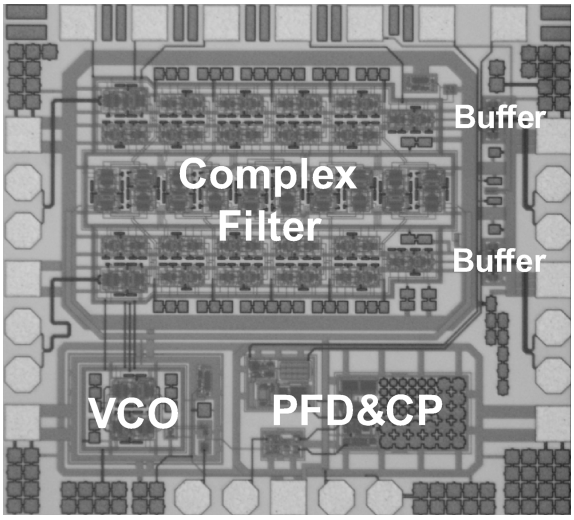
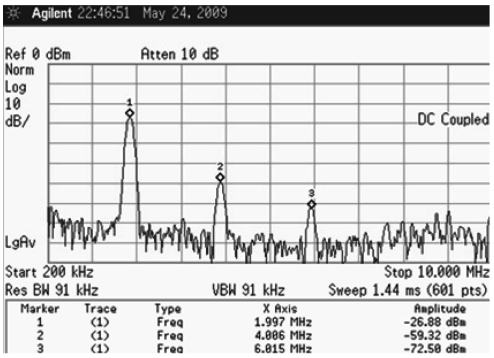
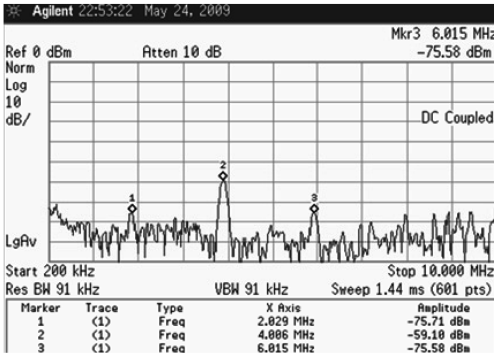


Fig. 15. Photomicrograph of the complex filter.



(a)



(b)

Fig. 16. Measured output spectra. (a) 2 MHz input signal. (b) 4 MHz input signal.

2 MHz and 4 MHz is –10.86 dB and –43.08 dB, respectively. Testing other frequency points from –2 to 6 MHz, we can obtain the filter frequency response between –2 to 6 MHz, as shown in Fig. 17. The figure shows that the image rejection ratio is more than 45 dB, which is sufficient for WSN specifications. The typical performance characteristics of the complex filter are summarized in Table 1.

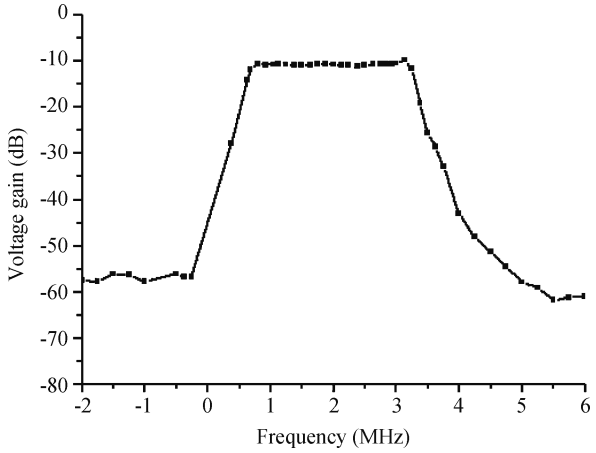


Fig. 17. Frequency response.

Table 1. Typical performance characteristics of the complex filter.

Parameter	Value
Filter response	Chebyshev
Filter order	5 + 5
Center frequency	2 MHz
Bandwidth	2.4 MHz
Input 1-dB compression point	0.23 V
Image rejection	> 45 dB
Passband ripple	< 1.2 dB
Supply voltage	1.8 V
Consumed current	4.9 mA
Frequency tuning error	< 7%

7. Conclusion

A fully balanced G_m–C complex filter with on-chip automatic frequency tuning is proposed in this paper. A conventional phase-locked loop is used to realize the automatic tuning. According to the measurement results, with the tuning system, the filter results in an accurate frequency response with high image rejection. The complete filter, including the tuning circuit, consumes 4.9 mA with 1.8 V single supply voltage.

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