Design and implementation of a hybrid circuit system for micro sensor signal processing*

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Abstract: This paper covers a micro sensor analog signal processing circuit system (MASPS) chip with low power and a digital signal processing circuit board implementation including hardware connection and software design. Attention has been paid to incorporate the MASPS chip into the digital circuit board. The ultimate aim is to form a hybrid circuit used for mixed-signal processing, which can be applied to a micro sensor flow monitoring system.

Key words: aircraft; flow monitoring; micro sensor signal processing; hybrid circuit
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1. Introduction

One of the big challenges for the next generation of civil aircraft is to dramatically reduce emissions. One way of significantly reducing drag and hence fuel burn and emissions in smaller civil aircraft is to design the aircraft to have natural laminar flow on the wings[1]. Thus a monitoring system consisting of micro sensors based on MEMS and their signal processing circuit systems will be required to demonstrate the flow on the surface of the aircraft wings. At present, micro sensors are receiving increasing attention from researchers in the fluid field[2−5]. However, the circuit system with low-power and small area would have to be as light as possible to process the sensor signal.

The micro sensor signal processing circuit system is essentially a mixed-signal system, because it needs to collect the analog signal from micro sensors and condition the received analog signal for digitization. Initially, there was a choice of three different approaches to manufacture a mixed-signal circuit system: (1) a fully integrated and customized ASIC design, (2) an approach combining discrete, off-the-shelf components with a customized mount, and (3) a hybrid circuit including off-the-shelf components and an integrated ASIC design that can be customized to exclude or include particular circuits, as desired. Since option (1) was a very high cost option with a high level of associated risk, it was discounted as a practical option at this stage of development[1]. Option (2) was also discounted because of the difficulty in choosing the most appropriate components. This left the hybrid approach (3) as the most sensible option at the current maturity level of the project. On the one hand, it can be customized to include the pivotal circuit, such as the analog part of the mixed circuit system, as desired, and ensure the whole system performance; on the other hand, it may decrease the manufacture cost and risk. Our work is an example of this hybrid circuit, namely, designing an integrated analog signal processing circuit system chip and mounting it in a digital signal processing circuit board for micro sensor signal process.

In this paper, the most recent work is reported, which has concentrated on two aspects. First, the monolithic low-power micro sensor analog signal processing circuit system (MASPS) will be introduced, which has been designed and implemented based on Central Semiconductor Manufacturing Corporation (CSMC) 0.5 μm double-poly three-metal (2P3M) 3.3 V CMOS technology. Second, a digital signal processing circuit board will be designed, and how the MASPS chip could be incorporated into the board to monitor the flow on the surface of aircraft wings will be considered. In order to set the scene for the reader, chip photographs are shown in Fig. 1.

2. Conceptual design

Figure 2 shows the framework of the proposed flow monitoring system, which consists of micro sensors and their signal processing circuit system, which actually includes two parts: an analog circuit (MASPS) and an interrelated digital circuit. Having established that the micro sensor was a viable approach to detect the boundary layer flow, the next work was to generate the idea for the design of signal processing circuit.

2.1. Analog circuit chip design

As shown in Fig. 1, the analog signal processing circuit system is composed of three important modules:

(1) Analog low pass filter: this is not only to restrict the noise and interference, so that the signal discrimination can be enhanced, but also to serve as the front end antialiasing filter of over sampling analog-to-digital converter (ADC) in the system. It is made up of a switched capacitor filter (SCF) and its antialiasing prefilter and smoothing postfilter, in which the SCF with a cutoff frequency of 0.7 kHz is the most important part. As shown in Fig. 3, the filter is based on the Butterworth type and has small ripple in the passband.

(2) Sigma–delta modulator: the output from the filter is an analog signal and the sigma–delta modulator is used to realize the conversion of the analog signal to a pulse-code modulation

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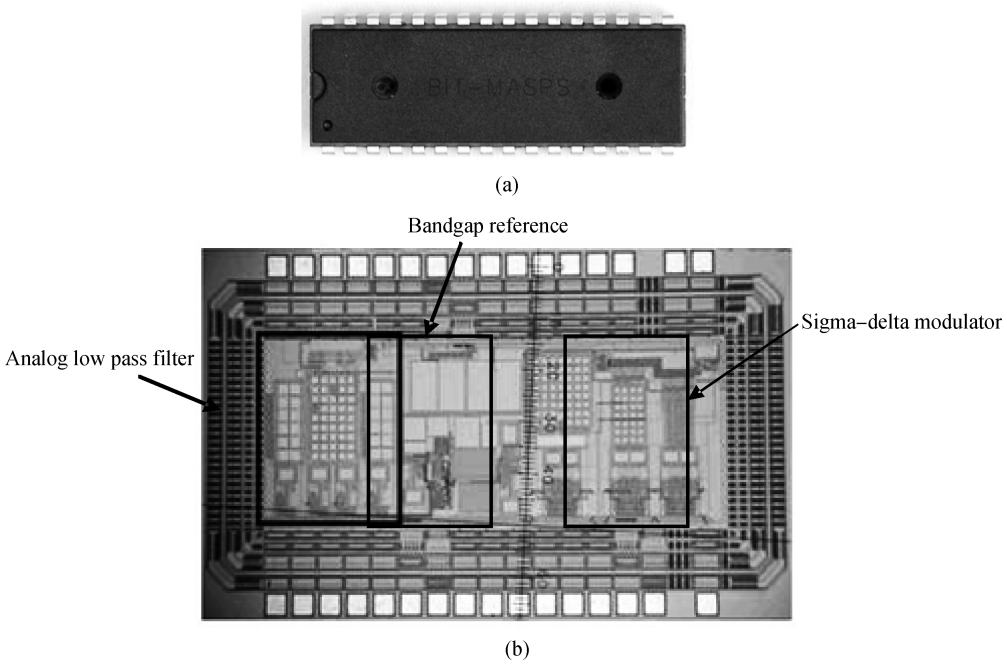

Fig. 1. Micro sensor analog signal processing circuit system chip photographs. (a) Chip package photograph. (b) Chip photomicrograph.

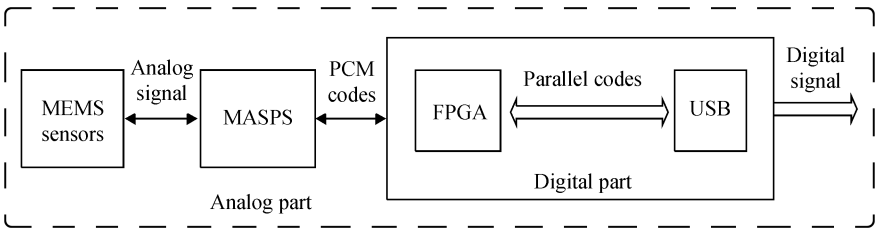

Fig. 2. Flow monitoring system framework.

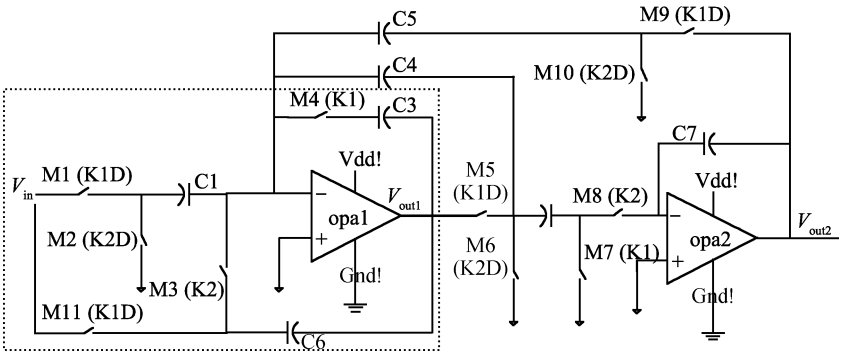

Fig. 3. Switched-capacitor filter circuit with correlated double sampling technology.

(PCM) code. A second-order one-bit sigma–delta modulator, with a resolution over 12 bits, was designed, which is most appropriate for the low-power design[6].

(3) Bandgap reference: this is one of the essential modules in the analog system. It offers a reference to other functional blocks. Its performance seriously hampers the overall signal processing system. The circuit was realized by a low-power voltage reference consisting of pure MOSFET.

In addition, some effective methods and technology have been adopted in this circuit system, such as sub-threshold technology, correlated double sampling (CDS) technology, and optimization switches. It has been fabricated with CSMC 0.5 μm 2P3M 3.3 V CMOS technology, with satisfactory results. The chip (MASPS) photomicrograph is shown in Fig. 1. The framework is shown in Fig. 4. The total performance is presented in Table 1.

2.2. Digital circuit board design

Having finished the design of the analog circuit part chip, the next steps were to turn to the design of the interrelated digital signal processing circuit board, including the hardware de-

Table 1. Performance summary of MASPS.

Parameter	Sample rate	Bandwidth	Power supply	Power dissipation	Area
Value	1.024 MHz	0.7 kHz	3.3 V	9.55 mW	3.30 mm^2

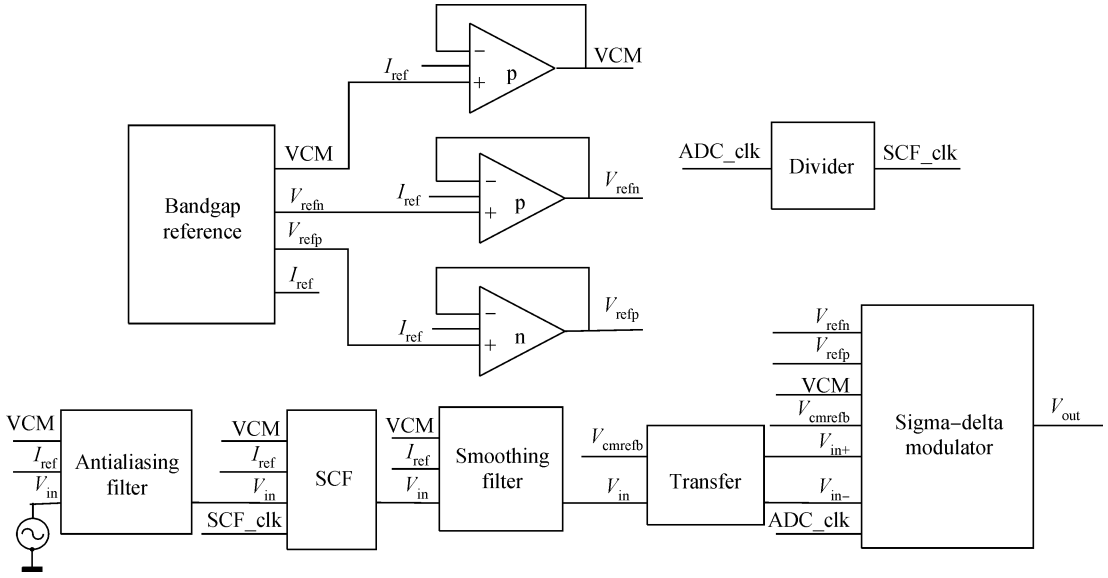

Fig. 4. Micro sensor analog signal processing circuit system framework.

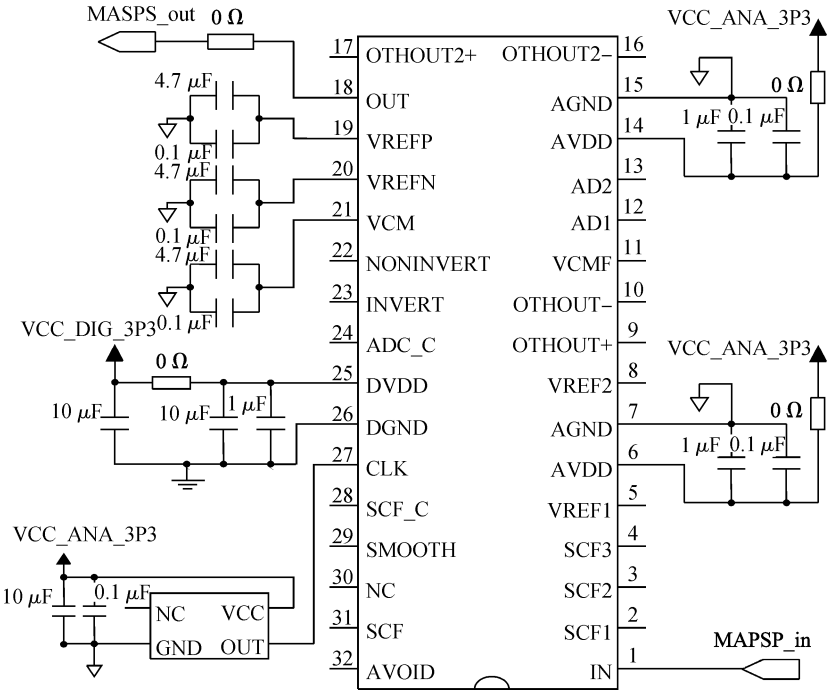

Fig. 5. Hardware connection of MASPS.

sign and software design, and apply the MASPS chip to the board and form the hybrid micro sensor signal processing circuit system.

As shown in Fig. 2, the digital signal processing circuit comprises two parts: a field programmable gate array (FPGA) and a universal serial bus (USB). The goal of the FPGA is to control the MASPS chip and IO interface circuits. Another purpose is to collect and convert the serial PCM codes from a sigma–delta modulator to 16-bit parallel digital codes. The USB is chosen as the IO interface circuit for data communication with peripheral equipment.

2.2.1. Hardware design

The first step in producing the digital signal processing circuit board was to design the hardware circuits using standard off-the-shelf components. Of course, the MASPS chip

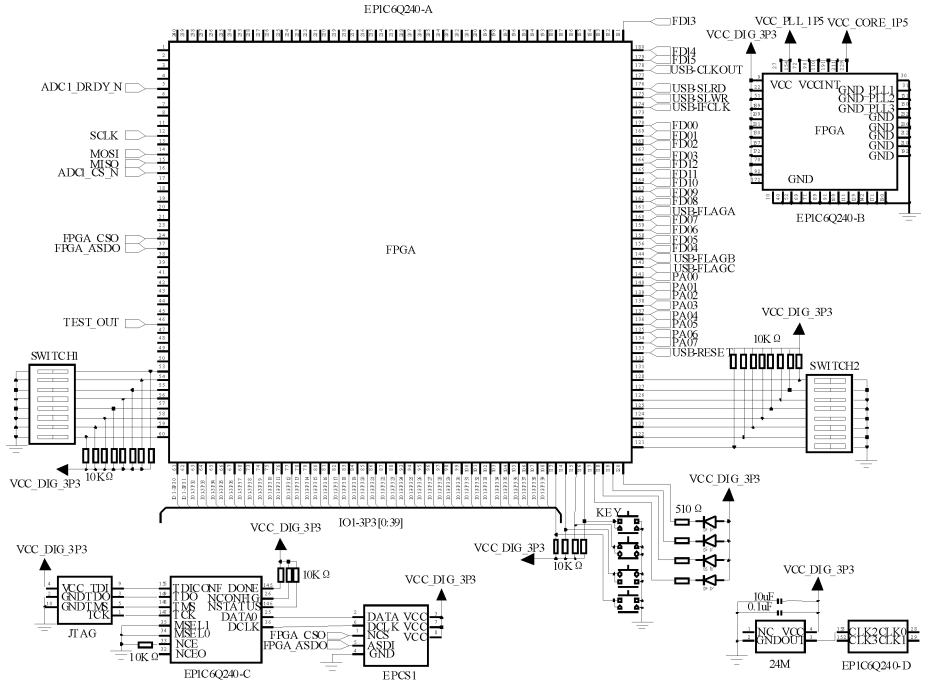

Fig. 6. Hardware connection of the FPGA.

also needs peripheral equipment to ensure that it can be incorporated into the digital circuit board.

Figure 5 shows the hardware connection of the MASPS chip. A 1.024 MHz crystal is connected to CLK ports to offer the whole clock. The chip has one input port and one output port. The output of the micro sensors is connected to the input port and then converted into PCM codes with a rate of 1.024 Mbps at the rising edge of the working clock. The output port is connected to the FPGA directly. The FPGA chip (EP1C6Q240) (as shown in Fig. 6) is made by ALTERA Corporation[7]. In addition, good power supply bypassing techniques are used in the circuit for the purpose of reducing coupling back to the analog input port. An external RC network is also used to further filter high frequency noise.

Figure 7 shows the hardware connection of the USB interface circuit. It is used to transport data from the FPGA to peripheral equipment. The USB chip (CY7C68013-56) is made by CYPRESS Corporation. It is configured to work in slave mode through the IFCONFIG signal in the framework program. A 24 MHz parallel resonant crystal is connected to XTALIN and XTALOUT ports. At high speed mode, the output bit rate can achieve as high as 480 Mbps, which meets the demand of real time transmission. In addition, an external EEPROM (24LC64) is needed to solidify the framework program[8].

2.2.2. Software design

The next step in producing the digital signal processing circuit board was the software design by using the software Quartus Ⅱ 9.1 and the hardware description language VHDL[9]. In the software design, the work must be finished: first, collecting the PCM codes from MASPS chip in correct timing; second, sending the PCM codes to USB interface.

As described in Part 2.2.1, the PCM codes received from

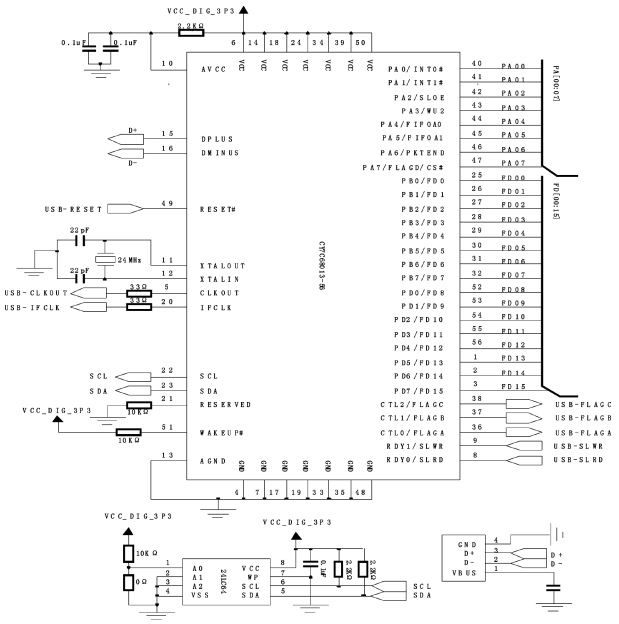

Fig. 7. Hardware USB connection.

the MASPS chip are put out at the rising edge of the working clock (1.024 MHz). So they must be collected by the FPGA at the falling edge of the clock. Moreover, the PCM codes are serial data, but the USB FIFO is a 16-bit parallel data bus, so the data conversion must be carried out. A 16-bit shift register is chosen in the program, owing to its economization and high efficiency.

The FPGA program controlling the USB chip is based on the slave FIFO asynchronous read-and-write timing. The USB slave FIFO architecture has eight 512-byte blocks in the endpoint RAM that directly serve as FIFO memories. These memories are controlled by FIFO control signals, such as SLRD,

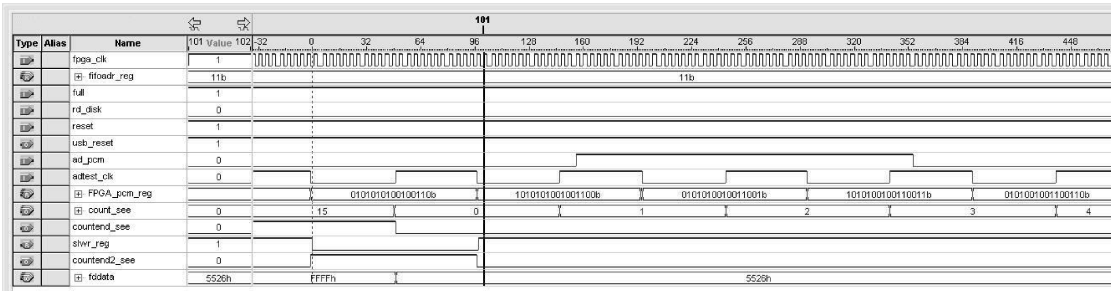

Fig. 8. Timing simulation results.

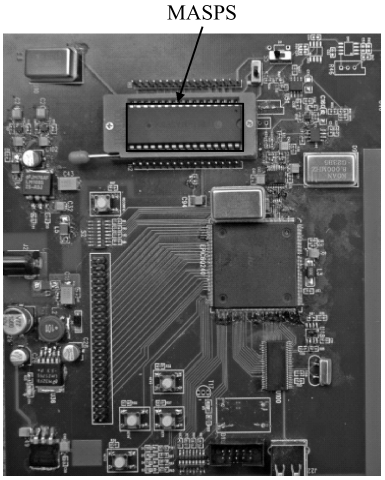

Fig. 9. Hybrid micro sensor signal processing circuit system.

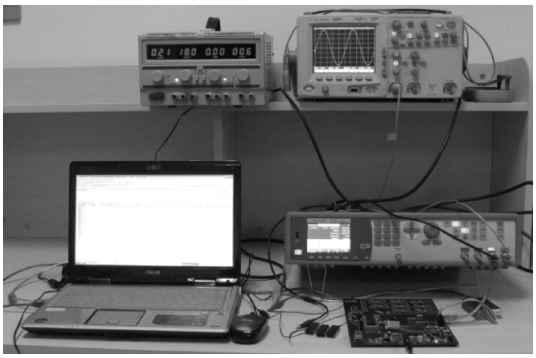

Fig. 10. Testing environment and apparatus.

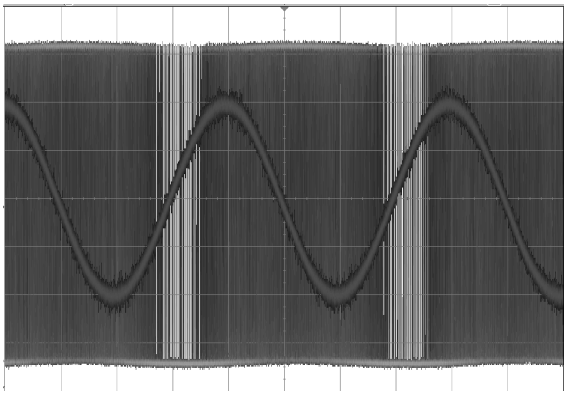

Fig. 11. Measurement wave of the MASPS chip.

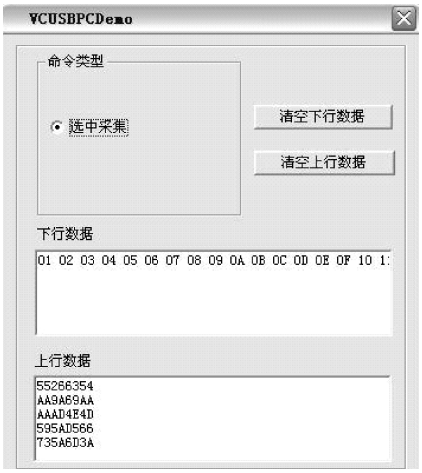

Fig. 12. Collection data of the computer.

SLWR, SLOE, FLAGS, which are connected to the FPGA directly. When the data from the FPGA are ready for transmission, FIFO's endpoint address is set as "11". Meanwhile, if FIFO's full signal is "1", which means that FIFO is not full, data can be written into FIFO for peripheral equipments to read them out.

When the FPGA program was finished, it was downloaded to the FPGA through the JTAG interface for further verification. The logical analyzer signal table was used to observe the real-time data in FPGA ports. The timing simulation results are shown in Fig. 8.

3. Measurement

Having finished the design and fabrication of the hybrid micro sensor signal processing circuit system (shown in Fig. 9), the overall performance of the system was tested and verified in an Agilent open laboratory. Figure 10 shows the testing environment and apparatus.

The test was done with a sine wave input signals with different frequency and amplitude, which were generated by function waveform generators (81150A). Figure 11 shows the measurement wave of the MASPS chip.

Figure 12 shows the output data connected by the computer, in hexadecimal form, when the collecting button in the computer program is chosen.

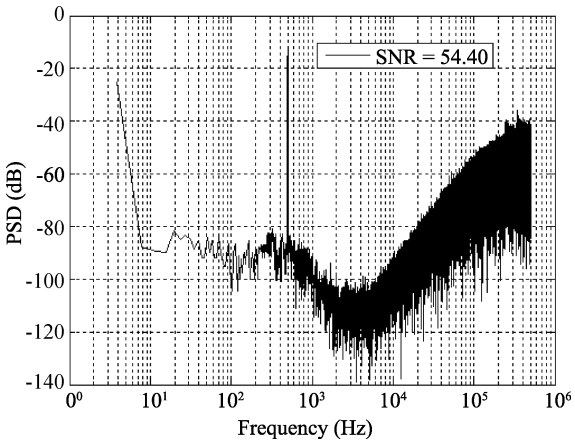

Fig. 13. Measured micro-sensor signal processing system spectrum.

Figure 13 shows the fast Fourier transform (FFT) plots at a sampling rate of 1.024 MHz. They demonstrate a whole chip SNR of 54.40 dB for 250 mVpp and a 500 Hz frequency input signal.

4. Conclusion

This paper presents a hybrid signal collecting and processing circuit system applied in a micro sensor flow monitoring system for the detection of the boundary layer flow on the surface of aircraft wings in real time. Considering the manufacture process, cost, and feasibility of the mixed-signal circuit system at this stage of development, the hybrid circuit design method is chosen to implement the micro sensor signal processing circuit system. The hybrid circuit contains an analog circuit chip and a digital circuit board. In this paper, the design of the chip and the board has been presented and the functions have been verified through chip and system measurement, which is well suited to the design of micro sensor mixed-signal processing and is more feasible and relatively effective for aircraft flow monitoring applications.

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