A programmable gain amplifier with a DC offset calibration loop for a direct-conversion WLAN transceiver

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Abstract: A high-linearity PGA (programmable gain amplifier) with a DC offset calibration loop is proposed. The PGA adopts a differential degeneration structure to vary voltage gain and uses the closed-loop structure including the input op-amps to enhance the linearity. A continuous time feedback based DC offset calibration loop is also designed to solve the DC offset problem. This PGA is fabricated by TSMC 0.13 μm CMOS technology. The measurements show that the receiver PGA (RXPGA) provides a 64 dB gain range with a step of 1 dB, and the transmitter PGA (TXPGA) covers a 16 dB gain. The RXPGA consumes 18 mA and the TXPGA consumes 7 mA (I and Q path) under a 3.3 V supply. The bandwidth of the multi-stage PGA is higher than 20 MHz. In addition, the DCOC (DC offset cancellation) circuit shows 10 kHz of HPCF (high pass cutoff frequency) and the DCOC settling time is less than 0.45 μs.

Key words: linear-in-dB; PGA; DC offset calibration
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1. Introduction

In wireless communication systems, the energy of the received signal spreads over a wide dynamic range after passing through unpredictable propagation paths, so a programmable gain amplifier (PGA) is usually adopted in the signal chain. The main function of the PGA is to maximize the dynamic range of the system by maintaining a fixed voltage output for different signal inputs. An important requirement for the PGA is a linear gain-in-dB control characteristic. This exponential gain control is required to achieve a wide dynamic range and to maintain the AGC loop settling time independent of the input signal level. Another consideration in many PGA circuits is the DC offset level. In a direct-conversion receiver, the main causes of DC offset are layout mismatch and self-mixing of the leakage local oscillator (LO) signal. After the mixer stage, the gain provided in each of the I and Q paths is in the 64 dB range, and then any differential offset at the mixer output may get enough amplification to cause clipping within the signal path, or at the output of the receiver. Therefore, offset suppression is necessary otherwise it will degrade the system dynamic range. In this work, a PGA with a continuous time feedback calibration loop is presented to reduce the DC offset without large capacitance.

Figure 1 shows the direct-conversion architecture for a WLAN transceiver. The power level of the transmitted or received signal can be controlled by the transmitter PGA or receiver PGA directly to meet the required output power level, respectively. In this paper, we aim to design a high-linearity wide-range PGA; the RXPGA provides over 64 dB gain range with 1 dB steps, and the gain is controlled by a 6-bit digital signal with a total of 64 steps. The DCOC circuit is used to remove DC offsets introduced from the RXPGA and the former circuits. And the TXPGA provides a 16 dB gain range, which is controlled by a 4-bit digital signal. In order to achieve consistent power control, the power gain must be monotonically changed with the control signal.

2. Architecture and circuit implementation

In this section, design considerations for the PGA and DCOC at system level as well as circuit level are described.

2.1. System design

Considering that the RXPGA is located at the end of the receiver, the linearity is dominated by the last stage of cascade amplifiers, thus, a high-linearity RXPGA should be employed. The RXPGA-DCOC architecture is depicted in Fig. 2. Since it is highly difficult to use a single PGA to realize a very wide dynamic range of gain tuning, we propose to utilize three stages of individual PGAs to attain the required 64 dB range and decibel linearity. Basically, the gain requirement is not difficult to achieve. However, the difficulties are the low-power and highly linearity. It is clear that the input-referred third-order intercept (IIP3) and noise figure (NF) constrain the gain distribution of the RXPGA chain. As can be seen in Fig. 2, to accomplish a wide range RXPGA, the first stage is a fixed-gain amplifier which serves as coarse-gain amplifier for the RXPGA chain. The fixed gain is 23 dB. And the second stage has two gains of 10 dB and 23 dB, which also serve as a coarse-gain amplifier for the RXPGA chain. On the other hand, a PGA with a total gain of 20 dB is used at the RXPGA chain to provide a fine-gain control of 1 dB per step, which varies from 3 to 20 dB.

The gain control is realized with switches that selectively turn on and off via the control signal. The switches K1–K6 are coarse gain switches. The gain control signal is provided by the

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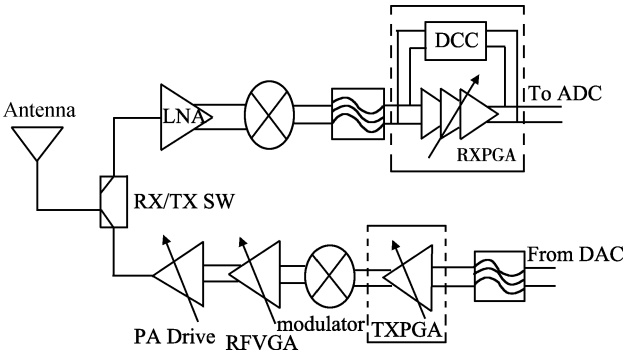

Fig. 1. Architecture of the WLAN transceiver.

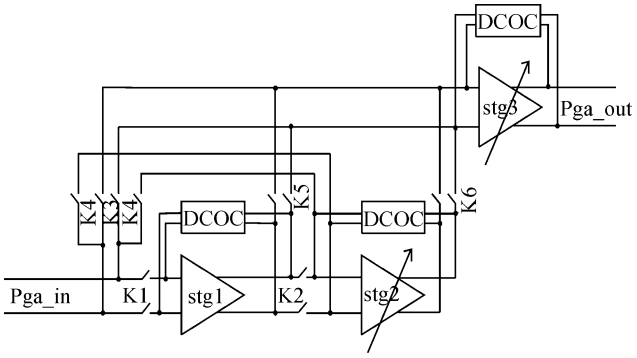

Fig. 2. RXPGA-DCOC architecture.

Table 1. RXPGA gain distribution.

Gain (dB)	Gain stage distribution
3–20	Stg3 (3 dB, 4 dB, …, 20 dB)
21–25	Stg2 (10 dB) + stg3 (11 dB, …, 15 dB)
26–35	Stg1 (23 dB) + stg3 (3 dB, …, 12 dB)
36–53	Stg1 (23 dB) + stg2 (10 dB) + stg3 (3 dB, …, 20 dB)
54–66	Stg1 (23 dB) + stg2 (23 dB) + stg3 (8 dB, …, 20 dB)

digital baseband. The gain distribution for the RXPGA can be seen in Table 1. It is chosen mainly to enhance the total noise performance of the RXPGA. It is clear that a large gain in the first stage will reduce the noise figure of the whole RXPGA. Multiple stages require a greater supply current, and the bandwidth, noise and linearity degrade at the output of each stage as more stages are cascaded. Reducing the number of stages may relax the requirement of the bandwidth, but this increases the gain of each stage. In this case, the design trade-off between gain-bandwidth product (GBW) of the amplifier, linearity, as well as power consumption of the whole amplifier chain, need to be carefully considered. Additionally, a multiple-stage amplifier introduces another problem: DC-offset cancellation. In this paper, we use three DCOC loops in each PGA stage, which prevents the DC offset from propagating in the amplifier chain.

The TXPGA gain varies from –5 to 10 dB with a 1 dB step, which is after the TX-filter of the transceiver, so that the demand of the TXPGA IIP3 is not too high. We use one stage of fine-gain amplifier to achieve 16 dB gain variation.

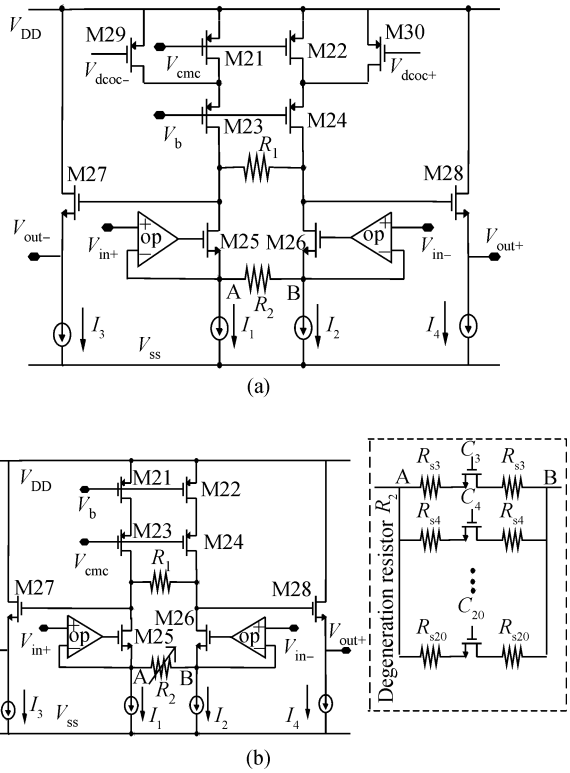

Fig. 3. Amplifier of the PGA. (a) Coarse-gain amplifier. (b) Fine-gain amplifier.

2.2. PGA and DCOC circuits design

2.2.1. PGA circuit design

The schematics of the amplifier in the RXPGA and TXPGA are depicted in Fig. 3. Figure 3(a) is the fixed gain amplifier, which serves as coarse-gain amplifier. It uses an open-loop structure[1], which consists of a V–I converter (input op-amps, M25/M26, and R_2) and a resistive load (R_1). M25 and M26 operate in source follower configuration: the differential input voltage $V_{\rm in} = V_{\rm in+} - V_{\rm in-}$ is copied over the series impedance of the two nonlinear transconductance $g_{\rm m1}$ (of M25/M26) and the linear degeneration resistor R_2. The $g_{\rm m1}$ linearity is improved by the closed-loop structure, including the input op-amps, which uses single differential pairs for high gain and low noise level. A source follower buffer is added to the output of the core amplifier to improve the driving capability and isolate the core amplifier from the loading. The buffer is implemented with M27/M28 in the schematic. To stabilize the output DC bias voltage, a common mode feedback (CMFB) amplifier is designed. By sensing the common mode voltage of the PGA output, the bias voltage $V_{\rm cmc}$ is generated.

The voltage gain of this amplifier can be approximated as

$$G = \frac{R_1}{R_2 + \dfrac{1}{g_{\rm m1}\,(1 + A_0)}} \frac{A_0}{1 + A_0} \cong \frac{R_1}{R_2}, \qquad (1)$$

where $g_{\rm m1}$ is the M25/M26 transconductance while A_0 is the input op-amp DC-gain. The PGA gain is adjusted by a digital control, which changes the values of R_1 and R_2. Changing R_2 corresponds to change DC-gain, NF and IIP3 at the same time.

This concept is exploited as follows. For large input signals, the DC-gain has to be low, which results in reduced noise requirements but a large input linearity requirement. On the other hand, for small input signals, the DC-gain has to be large, and the PGA has to exhibit low-noise and low input linearity. The PGA frequency response presents a single pole at the frequency $f_p = 1/2\pi R_1 C_{out}$, where C_{out} is the capacitive load, which is affected by R_1 changes. If the resistor R_1 does not change, accordingly the f_p value remains constant.

Basically the fine-gain amplifier (as shown in Fig. 3(b)) is similar to the coarse-gain amplifier, but its gain needs to cover from 3 to 20 dB. The gain of the fine-gain amplifier is made variable by varying the degeneration resistor R_2. The gain of the fine-gain amplifier is controlled by the fine-gain control signals. The MOS transistors are used to switch the resistors, thus, large sizes should be used to assure that the switch on-state resistance is much smaller than the switched resistors so that the designed gain is not influenced when switching.

The TXPGA has one stage of amplifier that is after the TX-filter. The amplifier uses the same configuration with the fine-gain amplifier of the RXPGA. Using 4 control bits, the TXPGA attenuates the input signal from DAC by –5 to 10 dB with a total of 16 steps.

2.2.2. DCOC circuit design

In order to solve the DC offset problem, the AC-coupling method may be regarded as an intuitive solution, and it requires a huge capacitor area and accompanies unavoidable in-band loss. In Ref. [2], a DC offset method is based on AC-coupling, and a differential voltage current conveyor with non-unity voltage and current gain factors is used to realize a large-value floating capacitor.

The second method for removing the DC offset, that is feed-forward[3], which needs the identical amplifier with the main op of the PGA and the high value of resistor, is realized by the channel resistance of the MOS setting on the sub-threshold region. The channel resistance of the MOS is seriously varied by temperature and process variation, which need a calibration circuit. The above two methods only can remove the offset voltage before the input of the circuit, and these methods will be invalid about the imbalanced of the circuits themselves.

The third DC offset method is a digital correction technique to remove the DC offset voltage. The DC offset is reduced by digital code without signal loss[4]. However, the system tends to be complicated and consumes much power.

Another method for removing the DC offset is continuous time feedback, as shown in Ref. [5], which can continuously remove the offset voltage. The output voltage is sensed by a RC filter and cancelled via a feedback loop with an amplifier. Continuous time feedback is adopted to realize a high-pass characteristic. The proposed approach is realization of a large-value capacitor or resistor to implement a high-pass filter with a low cutoff frequency, which is costly for huge chip size. To minimize the chip size, a larger resistor or capacitor should be implemented outside the die. Using the external components needs the additional pin and increases the application dimensions. To make matter worse, the HPCF of DC feedback is varied with the gain of the amplifier. The higher the gain, the larger the HPCF.

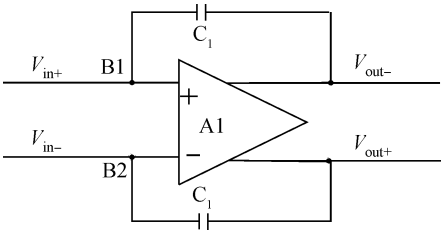

Fig. 4. The Miller effect.

To solve the above problems, we propose a DC offset cancellation circuit. The method is based on the continuous time feedback technique. At the same time, the Miller effect is used to realize a large value floating capacitor. The proposed approach is the realization of a large-value floating capacitor to implement a high-pass filter with a low cutoff frequency.

As shown in Fig. 1, the transfer function[6] of the closed-loop in the RX baseband is expressed as

$$H(s) = \frac{A}{1 + A\dfrac{\beta_0}{1 + s/\omega_0}} = \frac{A\,(s + \omega_0)}{s + (1 + A\beta_0)\,\omega_0}, \quad (2)$$

where A represents the gain of the RXPGA, and β_0 , ω_0 denote the DC gain and 3-dB bandwidth of the DC offset cancellation circuit, respectively. Therefore, the HPCF of the closed-loop path can be calculated by

$$f_c = f_0\,(1 + A\beta_0)\,. \quad (3)$$

When $A\beta_0 \gg 1$,

$$f_c \approx f_0 A\beta_0. \quad (4)$$

Considering that the DC offsets can corrupt the desired signal, therefore, the system requires a lower f_c, so that f_0 must be small enough. The DCOC cutoff-frequency is

$$f_0 = \frac{1}{2\pi RC}. \quad (5)$$

In order to obtain a lower f_0, the resistance R or capacitance C must be increased. A larger RC will occupy a huger area, which is disadvantageous for integration. Therefore, in this paper, the Miller effect[2] is used to increase the value of capacitance C, and its schematic diagram is shown in Fig. 4.

From Fig. 4, the equivalent capacitance of the B_1, B_2 can be determined as

$$C = (1 + A_v)\,C_1 \approx A_v C_1, \quad (6)$$

where A_v is the gain of amplifier A1 and $A_v \gg 1$. Figure 5 is the DC-coupled DC offset canceller using the Miller effect. A1 is the Miller amplifier, and A2 is the feedback amplifier. The PGA output DC offset voltage at low frequency is detected and stored in an equivalent capacitance $A_v C_1$. This voltage induces the offset correction current, which has opposite phase with the offset current in the PGA core. A2 injects this offset correction current back to the PGA core to nullify the DC offset current. For example, the capacitance C_1 is 5 pF and the gain of the A1 is 80 dB; using the Miller effect, the overall capacitance can

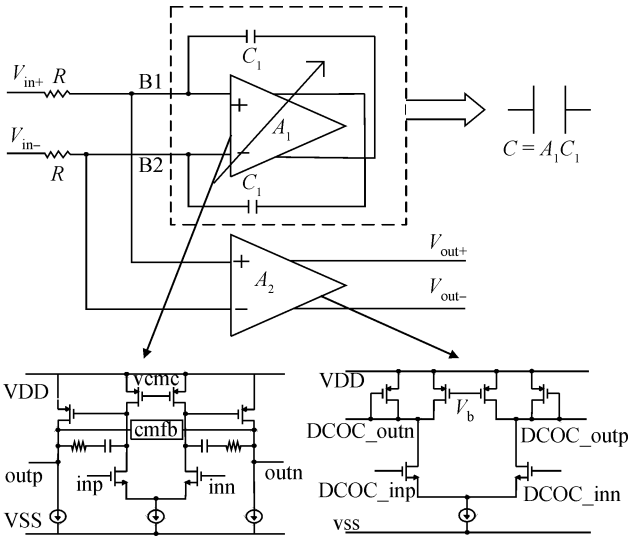

Fig. 5. DC-coupled canceller using the Miller effect.

Table 2. Parameter values using multi-amplifier.

f_c (kHz)	f_0 (kHz)	C (nF)	A_v (dB)	C_1 (pF)
1	0.01	53	80	5.3
10	0.1	5.3	60	5.3
100	1	0.53	40	5.3
1000	10	0.053	20	5.3

be up to 5 × 10000 pF, which is equivalent to 10000 times the capacitance expanded.

Although using the Miller effect can obtain a lower HPCF, the DCOC settling time is longer. Therefore, we need a higher HPCF to reduce the DCOC settling time. So, we use multi-HPF to achieve the requirement of lower HPCF and shorter DCOC settling time. In other words, we need different values of f_0 to achieve different values of f_c.

Based on the Miller effect, the multi-HPCF is also shown in Fig. 5. The amplifier A_1 has different voltage gain S to realize different HPCF. The calculated parameter values are shown in Table 2. Obviously, if $A_v = 80$ dB, $R = 300$ kΩ, $A\beta_0 = 40$ dB, C_1 = 5.3 pF, the closed-loop path cutoff frequency will be up to 1 kHz. However, if A_v = 20 dB, and the other parameters have the same values, the loop cutoff frequency will show 1 MHz. The operation of the DC offset canceller in Fig. 5 can be explained as follows. When the PGA is in operation state, amplifier A_1 reaches high gain, which is used to realize a large value floating capacitor, the PGA can achieve 1 kHz cutoff frequency, which does not corrupt the useful signal in the DCR. When the gain of the PGA is changing, with the state of the amplifier A_1 getting low gain, and the PGA obtained 1 MHz high pass cutoff frequency, which can satisfy the DCOC settling time requirement.

For these Miller effect realization amplifiers, how to design it would be reasonable? We analyze the closed-loop DC offset method as follows.

From Eq. (2), we can see that when

$$\left|\frac{A\beta_0}{1+s/\omega_0}\right| \gg 1,$$

the transfer function $H(s)$ can be approximated as A, which demands

$$|1+s/\omega_0| \gg A\beta_0,$$

and thus

$$\begin{aligned}1+\frac{s}{\omega_0} &= 1+\mathrm{j}\frac{\omega}{\omega_0} = 1+\mathrm{j}\frac{f}{f_0}\\ &= 1+\mathrm{j}\frac{f}{\frac{1}{2\pi RC}} = 1+\mathrm{j}2\pi RCf\\ &= 1+\mathrm{j}2\pi RA_mC_1f, \end{aligned} \tag{7}$$

where A_m is the gain of the Miller effect amplifier. If the Miller effect realization amplifier has one pole, which can be written as

$$A_m = \frac{A_0'}{1+\mathrm{j}\frac{f}{f_0'}}, \tag{8}$$

where A_0' is the DC gain of the Miller effect amplifier, AND f_0' is the miller op-amps cutoff frequency.

Substitution of Eq. (8) in Eq. (7) gives

$$\begin{aligned}1+\mathrm{j}2\pi RA_mC_1f &= 1+\mathrm{j}2\pi R\frac{A_0'}{1+\mathrm{j}\frac{f}{f_0'}}C_1f\\ &= 1+\mathrm{j}2\pi RC_1A_0'\frac{f}{1+\mathrm{j}\frac{f}{f_0'}}. \end{aligned} \tag{9}$$

If we want

$$|1+s/\omega_0| \gg A\beta_0,$$

Equation (9) must fulfill

$$\left|1+\mathrm{j}2\pi RC_1A_0'\frac{f}{1+\mathrm{j}\frac{f}{f_0'}}\right| \gg A\beta_0, \tag{10}$$

and we have

$$2\pi RC_1A_0'\frac{f}{\sqrt{1+\left(\frac{f}{f_0'}\right)^2}} > \alpha A\beta_0,$$

where $\alpha \approx \frac{|1+s/\omega_0|}{A\beta_0}$, and thus

$$\frac{\omega}{\omega_0}\frac{1}{\sqrt{1+\left(\frac{f}{f_0'}\right)^2}} > \alpha A\beta_0, \tag{11}$$

where $\omega = 2\pi f$, $\omega_0 = \frac{1}{A_0'RC_1}$.

Substitution of $\omega_c = A\beta_0\omega_0$ in Eq. (11) gives

$$\frac{\omega}{\omega_c}\frac{1}{\sqrt{1+\left(\frac{f}{f_0'}\right)^2}} > \alpha, \tag{12}$$

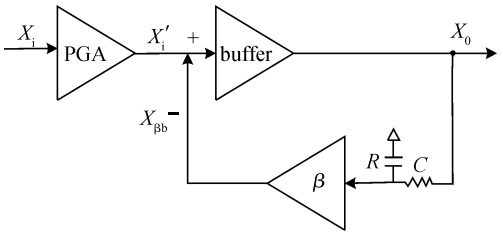

Fig. 6. Block diagram of the PGA with the DC offset canceller.

$$\left(\frac{\omega}{\alpha\omega_c}\right)^2 > 1 + \left(\frac{f}{f_0'}\right)^2,$$

$$f_0' > \frac{f}{\sqrt{\left(\frac{\omega}{\alpha\omega_c}\right)^2 - 1}}. \tag{13}$$

From Eq. (13), when

$$\left(\frac{f}{\alpha f_c}\right)^2 \gg 1, \tag{14}$$

$$f_0' > \frac{f}{\sqrt{\left(\frac{f}{\alpha f_c}\right)^2 - 1}} \approx \frac{f}{\frac{f}{\alpha f_c}} = \alpha f_c,$$

$$f_0' > \alpha f_c. \tag{15}$$

So, as for lower cutoff frequency f_c, we must design a suitable Miller effect realization amplifier Am to satisfy Eq. (15). When the cutoff frequency f_c is large enough, even Equation (14) cannot be satisfied, and the relation of $f_0' > \alpha f_c$ is still regarded as the guideline for our design.

Considering the continuous-time feedback DC offset canceller, the HPCF of the DC feedback is varied with the gain of the amplifier. In order to overcome the disadvantage of a higher gain with a higher HPCF, the proposed dc offset feedback loop with the PGA is shown in Fig. 6.

In Fig. 6, X_i and X_o are the input and output signal, respectively. The feedback network has a transfer function β and feeds back a signal $X_{\beta b}$ to the buffer input. From Fig. 6,

$$AX_i - \beta X_0 = X_0, \tag{16}$$

where A is the gain of the PGA, if the feedback amplifier β has one pole, and thus

$$\frac{X_0}{X_i} = \frac{A}{1+\beta} = \frac{A}{1 + \frac{\beta_0}{1 + s/\omega_0}}. \tag{17}$$

If $s \to 0$, $\beta_0 \gg 1$, Equation (17) simplifies to

$$\frac{X_0}{X_i} = \frac{A}{\beta_0}. \tag{18}$$

So the DC attenuation can be expressed as

$$\frac{A}{A\beta_0} = \beta_0. \tag{19}$$

Equation (19) indicates that the DC attenuation is constant regardless of the PGA with different voltage gain, and thus the HPCF of the DC feedback loop is constant with gain variation, which can be seen in Fig. 7.

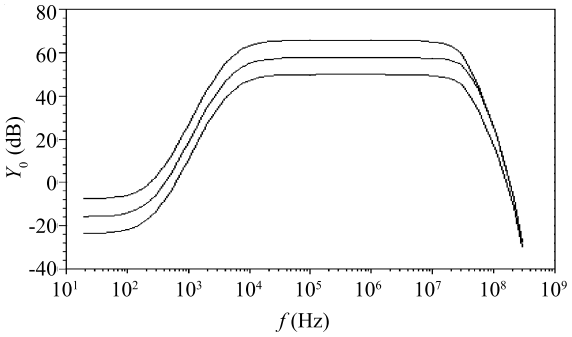

Fig. 7. DC attenuation at different gain settings.

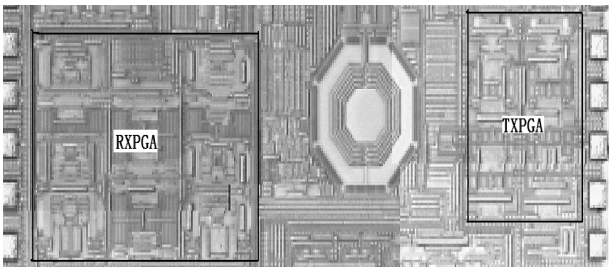

Fig. 8. Micrograph of the RXPGA and TXPGA.

Table 3. Summary of the baseband PGA.

Parameter		Value
Technology		0.13 μm CMOS
Supply voltage		3.3 V
RXPGA	dB-linear gain range	3–66 dB
	BW 3 dB	$\geqslant$ 20 MHz
	IIP3/34 dB	–12 dBm
	NF/34 dB	28 dB
	AGC settling time	0.2 μs
	DCOC settling time (32 dB/step)	$\leqslant$ 0.45 μs
	DCOC HPCF	10 kHz/1 MHz
	I_{total} (I and Q path)	18 mA
	Miller op current	1 mA/single
TXPGA	dB-linear gain range	–5 to 10 dB
	IIP3/3 dB	20 dBm
	NF/3 dB	27 dB
	I_{total} (I and Q path)	7 mA

3. Measurement results

Figure 8 shows a micrograph of the baseband RFIC, which is implemented in TSMC 0.13 μm CMOS technology with a supply voltage V_{DD} = 3.3 V. Table 3 gives a summary of the baseband PGA. Figure 9 shows the measurement results of the RXPGA and TXPGA. The RXPGA covers a 64 dB gain range in 1 dB steps with a total of 64 steps, and the TXPGA provides a 16 dB gain range in a 1 dB step with a total of 16 steps.

The PGA noise figure measurement result can be seen in Fig. 10. From equation NF = 174 dBm/Hz – Pin – 10lgRBW – SNR, we can calculate the noise figure as 28 dB at a 34 dB gain setting. Figure 11 is the frequency response when the PGA gain is 34 dB. The DCOC settling time of the proposed method is shown in Fig. 12. As can be seen in Fig. 12, the PGA gain

Table 4. PGA performance comparison.

	This work	Ref. [7]	Ref. [8]	Ref. [9]	Ref. [10]
Technology (μm)	0.13	0.18	0.18	0.13	0.18
V_{dd} (V)	3.3	1.5	1.8	1.5	1.8
I (mA)*	4.5	2.1	3.5	5.2	6.5
Gain range (dB)	3–66	–21 to 21	12–108	–32 to 52	–15 to 60
Gain error (dB)	±0.2	±0.54	—	±1	0.3
Gain step (dB)	1	1.31	6	—	2.5
BW3dB (MHz)	20	60	300	200	140
IIP3 (dBm) / gain (dB)	–45 to 20	–11.5 to 14	–5/12	–37 to 13	14.4
NF (dB) / gain (dB)	18/66	15/21	23.8/ 108	6.2/52	12.5/60
Year (Ref.)	—	09	08	08	07

*only one path (I or Q) and only the PGA current.

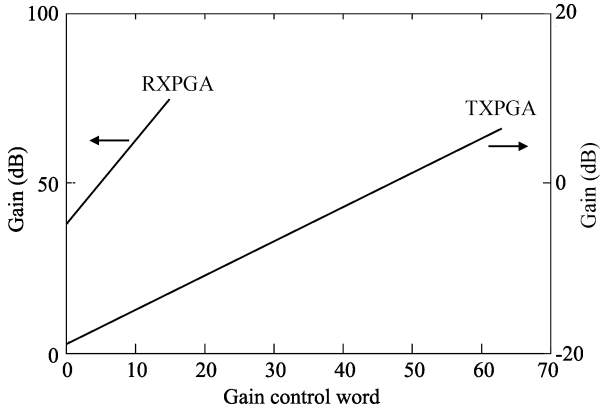

Fig. 9. Measured gain versus control signal of the RXPGA and TXPGA.

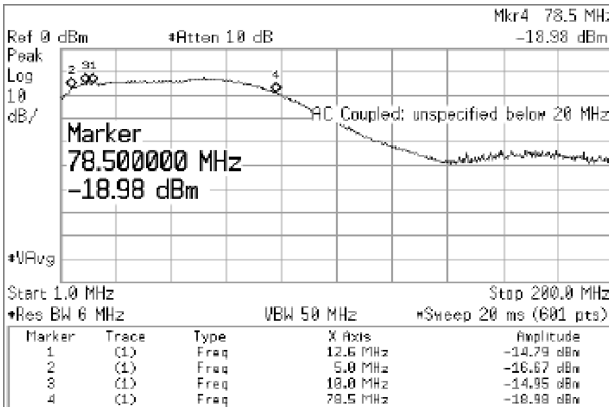

Fig. 11. The measured frequency response of the PGA.

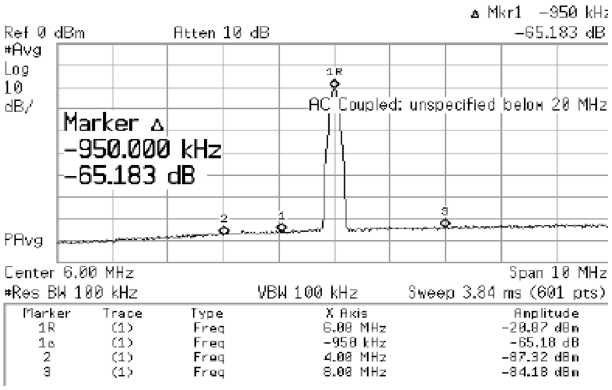

Fig. 10. PGA noise figure measurement result.

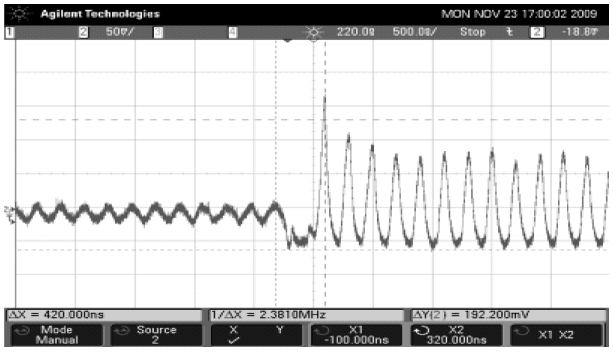

Fig. 12. The measured DCOC settling time with the gain varies 32 dB.

varies from 3 to 34 dB, and the settling time is less than 0.45 μs. From Table 3, we can see the DCOC circuit in order that lower HPCF consumes higher current compared with Ref. [5].

The PGA performance is compared with Refs. [7–10], as shown in Table 4. The proposed PGA achieves the best performance in terms of high linearity with a low power.

4. Conclusion

This paper has presented a low power high linearity baseband PGA for a direct-conversion WLAN transceiver. The receiver baseband PGA consumes 18 mA and the transmitter baseband consumes 7 mA (I and Q path) under a 3.3 V supply. By adopting the closed-loop structure to enhance the linearity, the IIP3 is –12 dBm at a 34 dB gain setting. Moreover, the DC offset canceller uses the Miller effect to realize a large capacitance. For example, passive HPF with a 300 Hz cutoff frequency requires a 1.78 nF capacitor and a 300 kΩ resistor. Such a capacitor consumes too much area. However, by using the proposed method, only a 5 pF capacitor is needed, then the required capacitance is reduced to 1/356. Since there is no need for large capacitance, the chip area is small and suitable for IC integration.

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