Spacing optimization of high power LED arrays for solid state lighting

Y. Sing Chan and S. W. Ricky Lee†

Electronic Packaging Laboratory, Center for Advanced Microsystems Packaging, Hong Kong University of Science and Technology, Hong Kong, China

Abstract: This paper provides an analytical approach to determine the optimum pitch by utilizing a thermal resistance network, under the assumption of constant luminous efficiency. This work allows an LED array design which is mounted on a printed circuit board (PCB) attached with a heat sink subject to the natural convection cooling. Being validated by finite element (FE) models, the current approach can be shown as an effective method for the determination of optimal component spacing in an LED array assembly for SSL.

Key words: high power LED; thermal resistance network; finite element modeling
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1. Introduction

The use of high power light emitting diode (LED) for solid state lighting (SSL) has become a tangible reality. Nevertheless, there still exist quite a number of technical issues to be addressed in practice. One major issue encountered in this field comes with the decision in the spacing (pitch) between LEDs for optimum cost, optical and thermal performance. Utilization of high power LED usually accounts for a major portion in the cost for manufacturing a lighting system. The number of components employed thus directly affects the selling price of the product. There exists a trade-off between cost and the system performance, and there requires an optimum spacing to achieve the compliance.

There are few literatures focusing on the design of an LED array. Rather, more discussion can be found regarding thermal management[1, 2]. Petroski[3] has studied numerically the effect of pitch, dielectric layer thickness, copper layer thickness and the boundary condition temperature on the thermal performance of a LED array which is mounted on a metal-cored PCB. By using a design of experiments methodology, he is capable to formulate the relative significance of the parameters on the maximum temperature of the array. Christensen and Graham[4] have developed numerical model and thermal resistance network to study the effect of pitch, power level, cooling method, package material and architecture on the thermal performance of a LED array which is mounted on an aluminum heat spreader. They have also utilized a degradation model to evaluate the optical performance of the array as a result of power and thermal concentration.

This paper devotes to the design of a array such that its desired optical performance (luminous flux) can be preserved. In addition, the luminous efficiency is accounted such that a more realistic thermal analysis can be achieved. The present study is divided into three parts. The first part derives a thermal resistance network for an LED array which is mounted on an organic or metal-cored PCB attached with a heat sink subject to the natural convection cooling. The second part outlines the procedures for the determination of an optimum pitch. In the last part the methodology is demonstrated for an LED tube design for the drop-in replacement of a 4ft T8 fluorescent lamp. The thermal results predicted by using the network are compared with those obtained by FE models for validation.

2. Thermal analysis

Assuming the desired luminous flux is uniformly borne by the array of LEDs such that the thermal loading of each device is identical, the thermal analysis of the array can then be simplified into a unit cell analysis. Figure 1 depicts an array with a pitch equal to $a[m]$ and Figure 2 shows a thermal analysis of the corresponding unit cell. The unit cell may be divided into three sections: the LED section, the LED footprint section and the heat spreading section. Assuming there is no heat being transferred through the top of the LED such that all of the heat generated is conducted into the footprint section[4], there remain two pathways for heat dissipation. The first one, a shorter one, is all the way through the PCB, thermal interface material (TIM) and the heat sink to the bottom surface of the footprint section by conduction and then to the ambient by convection.

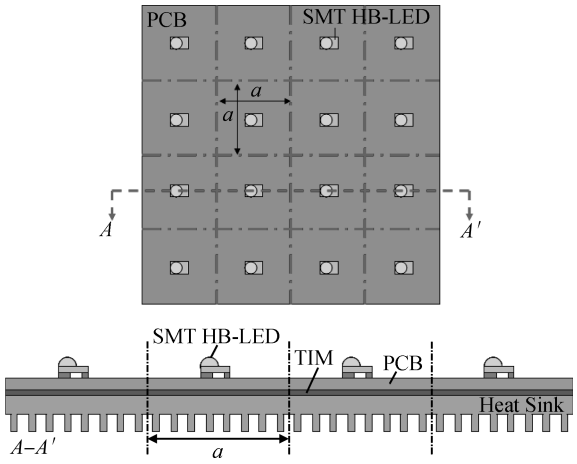

Fig. 1. An array of LEDs with pitch a.

† Corresponding author. Email: rickylee@ust.hk
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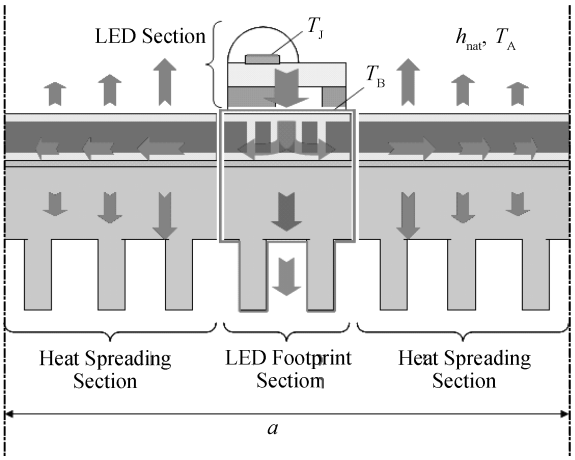

Fig. 2. Heat flow in a unit cell.

The second path works as a fin mechanism. Heat is first conducted laterally into the PCB of the spreading section. As the thermal energy goes along the PCB, some potions are being conducted to the surfaces of the spreading section and carried away to the ambient by convection. The arrows in Fig. 2 help to illustrate this heat flow analysis.

The thermal resistance within the footprint section is negligible for metal-cored PCB. In case of organic PCB, the corresponding thermal resistance could be reduced to < 1 K/W with the use of thermal vias. For such a small value, the thermal resistance of the footprint section could be neglected. As a result, we may assume the entire footprint section bears a uniform temperature T_B [K] from the design point of view. The junction temperature on the LED chip T_J [K] thus depends on: (1) thermal resistance R_{JB} [K/W], as heat flows through the LED and the bonding material to the footprint section; (2) thermal resistance $R_{BA,FP}$ [K/W], as heat being convected to the ambient through the bottom surface of the footprint section and; (3) thermal resistance $R_{BA,HS}$ [K/W], as heat being conducted through the PCB and simultaneously convected to the ambient through the surfaces of the spreading section. R_{JB} is known since the thermal resistance of the LED is given by the supplier and the thermal resistance of the bonding material can be estimated using a simple conduction thermal resistance equation[5]:

$$R_{cond} = \frac{L_{cond}}{k_{cond} A_{cond}}, \tag{1}$$

where R_{cond} [K/W] is the conduction thermal resistance, L_{cond} [m] is the thickness of the bonding material, k_{cond} [W/(m·K)] is the corresponding thermal conductivity and A_{cond} [m^2] is the cross-sectional area heat passing through. $R_{BA,FP}$ can be estimated by using a convection thermal resistance equation[5]:

$$R_{conv} = \frac{1}{h_{conv} A_{conv}}, \tag{2}$$

where R_{conv} [K/W] is the convection thermal resistance, h_{conv} [W/(m^2·K)] is the convection coefficient and A_{conv} [m^2] is the surface area for convection heat transfer. The difficulty remains on the determination of $R_{BA,HS}$, which is discussed in detail in the coming session. The heat flow of the present thermal analysis can be represented by a simple thermal resistance network, as depicted in Fig. 3.

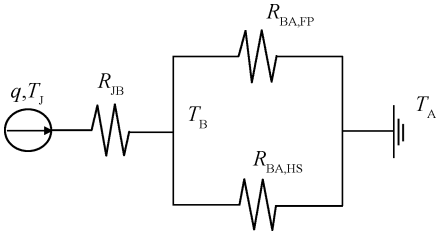

Fig. 3. Thermal network for thermal analysis.

$R_{BA,HS}$ can be estimated using a circular fin model[6, 7] after three transformations. The first transformation requires the calculation of a mean convective coefficient $\overline{h}$ [W/(m^2·K)], assuming the internal resistance of the heat sink is negligible. Let h_{nat} [W/(m^2·K)] be the natural convection coefficient over both the PCB surface and the heat sink surface. If β [ND] represents the ratio between the active surface area of the heat sink and the bottom PCB surface area, βh_{nat} becomes the effective convective coefficient at the bottom PCB surface. $\overline{h}$ can then be calculated as:

$$\overline{h} = \frac{h_{nat} + \beta h_{nat}}{2} = \frac{h_{nat}(1+\beta)}{2}. \tag{3}$$

The second transformation converts the square unit cell into a circular one with radius r_2 [m], by preserving the unit cell surface area[6]. The unit cell surface area equals a^2. Therefore, r_2 can be found as:

$$r_2 = \sqrt{a^2/\pi}. \tag{4}$$

The last transformation requires the determination of an effective fin thickness t_{fin} [m]. When there is a heat sink attachment, t_{fin} is approximately the thickness of the base of the heat sink. If there is no heat sink attached, t_{fin} is about the total thickness of the metallic potion of the PCB for heat spreading and dissipation. The above definitions assume critically low thermal conductivity of the dielectric and TIM layers [typically < 1 W/(m·K)] such that they provide no help for heat spreading in the fin. In addition, these definitions assume negligibly thermal resistances of the dielectric and TIM layers, which become valid under the natural cooling conditions. When metal-cored PCB is in use, t_{fin} is about the thickness of the board. In case of organic PCB, t_{fin} is the total thickness of the continuous copper layers[8]. Assuming the thickness of each copper layer is t_{cu} [m] and the number of copper layers is n_{cu} [ND], t_{fin} for organic PCB can be calculated as:

$$t_{fin} = t_{cu} n_{cu}. \tag{5}$$

After the three transformations, the spreading section eventually becomes a circular fin and hence the circular fin model applies:

$$R_{\mathrm{BA,HS}} = \Psi \frac{I_0(\alpha r_1) K_1(\alpha r_2) + K_0(\alpha r_1) I_1(\alpha r_2)}{K_1(\alpha r_1) I_1(\alpha r_2) - I_1(\alpha r_1) K_1(\alpha r_2)},$$
$$\Psi = \frac{1}{k_{\mathrm{fin}}(2\pi r_1 t_{\mathrm{fin}})\alpha},$$
$$\alpha = \sqrt{\frac{2\overline{h}}{k_{\mathrm{fin}} t_{\mathrm{fin}}}}, \tag{6}$$

where I [ND] and K [ND] are modified Bessel functions and their subscripts represent the order of the functions, k_{fin} [W/(m·K)] is the thermal conductivity of the fin material and r_1 [m] is the effective radius of the footprint section. For aluminum-cored PCB, k_{fin} is the thermal conductivity of aluminum k_{al} [W/(m·K)] which is about 180 W/(m·K). In case of organic PCB, k_{fin} is the thermal conductivity of copper k_{cu} [W/(m·K)] which is about 390 W/(m·K). For the situation the footprint section is non-circular, r_1 can be determined in the same way as r_2 by area preservation, as demonstrated by Eq. (4).

3. Spacing optimization

For a required luminous flux F [lm] to be emitted from a confined area A [m^2], an array may be designed using different kind of LEDs (in terms of efficacy and lumen output) with different number adopted. Assuming the array is uniformly distributed over A with identical LEDs, a larger pitch (hence smaller number of LEDs) requires each of them to deliver more lumen output and hence bear a larger thermal loading. On the contrary, smaller pitch (hence larger number of LEDs) adoption reduces both optical and thermal loading of each device. Since there are emission range and maximum allowed temperature for LEDs, there forms a design space regarding the thermal performance and the pitch or eventually the cost of the system. In the following sections the procedures for the determination of this design space are outlined. Using the design space, the optimized configurations like the lowest cost design or the highest thermal performance can be justified.

3.1. Optical bounds for pitch

Assuming f [lm] is the lumen output of each LED and n [ND] is the number of LED used, in order to satisfy the functionality of the array, it requires:

$$f = F/n. \tag{7}$$

On the other hand, n is related to a by:

$$n = A/a^2. \tag{8}$$

Combining Eqs. (7) and (8), a can be found as:

$$a = \sqrt{Af/F}. \tag{9}$$

If $f_{\max}$ [lm] and $f_{\min}$ [lm] are respectively the maximum and minimum lumen output of each LED, the optical bounds for the pitch are:

$$\begin{cases} a_{\mathrm{F,max}} = \sqrt{\dfrac{Af_{\max}}{F}}, \\ a_{\mathrm{F,min}} = \sqrt{\dfrac{Af_{\min}}{F}}. \end{cases} \tag{10}$$

3.2. Thermal bounds for pitch

T_{J} depends on the overall thermal resistance of the unit cell R_{JA} [K/W], the heat generation of each LED q [W] and the ambient temperature T_{A} [K], as illustrated in Fig. 3:

$$T_{\mathrm{J}} = \left(R_{\mathrm{JB}} + \frac{R_{\mathrm{BA,FP}} R_{\mathrm{BA,HS}}}{R_{\mathrm{BA,FP}} + R_{\mathrm{BA,HS}}}\right) q + T_{\mathrm{A}}$$
$$= R_{\mathrm{JA}} q + T_{\mathrm{A}}. \tag{11}$$

If heat is the only form of energy remains after luminous emission, q becomes dependent only on f, the luminous efficacy η_{f} [lm/W] and the luminous efficiency η_{l} [ND]:

$$q = (1 - \eta_{\mathrm{l}}) \frac{f}{\eta_{\mathrm{f}}}. \tag{12}$$

Assuming the maximum η_f for white LED is 300 lm/W at which all of the energy input is converted to white light[9], η_{l} and η_{f} can be correlated as:

$$\eta_{\mathrm{l}} = \frac{\eta_{\mathrm{f}}}{300}. \tag{13}$$

Combining Eqs. (7), (8), and (11–13), T_{J} can be evaluated in terms of R_{JA}, T_{A}, F, A, η_{f} and a:

$$T_{\mathrm{J}} = R_{\mathrm{JA}} \left(1 - \frac{\eta_{\mathrm{f}}}{300}\right) \left(\frac{Fa^2}{\eta_{\mathrm{f}} A}\right) + T_{\mathrm{A}}. \tag{14}$$

Equation (14) can be rewritten as:

$$T_{\mathrm{J}} = K_{\mathrm{JA}} \eta_{\mathrm{q}} I + T_{\mathrm{A}}. \tag{15}$$

I [lm/m^2] is the luminous intensity required to be delivered by the array, which is a given criteria for the design practice. η_{q} [W/lm] is the heat generation coefficient of individual LEDs. For the kind of LED selected, $\eta_{\mathrm{q}} f$ tells the amount of heat generation for each LED at different lumen output levels. K_{JA} [m^{2}K/W] is the luminous-intensity-preserved thermal resistance, which determines the thermal performance of the array based on different I levels. It is clear that K_{JA} is the critical design parameter for the thermal performance of an LED array.

3.3. Practical design spacing

The practical design space falls within both the optical and thermal bounds, wherein the thermal performance of the array bears meaningful design value. Assuming m [US$] is the cost for each LED, the total cost of the array C [US$] can be correlated to a as:

$$C = mn = \frac{mA}{a^2}. \tag{16}$$

Using Eqs. (15) and (16) within the design space, optimum designs can be justified.

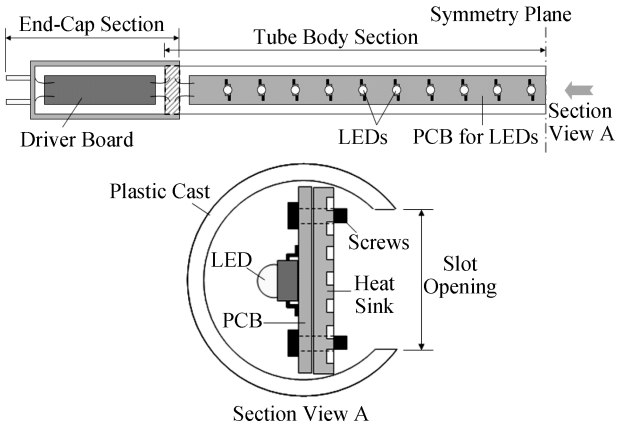

Fig. 4. Effect of a on K_{JA} for different β.

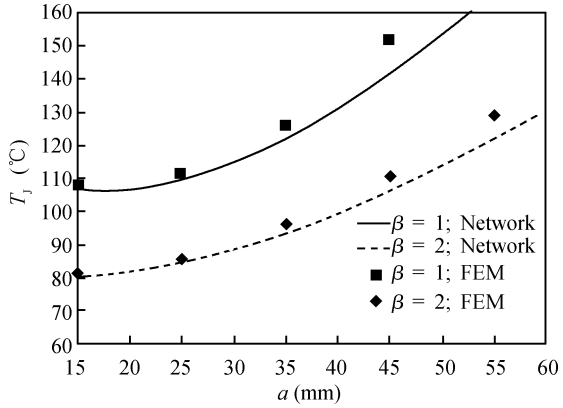

Fig. 5. T_J of the LED tube for different a and β.

3.4. Case study

Figure 4 shows a 4 ft T8 LED tube design which requires a LED array to serve the functioning. Assuming a certain kind of LED is selected and 1 mm organic PCB is to be used, the following specifications need to be satisfied:

F = 2800 lm, A = 30000 mm^2, T_A = 30 ℃, η_f = 70 lm/W, f_{max} = 165 lm, f_{min} = 30 lm, R_{JB} = 15 K/W, r_1 = 4 mm, t_{cu} = 0.035 mm, n_{cu} = 2, h_{nat} = 8 W/m^2·K, $T_{J,max}$ = 130 ℃, m = US$1.

Using Eq. (10), the optical bounds are ($a_{F,min}$, $a_{F,max}$) = (18 mm, 42 mm). T_J against a for β = 1 (no heat sink) and β = 2 (with heat sink) is plotted in Fig. 5, by Eq. (15). For β = 1, the thermal bounds are ($a_{T,min}$, $a_{T,max}$) = (18 mm, 39 mm). For β = 2, the thermal bounds become (15 mm, 59 mm). Hence, the practical design space is (18 mm, 39 mm) for β = 1 and (18 mm, 42 mm) for β = 2. It is shown that when the thermal performance of the LED array is poor, the optical bounds can not be fully utilized. When heat sink is employed to boost the heat dissipation capability of the system, the entire optical bounds become available for the array design. Incorporating Eq. (16), Figure 5 can be transformed to give the thermal performance-cost relation for the LED tube within the design space, as illustrated in Fig. 6. Two major observations are noted from the plot: (1) using more LEDs from the lowest cost design effectively improves the thermal performance of the array. Yet, the effectiveness drops with the further investment; (2) the effect

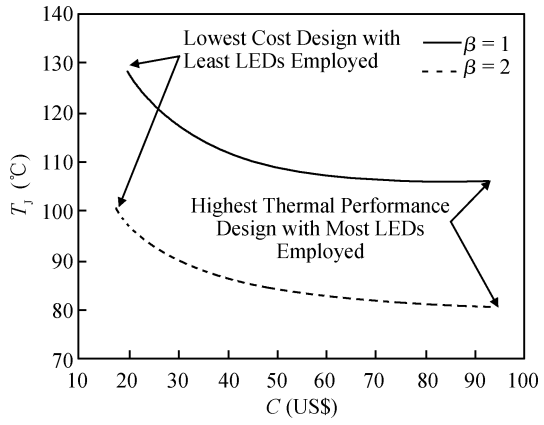

Fig. 6. Thermal performance-cost relationship of the LED tube for different β.

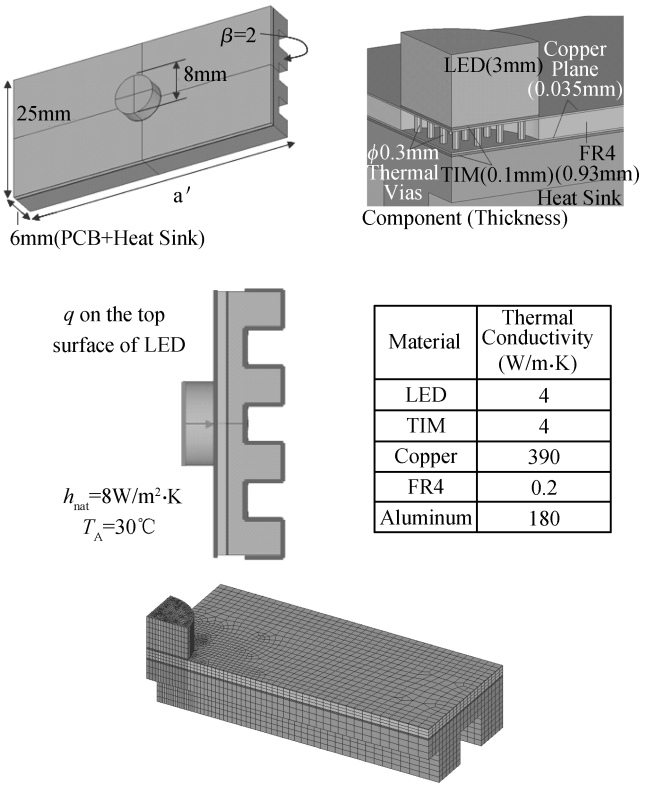

Fig. 7. Details of FE model.

of using more LEDs for thermal performance enhancement is independent of the heat sink design. Undoubtedly, the current optimization methodology allows flexibility the consideration of different kinds of LED, PCB designs and heat sink configurations, leading to a quick estimation for a cost effective thermal design of a LED array which satisfies the necessary luminous requirement.

Using the commercial code ANSYS®, FE models are developed to validate the thermal analysis performed by the thermal resistance network. For simplification, the unit cell is analyzed using a quarter model. The LED is lumped into a cylinder with its thermal resistance preserved by using an effective thermal conductivity. Ten thermal vias of 300 μm are employed to minimize the temperature difference within the footprint

section. TIM has to be used in practical situation, for which 100 μm TIM is assumed for the thermal connections between the LED and the PCB, as well as between the PCB and the heat sink. Since a single row of LEDs is assumed (one side of the unit cell is set to be 25 mm), a modified pitch a' [m] is required to characterize the separation between the LEDs by area preservation. Using element SOLID70, an eight-node 3-D element containing temperature as the only degree of freedom, five models with different a' are solved for the two β configurations. Details for the FE models are depicted in Fig. 7, where the modeling results are overlaid on Fig. 5. Good agreement is shown between the FE and network results, despite there is deviation and it increases with a.

There are two major reasons for the under-estimation of T_J from the network approach: (1) the internal thermal resistance of the footprint section is neglected from the derivation of the network approach. When a gets larger, power concentration becomes severe and so does the temperature difference within the footprint section. The omission of this effect in the network makes it under-estimated T_J; (2) the network model is developed using the circular fin model which assumes axisymmetric temperature distribution, this under-estimates the temperature non-uniformity induced by the growing rectangular unit cell as a increases.

4. Conclusions

An analytical and systematic methodology which allows a first order estimation for an optimum component spacing of a LED array assembly is developed in this study. The assembly concerned allows both organic or metal-cored PCB as the LED carriers. Different heat sink designs can be attached at the back of the PCB for natural cooling enhancement.

This methodology assumes the optical performance as a design criterion, rather than a design parameter. With the optical performance taken into consideration, it is found that the luminous-intensity-preserved thermal resistance K_{JA} being the critical design parameter which directly affects the thermal performance of the array. In addition to the geometric and material influences, the current study has accounted for the luminous efficiency, which delivers a more realistic thermal analysis. Having considered the optical and thermal tolerances of the LEDs, the present study has defined a practical design space for the component spacing optimization. The relationship between the thermal performance and the total cost of the array are correlated through the component spacing, which facilitates design optimization based on an added-on criterion.

The methology has been demonstrated through the design of a LED tube for the drop-in replacement of a 4 ft T8 fluorescent lamp. Being validated using finite element models, the method can be shown an effective and efficient one for determination of an optimized LED array design.

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