# A 270-MHz to 1.5-GHz CMOS PLL clock generator with reconfigurable multi-functions for FPGA*

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**Abstract:** A PLL clock generator with reconfigurable multi-functions for FPGA design applications is presented. This clock generator has two configurable operation modes to achieve clock multiplication and phase alignment functions, respectively. The output clock signal has advanced clock shift ability such that the phase shift and duty cycle are programmable. In order to further improve the accuracy of phase alignment and phase shift, a VCO design based on a novel quick start-up technique is proposed. A new delay partition method is also adopted to improve the speed of the post-scale counter, which is used to realize the programmable phase shift and duty cycle. A prototype chip implemented in a 0.13-$\mu$m CMOS process achieves a wide tuning range from 270 MHz to 1.5 GHz. The power consumption and the measured RMS jitter at 1 GHz are less than 18 mW and 9 ps, respectively. The settling time is approximately 2 $\mu$s.

**Key words:** PLL; clock generator; reconfigurable; VCO
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## 1. Introduction

Phase-locked loops (PLLs) for clock multiplication and phase alignment are widely used in high speed, large-scale field programmable gate arrays (FPGAs) as a key component responsible for the global clock distribution networks across the chip. In addition to those common needs such as high frequency output, wide frequency tuning range and low jitter, this type of application usually demands flexible configuration capabilities in terms of some generation of discretionary output clock frequency, duty cycle together with specified phase relationship among input and output clock signals, which means nearly all of the functions of the PLL should be programmable.

A majority of the reported PLL circuits have been focused on optimizing the jitter or power performance[1−3] without sufficient consideration for multi-functional and reconfigurable characteristics required by the FPGA applications. On the other hand, the PLL clock generators used in the commercial FPGA chips are capable of providing multi-functions to guarantee the diversity of applications, however, usually they are unable to match with the performance of those reported standalone PLL chips in the aspects of frequency range, jitter and lock time, etc. To maximize both sides of the requirements, this paper presents a PLL clock generator with reconfigurable multi functions, yet sustaining the satisfying performances in comparison. The PLL has two configurable operation modes, including the clock generation mode and the skew compensation mode to achieve clock multiplication and phase alignment functions, respectively. Phase alignment can be realized by feeding back the external output clock or a middle point clock off the clock tree to align them with the input clock[3]. The output clock signal has advanced clock shift ability such that the phase shift and duty cycle are programmable by an ingenious post-scale counter design. All of these functions can be reconfigured by a serial data interface and its control logic. To guarantee the functions of phase shift and phase alignment accurately, a quick start-up technique is used in the VCO to attain an accurate phase relationship of the multi oscillating waveforms. A novel delay partition method is also proposed to improve the speed of the post-scale counter. Another reconfigurable design is implementation of a variable current charge pump that is used to achieve an approximately constant loop bandwidth over wide loop configuration settings, since the variable loop bandwidth will severely impact the phase-noise optimization and loop stability[4].

## 2. System design consideration

The block diagram of the proposed clock generator is shown in Fig. 1. The block $N$ is the pre-divider and $M$ is the feedback divider. The post-scale counter can divide down the high-frequency output of the VCO. So the whole system derives the output signal to match

$$f_{\rm OUT} = \frac{M}{N \cdot \text{postscale}} \cdot f_{\rm IN}. \quad (1)$$

The divider $N$ also eases the limit of the input frequency range.

The clock generator in Fig. 1 has three feedback loops which can be switched over to each other by configuration to implement different functions. The first one is the general PLL loop to achieve clock multiplication. The second includes a post-scale counter and a clock tree. A point in the middle of

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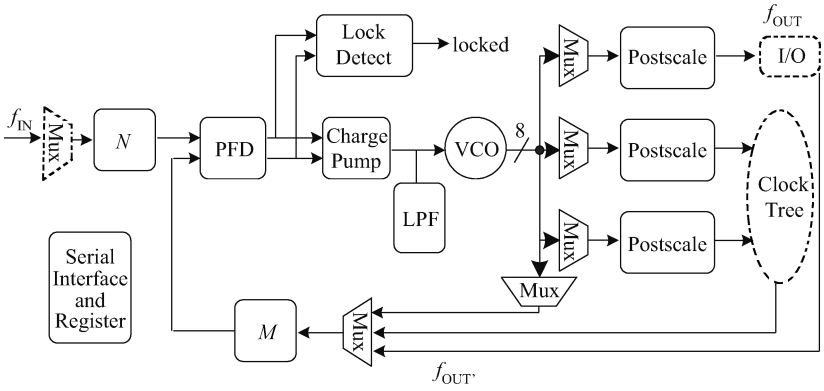


Fig. 1. Block diagram of the proposed clock generator.

the clock tree is chosen and used as a feedback signal to the PLL to reduce the skew of the clock tree for FPGA applications. The third includes a post-scale counter and an I/O port, which is bidirectional to add the matched I/O delay in the feedback path so as to align the external output clock $f_{OUT}$ with the external input clock accurately. As a further consideration to obtain the accurate phase alignment in the last two feedback loops, the dividers $M$ and $N$ must be matched and the dummy multiplexer (Mux) is placed before the divider $N$ to make sure the input signal and the feedback signal have matched paths into the phase/frequency detector (PFD).

The VCO in Fig. 1 is a 4-stage differential ring oscillator which can provide four phases and their complements with 45° phase shift per stage. By choosing a different phase from the eight signals, the absolute phase resolution equals $T_{VCO}/8$, where $T_{VCO}$ is the period of the VCO oscillating signal. This is the fine tuning of the phase. The coarse tuning implementing the absolute phase step of $T_{VCO}$ is realized through the post-scale counter.

An additional lock detect block is designed to indicate the state of locked or unlocked. In addition to the state expression of the PLL itself, the block output is always used as a sign or enable signal in FPGA applications. It is indispensable in such PLL clock generator design.

The division ratios of the divider $M$, $N$ and the post-scale counter are input through the serial interface and stored in the internal registers. All other configurations are also operated through the serial data interface and registers to control the phase shift and duty cycle of the output signal, the function modes, and the current of the charge pump according to the division ratio of $M$.

## 3. Circuit implementation

### 3.1. VCO

Because of the requirement of phase shift and phase alignment, the oscillating waves must keep an accurate phase relationship soon after the oscillation starts up; otherwise, the configured phase information will be interrupted by the small pulses during start-up of the VCO. So a quick start-up technique is proposed in the VCO design, one of the key circuits in the proposed clock generator.

Figure 2 shows the presented VCO, which comprises a

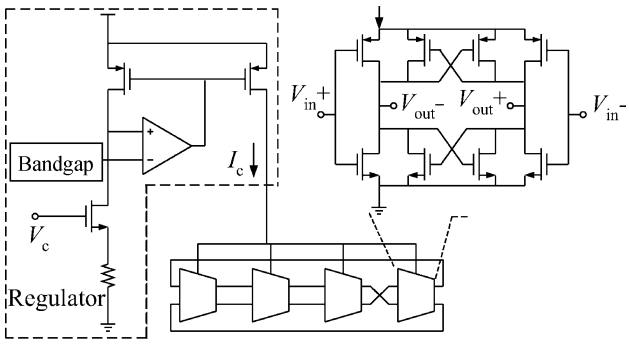


Fig. 2. Circuit diagram of the VCO.

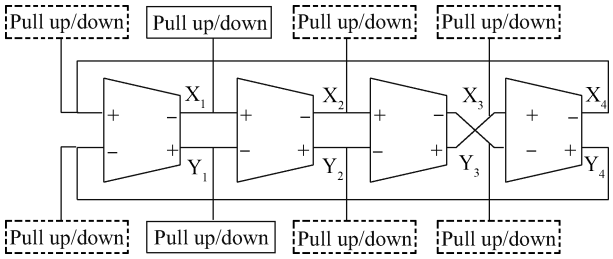


Fig. 3. 4-stage oscillator with pull up/down.

supply regulator and a 4-stage differential ring oscillator. The inverting stage of the oscillator can achieve a full-swing oscillation. The regulator converts the control voltage $V_c$ into the current $I_c$ and improves the power supply rejection ratio (PSRR) effectively[5]. This reduces the shift of the center frequency due to the supply voltage variation. In addition, it can reduce the power supply bounces on the jitter performance below the loop bandwidth of the regulator[6].

The principle of the proposed quick start-up technique is shown in Fig. 3. Unlike the conventional ring VCO[7, 8], a weak pull-up/down circuit is placed at each node of the oscillator. Two pull-up/down circuits at $X_1/Y_1$ are available while another six are dummies to make sure all stages are identical. The pull-up/down enable signal is the complement of the VCO enable signal. When the VCO is disabled, node $X_1$ will be high level by weak pull-up and node $Y_1$ will be low level by weak pull-down. Once the VCO is enabled, the pull-up/down is disabled and the circuit will oscillate immediately, as shown in

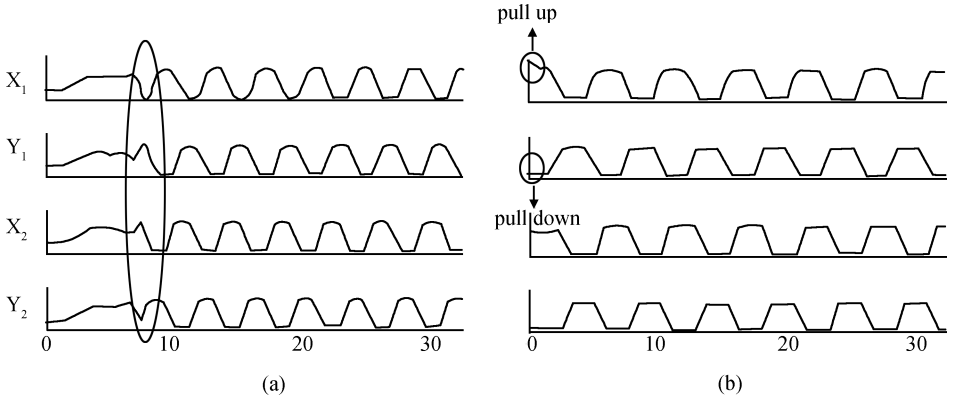


Fig. 4. Comparison of VCO start-up wave (a) without pull-up/down and (b) with pull-up/down.

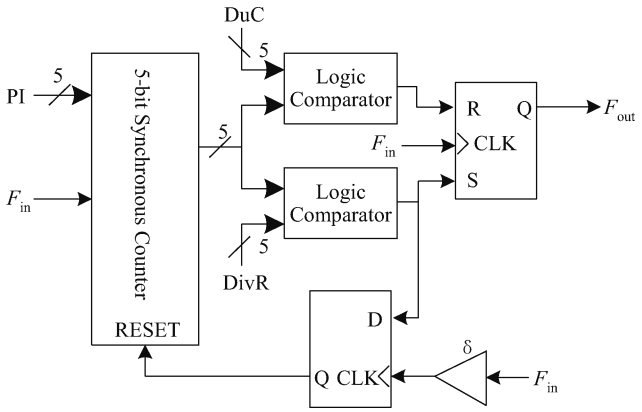


Fig. 5. Block diagram of post-scale counter.

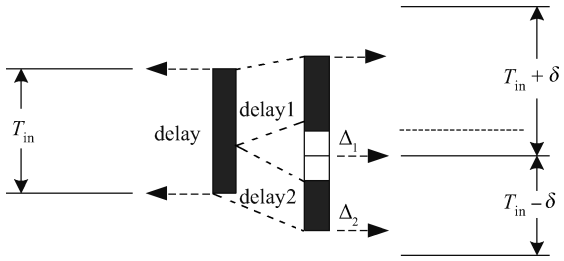


Fig. 6. A novel method to improve the speed of the post-scale counter.

Fig. 4(b). Because the pull-up/down circuits equivalently input an almost full-swing differential signal to the oscillator and the process of amplifying small differential signal stage by stage is no longer necessary. Such an oscillating wave does not include any small rise edge compared with the start-up wave of the VCO without a pull-up/down circuit in Fig. 4(a). The waves in Figs. 4(a) and 4(b) are controlled by the same enable signal. The small rise edges will probably disturb the initial phase configuration in the post-scale counter following the VCO. So the proposed technique avoids the failure of phase configuration. The pull-up/down circuits take little power expense since the pull-up/down is weak and the current $I_c$ is shut down when the pull-up/down circuit is enabled.

### 3.2. Post-scale counter

Figure 5 shows the block diagram of the post-scale counter, which implements a continuous division ratio of 1 : 32, programmable phase shift and duty cycle. The operating speed is limited by the function diversity of the counter. Therefore, a novel delay partition method is proposed to improve the speed of the counter.

The input of PI sets different initial values of the 5-bit synchronous counter to implement different phase shifts[8]. The counter value is compared with the configuration codes of the division ratio (DivR) and duty cycle (DuC) in the two logic comparator blocks, respectively. The comparison results are sent to control RS flip-flop, and then the programmable division and duty cycle are attained. The former comparison result is also fed back to reset the 5-bit synchronous counter to guarantee the exact value of division ratio.

The feedback path delay is a bottleneck that limits the speed of the post-scale counter. This paper takes a novel delay partition method to solve the problem. If there is not a D flip-flop in the feedback loop as a conventional counter, the period of the input clock $T_{in}$ could not become smaller than the delay of the feedback path (from the input end to the reset end of the 5-bit synchronous counter, including the setup time). This design in Fig. 5 releases such a limit by adding a D flip-flop in the feedback loop and triggering it by the clock signal generated by delaying the input clock. The reset signal can arrive at the counter during the next period of the input clock. The total feedback delay is partitioned into two parts, delay1 and delay2, as shown in Fig. 6, where $\Delta_1$ and $\Delta_2$ are small delays generated by the D flip-flop. The limits of $T_{in}$ become[9]

$$\begin{cases} \text{delay1} + \Delta_1 \leqslant T_{in} + \delta, \\ \text{delay2} + \Delta_2 \leqslant T_{in} - \delta. \end{cases} \tag{2}$$

The delay $\delta$ tunes the two time windows to make $T_{in}$ as small as possible. Such a method improves the speed of the post-scale counter effectively.

### 3.3. Charge pump

The open-loop transfer function of the PLL system in Fig. 1 is given by

$$H_{\text{open-loop}}(s) = \frac{I_P K_{VCO}}{2\pi M s} F(s), \tag{3}$$

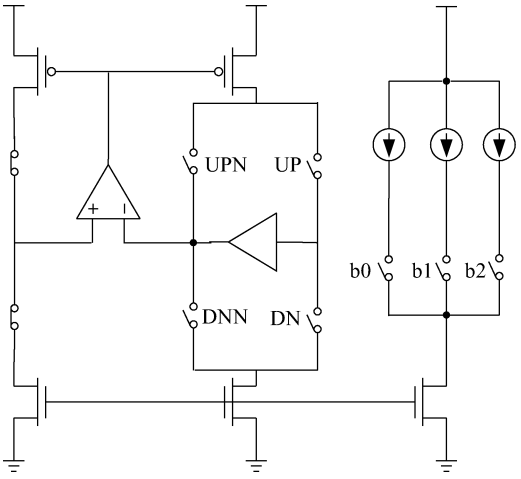


Fig. 7. A variable current charge pump.

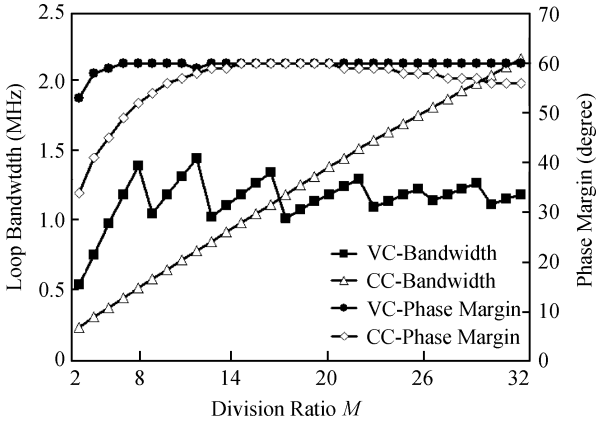


Fig. 8. Improvement of the loop bandwidth and phase margin by variable current charge pump.

where $K_{VCO}$ is the gain of the VCO, $F(s)$ is the transfer function of the low-pass filter (LPF), and $I_P$ is the charge and discharge current of the charge pump. To get the wide frequency tuning range, the loop division ratio $M$ varies from 2 to 32, which causes a big fluctuation in the loop bandwidth based on Eq. (3). The variance of the loop bandwidth affects the phase noise performance and loop stability. So as shown in Fig. 7, a variable current charge pump is designed to reduce such an effect[10]. The current of the charge pump can vary proportionally to the value of M through a 3-bit control signal, so the transfer function $H_{open\text{-}loop}(s)$ is almost invariable.

Figure 8 shows the simulated system loop bandwidths and phase margins with the variable current charge pump and a constant current charge pump as a comparison. Assuming that the VCO gain is constant, the current of the charge pump and the division ratio $M$ are main factors of the loop bandwidth and phase margin. As Figure 8 shows, the loop bandwidth of the system with constant charge and discharge current varies widely against the division ratio $M$ (the CC-bandwidth curve). Correspondingly, the loop bandwidth of the system with variable current fluctuates a little around the specific value 1.2 MHz (the VC-bandwidth curve). The division ratio 2–4 is barely used while the measured tuning range is 270 MHz to 1.5 GHz. So the VC-bandwidth curve is acceptable although

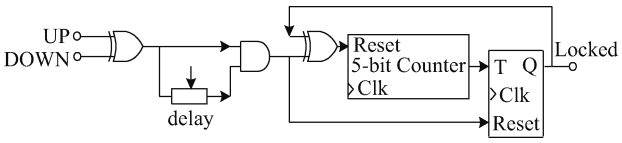


Fig. 9. Block diagram of the lock detect circuit.

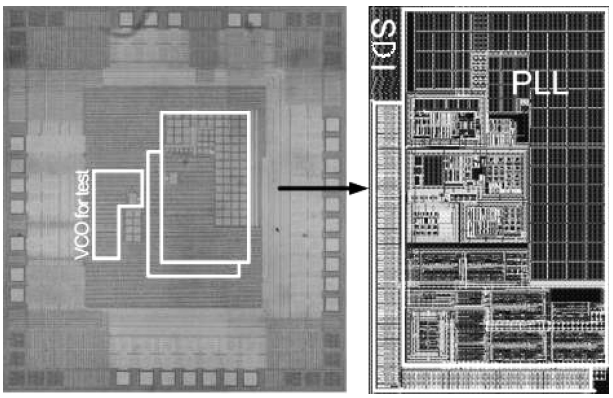


Fig. 10. Chip microphotograph of the proposed clock generator and layout of the core circuits.

the curve is deteriorating in the division range 2–4. The phase margin is insensitive to $M$ due to the second-order low-pass filter, but the variable current charge pump still improves the stability of the system with the comparison of the two curves CC-phasemargin and VC-phasemargin.

### 3.4. Lock detect circuit

The lock detect circuit gives a logic level output "locked" to indicate whether the PLL is in the locked state. As shown in Fig. 9, when the difference in the pulse widths between the UP and DOWN signals is below one specific value, the PLL is considered locked. The asymmetrical hysteresis is built into the lock detect circuit. When the condition of lock is satisfied for 32 periods of the reference clock, the signal "locked" becomes high level. But once the locked condition is not satisfied, the signal "locked" becomes low level.

In the ideal PLL system, the difference in the pulse widths between the UP and DOWN signals will turn to zero finally. But a real PLL will always have such a difference due to many nonideal factors, such as the mismatch between charge and discharge currents, the variant of the process. To ease the affect of these nonideal factors, the window of the locked state is reconfigurable by tuning the delay in Fig. 9.

## 4. Measurement results

The proposed clock generator is fabricated in a 0.13-$\mu$m CMOS process with a 1.5 V supply voltage. The chip microphotograph of the clock generator and the layout of the core circuits are shown in Fig. 10. The PLL occupies an active area of 0.36 mm$^2$, including the serial data interface and its control logic (SDI).

Figure 11(a) shows the test waveforms of the PLL enable signal, the "locked" signal and the output clock signal after the post-scale counter. When the enable signal is at a high level, the

Table 1. Performance comparison.

| Parameter | Ref. [11] | Ref. [12] | Ref. [13] | This work |
|---|---|---|---|---|
| Frequency tuning range (MHz) | 125–1250 (90%) | 480–1000 (52%) | 500–1000 (50%) | 270–15000 (82%) |
| Power consumption (mW) | 15.7 @ 486 MHz | 22 | N/A | 18 @ 1 GHz |
| Power down feature (mW) | N/A | N/A | N/A | < 1.5 |
| Power supply | 3.3/1.2 | N/A | 1.5 | 1.5 |
| Active area ($mm^2$) | 0.47 | 0.63 | N/A | 0.36 |
| Jitter (ps) | < 10.7 @ 486 MHz | 0.94 | N/A (< 300 ps pk–pk) | < 9 (< 58 ps pk–pk) |
| Lock time ($\mu$s) | N/A | 2.2 | > 10 | 2 |
| Multi function capability | N/A | N/A | Programmable phase shift and duty cycle, phase alignment | Programmable phase shift and duty cycle, phase alignment |
| Process technology | N/A | 0.13 $\mu$m CMOS | 0.13 $\mu$m CMOS | 0.13 $\mu$m CMOS |

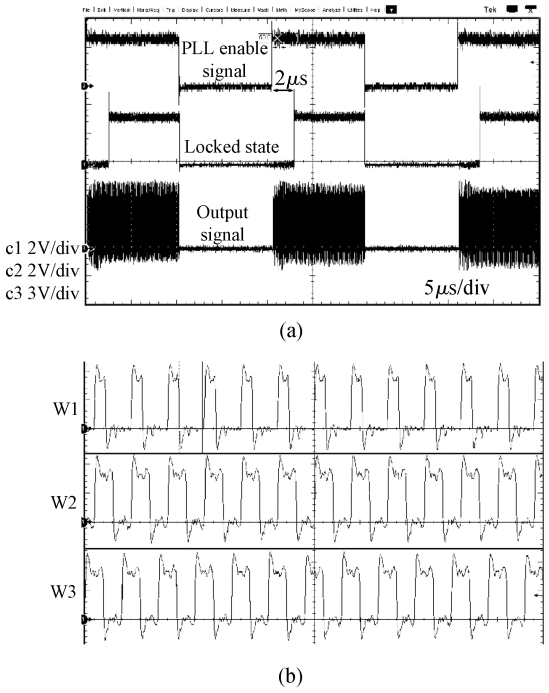


Fig. 11. Measured (a) lock state signal versus PLL enable signal and (b) output signal with programmable duty cycle and phase shift (deteriorated due to the bandwidth of the oscilloscope).

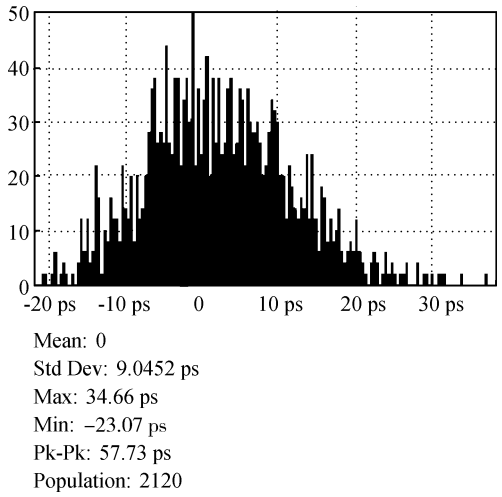


Fig. 12. Measured jitter histogram.

VCO starts to oscillate and the PLL starts the locking process. After about 2 $\mu$s, the locked state signal becomes high level, which means that the PLL has a fast lock time of 2 $\mu$s approximately. When the enable signal is at a low level, the locked state signal becomes low level, and the whole PLL is powered down. The measured power consumption locked at 1 GHz is about 13 mA, and less than 1 mA in the power-down state.

Figure 11(b) shows the output signal of the proposed clock generator. The PLL is locked at 1 GHz. The division ratio of the post-scale counter is 20, so the frequency of the output signal is 50 MHz. The duty cycle of the first waveform W1 is 30%, and the duty cycle of W2 is 50%. W3 is with the leading phase of $\pi/2$ compared with the two waveforms above. The programmable duty cycle and phase shift are reconfigured by the serial interface and registers.

According to the measurement results, the proposed PLL shows a wide tuning range of 270 MHz to 1.5 GHz with the RMS jitter of 9 ps at 1 GHz, as shown in Fig. 12. In fact, the tested signal is the 1 GHz clock signal divided down to 50 MHz by the post-scale counter. So the measured result has the jitter contribution from the post-scale counter. The real RMS jitter should be less than 9 ps at 1 GHz. There are also other reasons why the measured jitter is a little larger than some low-jitter design. Firstly, it results from the high VCO gain to realize the wide tuning range, which is proportional to the noise. Secondly, the measurement is carried out in real application environments. The proposed clock generator is integrated into a FPGA chip. All of the test work is done with the application circuit of the FPGA chip.

The skew compensation mode is also verified by feeding back the output signal through the bidirectional I/O. The phase of the output signal follows the phase of the input signal strictly according to the measurement result. But there is still a constant phase difference between the two signals due to the mismatch between the charge and discharge currents in the charge pump and the mismatch between the two paths from the input and output clock I/Os to the input terminals of the oscilloscope, respectively.

The measured performance of the clock generator is summarized in Table 1 compared with the recently published clock generators and the one in the Cyclone FPGA. In contrast with the recently reported PLLs[11, 12], the reconfigurable multi-

functions are the highlights of this work besides the comparatively satisfying performances. Compared with the commercial one[13], this work extended the frequency tuning range from 50% to 82%, improved the jitter performance from 300 to 58 ps (the peak–peak period jitter) and shortened the lock time from 10 to 2 $\mu$s.

## 5. Conclusion

This paper presents a reconfigurable multi-function PLL clock generator with a wide tuning range of 270 MHz to 1.5 GHz for FPGA applications. By configuration, the output clock signal has a variable phase shift and duty cycle. The clock generator also has the function of phase alignment between the clock tree or output clock and the input clock. A quick start-up technique is proposed to guarantee accurate phase shift and phase alignment. A novel delay partition method is proposed to improve the speed of the post-scale counter. The total power consumption at 1 GHz is 18 mW with a 1.5 V voltage supply, while it is less than 1.5 mW in the power down state.

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