Influence of growth temperatures on the quality of InGaAs/GaAs quantum well structure grown on Ge substrate by molecular beam epitaxy*

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Abstract: Molecular beam epitaxy growth of an $In_xGa_{1-x}As$/GaAs quantum well (QW) structure (x equals to 0.17 or 0.3) on offcut (100) Ge substrate has been investigated. The samples were characterized by atomic force microscopy, photoluminescence (PL), and high resolution transmission electron microscopy. High temperature annealing of the Ge substrate is necessary to grow GaAs buffer layer without anti-phase domains. During the subsequent growth of the GaAs buffer layer and an $In_xGa_{1-x}As$/GaAs QW structure, temperature plays a key role. The mechanism by which temperature influences the material quality is discussed. High quality $In_xGa_{1-x}As$/GaAs QW structure samples on Ge substrate with high PL intensity, narrow PL linewidth and flat surface morphology have been achieved by optimizing growth temperatures. Our results show promising device applications for III–V compound semiconductor materials grown on Ge substrates.

Key words: Ge substrate; InGaAs/GaAs quantum well; molecular beam epitaxy

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1. Introduction

III–V compound semiconductor materials grown on Ge substrates have attracted much attentions for years. On the one hand, light emission is hard to observe from Ge because of its indirect bandgap structure. Growing direct bandgap III–V compound semiconductor materials on Ge substrate is feasible to achieve good luminescence[1]. One of the reasons is that GaAs and Ge have almost the same lattice constant (lattice mismatch equals 0.08%) and it is easy to grow III–V compound semiconductor materials on GaAs. On the other hand, Ge substrate offers the advantages of low price, light weight, high strength, and large area compared to GaAs[1], and those advantages satisfy the need for both space and terrestrial solar cells[2, 3]. III–V solar cells which consist of a single junction or multi-junction based on Ge substrate have been rapidly developed. Since 2007, high efficiency (over 40%) multi-junction solar cells based on Ge substrate have been realized[4, 5].

Anti-phase domain (APD) is a key problem for growing GaAs on Ge substrate, as a polar on non-polar epitaxy[6]. It is suggested that APD can be eliminated by a double-step method using an offcut substrate[7–9]. However, it is not enough to grow APD-free GaAs on Ge just by using an offcut substrate by molecular beam epitaxy (MBE). The quality of epitaxial GaAs material depends intensively on the growth parameters[10, 11]. However, there is no discussion of the influence of growth temperature. In addition, most previous studies focus on the growth of GaAs, but few investigate the growth of other III–V compound semiconductor materials on Ge substrate.

In this work, MBE growth of an $In_xGa_{1-x}As$/GaAs quantum well (QW) structure (x equals 0.17 or 0.3) on offcut (100) Ge substrate has been investigated. The growth temperature has been found to have a crucial influence on the quality of GaAs/Ge hetero-epitaxy as well as the $In_xGa_{1-x}As$/GaAs QW structure. By optimizing the growth parameters, a high quality $In_xGa_{1-x}As$/GaAs QW structure with high PL intensity, narrow linewidth and flat surface morphology has been achieved. We focus on the surface morphology and optical properties, but the electronic properties of the GaAs/Ge hetero-structure is not studied here. This provides great application potential for III–V compound semiconductor lasers, detectors and solar cells based on Ge substrate.

2. Experiments

All of the samples were grown in a Veeco Mod Gen-II solid source MBE system. (100) Ge substrates, 6° off cut towards ⟨111⟩, were bought from the AXT company. Prior to being loaded into the growth chamber, a Ge substrate was baked at 180 ℃ for 3 h in the intro-chamber and then degassed at 420 ℃ for 0.5 h in the buffer chamber. In the growth chamber, firstly the Ge substrate was annealed at a relatively high temperature (T_A) for 20 min. Secondly, the substrate was exposed to an As_4 molecular beam for 2 min at a relatively low temperature (T_B) to form an As-terminated surface, while the As_4 beam equivalent pressure was 6.2×10^{-6} Torr. Thirdly, a 400 nm thick GaAs buffer layer was deposited at the same temperature at a growth rate of 0.8 μm/h. After that, the $In_xGa_{1-x}As$/GaAs QW structure was grown

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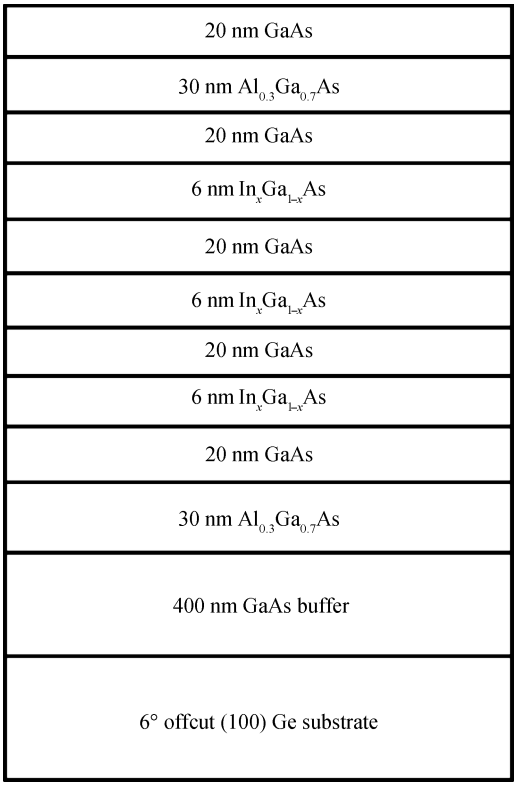

Fig. 1. Schematic diagram of the $In_xGa_{1-x}As$/GaAs quantum well structure on an offcut Ge substrate.

on the GaAs buffer at an even lower temperature (T_Q). The QW structure, which was sandwiched between two 30 nm $Al_{0.3}Ga_{0.7}As$ potential barrier layers, contains 3 periods of 6 nm $In_xGa_{1-x}As$ layer and 20 nm GaAs layer. Finally, a 20 nm thick GaAs layer was deposited to avoid the oxidation of the $Al_{0.3}Ga_{0.7}As$ layer. Among the samples, the range of T_A was from 680 to 735 ℃; the range of T_B was from 526 to 600 ℃; and the range of T_Q was from 445 to 500 ℃. A schematic diagram of the sample structure is displayed in Fig. 1.

The morphologies of all samples were measured using a Nanonavi Esweep S-II atomic force microscope (AFM) in contact mode. Photoluminescence (PL) spectra were measured at room temperature using a Nicolet FTIR760 Fourier transform spectrometer and detected by a liquid nitride cooled Ge detector. The excitation light source was the 632.8 nm line from a He–Ne laser and the power was about 11 mW. A Philips Tecnai F30 field emission gun transmission electron microscope (FEG-TEM) was used to evaluate the microstructure and crystal quality of GaAs/Ge interface.

3. Results and discussion

3.1. Influence of annealing temperature

Growing GaAs on Ge substrate, as a polar on non-polar epitaxy, will generate APD. It is suggested that APD can be eliminated by double-step method by using offcut Ge substrate with an appropriate off cut angle[8]. However, after chemical-mechanical polishing (CMP), the double-step structure is partly destroyed so that the off cut Ge substrate surface contains not only double-steps but also single-steps. These single-steps will result in APDs during the GaAs epitaxy on Ge. It was found that high temperature annealing can effectively help to generate a double-stepped Ge surface[10].

In our experiment, first series samples (A1, A2, A3, A4) were grown to study the influence of high temperature annealing. The growth parameters were the same for the four samples except that the annealing temperatures were 680, 698, 715, and 735 ℃ for A1, A2, A3, and A4, respectively. The highest T_A was set at 735 ℃, since the highest temperature to which the substrate could be heated was 770 ℃.

Figure 2(a) shows that the root mean square (RMS) roughness ($10 \times 10\ \mu m^2$) increases from 0.73 to 2.47 nm while T_A decreases from 735 to 680 ℃. Flat surface morphologies of A4 can be seen in Fig. 2(b) while there are several pits on the surface of sample A1 from Fig. 2(c). These pits are thought to be APDs. The comparison of A1 and A4 indicates that high temperature annealing is necessary to obtain APD-free GaAs layers on Ge substrate. Further improvement of the RMS roughness can be realized by optimizing the growth of the GaAs buffer layer, which is described in the next section.

Figures 2(d) and 2(e) show the surface morphologies ($500 \times 500\ nm^2$) of sample B4 and offcut Ge substrate (without high temperature annealing), respectively. Compared with sample A4, sample B4 has the same T_A (735 ℃) and T_Q (472 ℃) but different T_B. Obvious lines, i.e., atomic steps, can be seen in both figures. However, the atomic steps on sample B4 have better uniformity along a special direction than those of Ge substrate. Since double-steps and single-steps cannot be transformed during the epitaxial growth of GaAs buffer and QW structure, the better uniform atomic steps are attributed to the high temperature annealing. For the same reason, the atomic steps should be the same for A4 and B4, although they have different GaAs buffer growth temperatures (T_B). Additionally, sample B4 has a smaller RMS roughness of 0.32 nm than Ge substrate (0.34 nm). The flat surface of sample B4 (in Fig. 2(f)) also indicates a high quality GaAs/Ge interface. The TEM image of sample B4 in Fig. 3 directly proves the existence of a flat GaAs/Ge interface without APDs.

These results show that high temperature annealing is necessary to generate double-steps on Ge substrate surface and thus necessary to grow high quality GaAs layers on Ge substrate without APDs.

3.2. Influence of GaAs buffer growth temperature

Since the smallest RMS roughness value was obtained on sample A4 among the first series samples, the same annealing temperature 735 ℃ was used in the second series samples B1, B2, B3, B4 and B5. Apart from the growth temperature of the 400 nm GaAs buffer layer, the other growth parameters were the same for the five samples. T_B was 526, 544, 562, 580, and 600 ℃ for B1, B2, B3, B4, and B5, respectively. For the $In_xGa_{1-x}As$/GaAs QW structure in the first two series samples, x was 0.17 and the QW growth temperature was 472 ℃. The PL peak energy is 1.27 eV and the full width at half maximum (FWHM) is smaller than 17 meV.

Figure 4 shows the dependence of the RMS roughness ($10 \times 10\ \mu m^2$) and PL intensity on T_B. It can be seen that the RMS roughness decreases from 0.73 to 0.32 nm while T_B in-

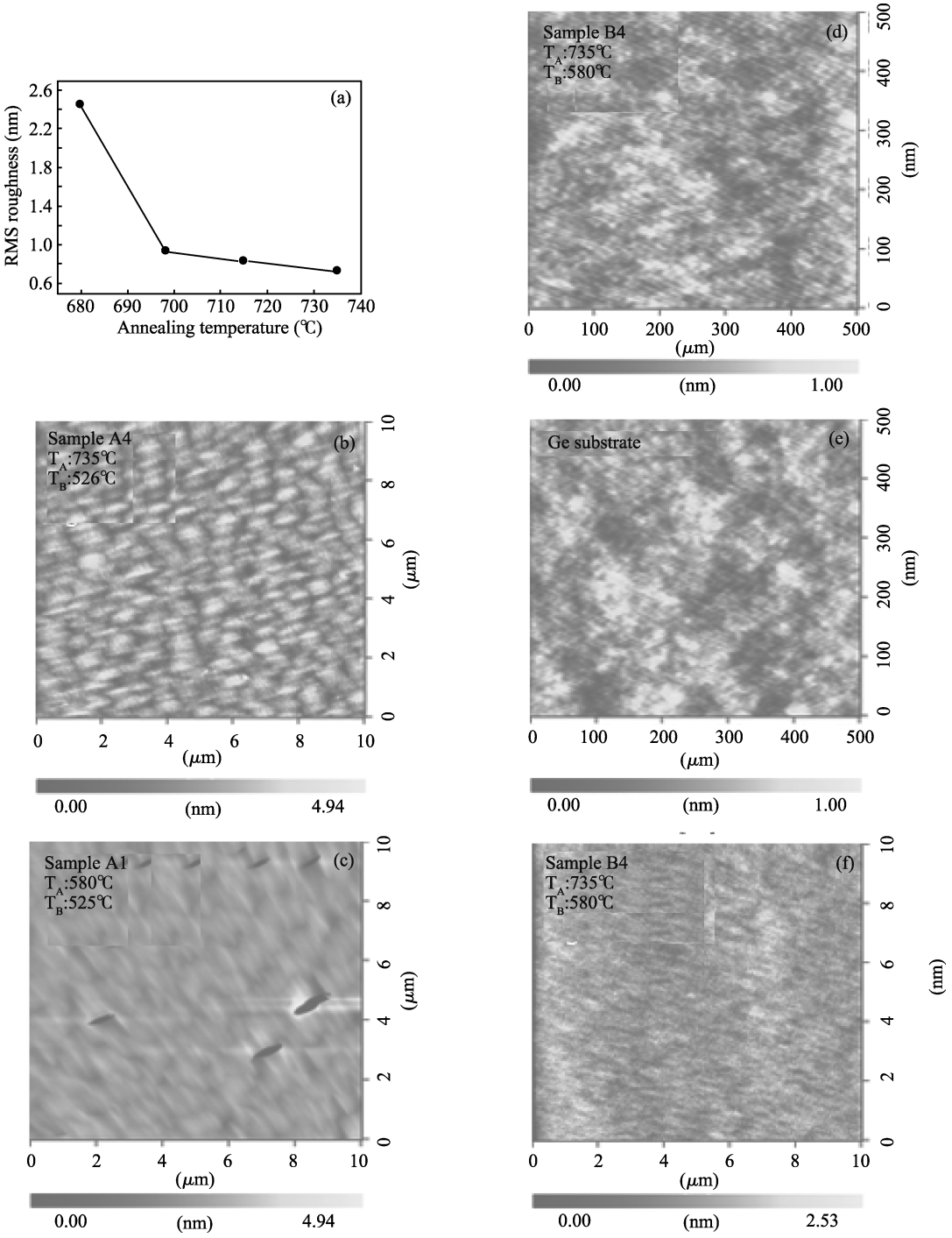

Fig. 2. (a) RMS roughness of samples A1, A2, A3 and A4 grown at different annealing temperatures. (b), (c) AFM images (10×10 μm^2) of samples A4 and A1. (d), (e) AFM images (500×500 nm^2) of sample B4 and Ge substrate. (f) AFM image (10×10 μm^2) of sample B4.

creases from 526 to 580 ℃, and then keeps constant at 0.32 nm when T_B further increases to 600 ℃. Considering that the RMS roughness of Ge substrate is 0.34 nm, this value of 0.32 nm shows that sample B4 (B5) has a very flat surface.

From Fig. 4, it can also be seen that as T_B increases from 526 to 600 ℃, the PL intensity first climbs up rapidly to a peak value at 580 ℃, and then begins to fall down. The increase in PL intensity with T_B from 526 to 580 ℃ is consistent with the decrease in RMS roughness, due to the improved quality of the GaAs/Ge interface and GaAs buffer layer. However, the PL peak intensity becomes smaller when T_B increases to 600 ℃. There are two competing mechanisms that influence the GaAs buffer. On one hand, at high temperature, the migration of Ga atoms increases because of the high thermal energy, which improves the GaAs buffer uniformity. Note that 580 ℃ is often used as the growth temperature of GaAs on GaAs substrate in MBE. On the other hand, the intermixing of Ga and As atoms with Ge atoms near the GaAs/Ge interface becomes more and more serious as the temperature increases. These two mechanisms reach a balance at 580 ℃. When the growth temperature is lower than 580 ℃, the first mechanism plays an important role, while the second one becomes dominant when the

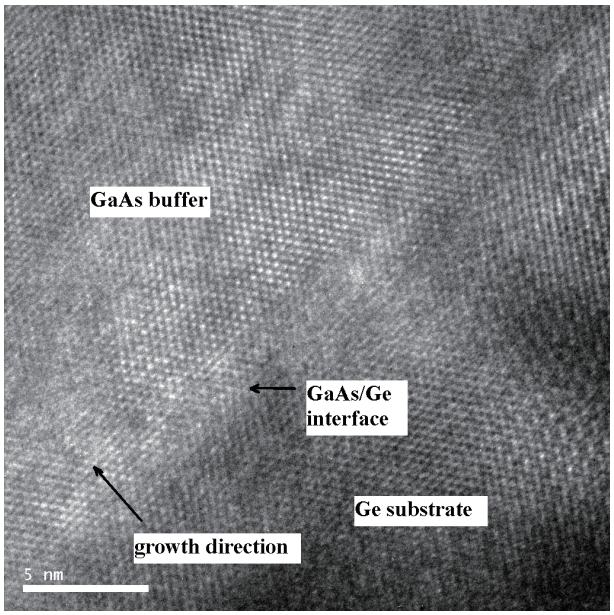

Fig. 3. Cross-sectional HRTEM image of GaAs/Ge interface.

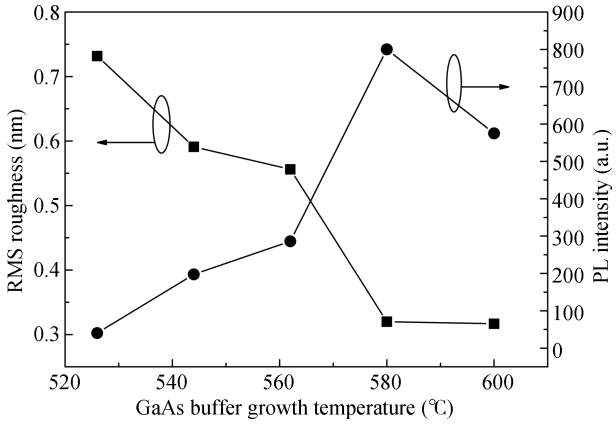

Fig. 4. Dependence of RMS roughness and PL intensity on GaAs buffer growth temperature (T_B) for the second series samples B1, B2, B3, B4, and B5.

temperature is above 580 ℃. As a result, the quality of the GaAs/Ge interface and GaAs buffer becomes worse and the $In_xGa_{1-x}As$/GaAs QW exhibits low PL intensity.

Combining the RMS roughness and PL intensity, 580 ℃ is found to be the most appropriate temperature for GaAs buffer layer growth. So T_B was set to be 580 ℃ in the growth of a third series samples Q1, Q2, Q3 and Q4.

3.3. Influence of $In_xGa_{1-x}As$/GaAs quantum well growth temperature

The peak wavelength of $In_{0.17}Ga_{0.83}As$/GaAs QW is 976 nm (1.27 eV), which is far away from the 1300–1550 nm range useful for fiber communication. In order to extend the wavelength, we increased the indium content of $In_xGa_{1-x}As$/GaAs QW. We chose $x = 0.3$ in the third series samples Q1, Q2, Q3 and Q4. The annealing temperature was set at 735 ℃ while the growth temperature for 400 nm GaAs buffer was 580 ℃. The growth rate of $In_{0.3}Ga_{0.7}As$ was 1 μm/h, and the V/III ratio

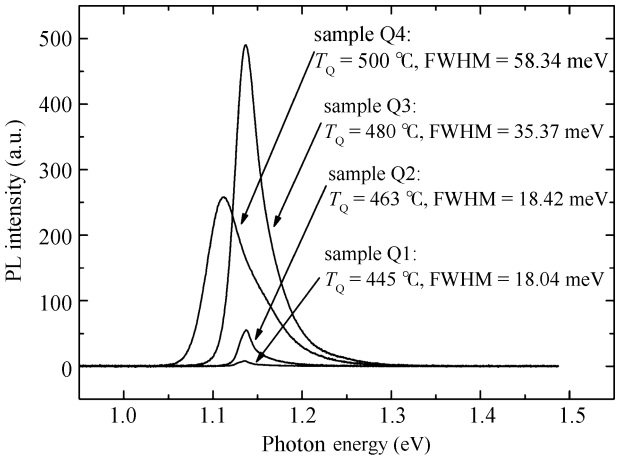

Fig. 5. Room temperature PL spectrum of the third series samples Q1, Q2, Q3 and Q4 grown at different quantum well temperatures (T_Q).

was 20. The thickness of the $In_{0.3}Ga_{0.7}As$ layer, 6 nm, is less than the critical thickness according to our previous work[12]. The only difference among the four samples was the growth temperature of the $In_{0.3}Ga_{0.7}As$/GaAs QW layers, which was 445, 463, 480, and 500 ℃ for Q1, Q2, Q3, and Q4, respectively. Thus, different properties of those samples should originate from the different QW layer growth temperatures T_Q. The RMS roughness of all of the third series samples is below 0.40 nm, so that the influence of T_Q on the surface morphology is negligible.

From Fig. 5, three trends can be seen. Firstly, the PL intensity increases significantly from 445 to 480 ℃ and then drops with further increase in temperature. Secondly, the FWHM becomes broad with an increase in T_Q. Finally, the PL peak energy has an obvious red shift for Q4 (500 ℃) compared to the other three samples. Explanations are as follows. Increasing the growth temperature enhances the intermixing of In and Ga atoms at the $In_{0.3}Ga_{0.7}As$/GaAs QW interface, which consequently results in the fluctuation of interface[13]. The fluctuation of QW interface not only leads to the broadening of FWHM but also to the weakening of quantum confinement for carriers in the $In_{0.3}Ga_{0.7}As$ well, which attributes to the red shift of PL peal energy. On the other hand, the migration of atoms on the epitaxial surface (during the growth) is enhanced at higher temperature because of the high thermal energy, leading to a well-ordered InGaAs alloy and strong PL intensity when T_Q rises from 445 to 480 ℃[13]. However, when T_Q increases further to 500 ℃, the interface fluctuation plays the dominant role so that the PL intensity decreases. Those results indicate that there is an appropriate growth temperature window for the InGaAs/GaAs QW structure.

4. Conclusions

In conclusion, the $In_xGa_{1-x}As$/GaAs QW structure has been grown on offcut (100) Ge substrate using MBE. The growth temperature is found to have a crucial influence on the quality of GaAs/Ge hetero-epitaxy as well as the $In_xGa_{1-x}As$/GaAs QW structure. Prior to epitaxial growth, high temperature annealing is necessary to generate a uniform double-step surface on Ge substrates to eliminate APD during

the subsequent growth of GaAs. An appropriate high growth temperature is necessary for high quality epitaxy as enhanced migration for atoms, but the serious intermixing of GaAs/Ge and the $In_xGa_{1-x}As$/GaAs interface may result in poor crystal quality when the growth temperature is too high. The optimized sample shows small RMS roughness of 0.32 nm and narrow linewidth under AFM and PL measurement.

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