A two-dimensional analytical model of fully depleted asymmetrical dual material gate double-gate strained-Si MOSFETs*

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Abstract: On the basis of the exact resultant solution of two dimensional Poisson's equations, a new accurate two-dimensional analytical model comprising surface channel potentials, a surface channel electric field and a threshold voltage for fully depleted asymmetrical dual material gate double-gate strained-Si MOSFETs is successfully developed. The model shows its validity by good agreement with the simulated results from a two-dimensional numerical simulator. Besides offering a physical insight into device physics, the model provides basic design guidance for fully depleted asymmetrical dual material gate double-gate strained-Si MOSFETs.

Key words: dual material gate; double-gate MOSFET; strained-Si; short-channel effect; the drain-induced barrier-lowering

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1. Introduction

Double-gate MOSFETs seem to be a very promising option for ultimate scaling of CMOS technology[1]. Excellent short-channel effect (SCE) immunity, high transconductance, and ideal subthreshold performance[2, 3] have been reported from theoretical and experimental work on this device. In particular, asymmetrical DG SOI MOSFETs are becoming popular since these structures provide a desirable threshold voltage unlike symmetrical DG SOI MOSFETs. To enhance the immunity against SCEs, a new structure called a dual-material (DMG) gate MOSFET has been proposed. A dual-material gate structure induces the peak of the electric field at the interface between the different materials, which enhances the carrier's speed and improves the device's performance[4−6]. In addition, strained-Si devices can enhance mobility, high-field velocity and velocity overshoot of carriers are promising candidates for future high-performance MOSFETs[7]. To incorporate the advantage of asymmetrical DG MOSFETs and dual-material gate structure and strained-Si devices, the asymmetrical dual material gate double-gate strained-Si MOSFET has been proposed. In this paper, a novel, fully depleted asymmetrical dual material gate double-gate strained-Si MOSFETs is investigated. The analytical models for surface potential distribution and threshold voltage are derived based on the two dimensional Poisson's equations. The models are verified by the simulation results that agree well with those of the two-dimensional numerical simulator. With appropriate modification, the model can also be extended to asymmetrical and symmetrical DG MOSFETs.

2. Strained-Si MOSFET

2.1. Effect of strain on bandgap

In the presence of strain, the silicon thin film experiences biaxial tension and changes its band structure[8−11]. The strain can increase the electron affinity of silicon. It can also cause the bandgap and the effective mass of carriers to decrease. The above strain-related effects on the silicon band structure are modeled as follows[12, 13],

$$(\Delta E_{\mathrm{C}})_{\mathrm{s\text{-}Si}} = 0.57X, \tag{1}$$

$$(\Delta E_{\mathrm{g}})_{\mathrm{s\text{-}Si}} = 0.4X, \tag{2}$$

$$V_{\mathrm{T}} \ln \frac{N_{\mathrm{V,\,Si}}}{N_{\mathrm{V,\,s\text{-}Si}}} = V_{\mathrm{T}} \ln \left(\frac{m^*_{\mathrm{h,\,Si}}}{m^*_{\mathrm{h,\,s\text{-}Si}}} \right)^{3/2} = 0.075X, \tag{3}$$

where X is the strain in the equivalent Ge mole fraction in the relaxed SiGe butter layer, $(\Delta E_{\mathrm{C}})_{\mathrm{s\text{-}Si}}$ is the increase in electron affinity of silicon due to strain, $(\Delta E_{\mathrm{g}})_{\mathrm{s\text{-}Si}}$ is the decrease in the bandgap of silicon due to strain, and V_{T} is the thermal voltage. $N_{\mathrm{V,\,Si}}$ and $N_{\mathrm{V,\,s\text{-}Si}}$ are the density of states (DOS) in the valence band in normal and strained-Si, respectively, $m^*_{\mathrm{h,\,Si}}$ and $m^*_{\mathrm{h,\,s\text{-}Si}}$ are the effective masses of hole DOS in normal and strained-Si, respectively.

2.2. Effect of strain on flatband voltage

Since the structure is symmetrical, the effect of strain on the front-channel flatband and back-channel flatband voltage of this structure MOSFET can be modeled as follows[12, 13],

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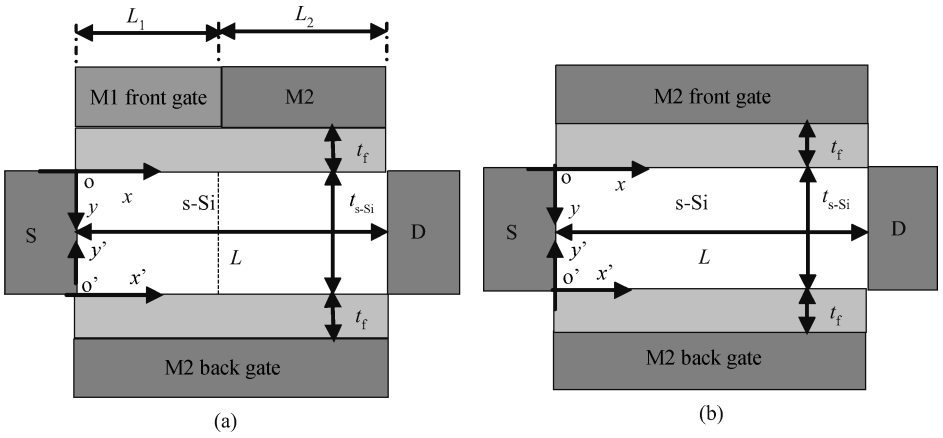

Fig. 1. Schematic structure of (a) a asymmetrical DMG DG strained-Si MOSFET and (b) a symmetrical DG strained-Si MOSFET.

$$(V_{\mathrm{FB,f}})_{\text{s-Si}} = (V_{\mathrm{FB,f}})_{\mathrm{Si}} + \Delta V_{\mathrm{FB,f}}, \tag{4}$$

where

$$(V_{\mathrm{FB,f}})_{\mathrm{Si}} = \phi_{\mathrm{M}} - \phi_{\mathrm{Si}},$$

$$\Delta V_{\mathrm{FB,f}} = \frac{-(\Delta E_{\mathrm{C}})_{\text{s-Si}}}{q} + \frac{(\Delta E_{\mathrm{g}})_{\text{s-Si}}}{q} - V_{\mathrm{T}} \ln \frac{N_{\mathrm{V,Si}}}{N_{\mathrm{V,s\text{-}Si}}},$$

$$\phi_{\mathrm{Si}} = \chi_{\mathrm{Si}}/q + E_{\mathrm{g,Si}}/2q + \phi_{\text{f-Si}},$$

$$\phi_{\text{f-Si}} = V_{\mathrm{T}} \ln(N_{\mathrm{A}}/n_{\mathrm{i,Si}}).$$

In the above relations, ϕ_{M} is the work function of the gate, ϕ_{Si} is the work function of unstrained-Si, $\phi_{\text{f-Si}}$ is the Fermi potential of unstrained-Si, $E_{\mathrm{g,Si}}$ is the bandgap of unstrained-Si, q is the electronic charge, N_{A} is the body doping concentration, and $n_{\mathrm{i,Si}}$ is the intrinsic carrier concentration in unstrained-Si.

It is also important to consider the effect of strain on the built-in voltage across the source-body and drain-body junctions in strained-Si thin film, which can be written as

$$V_{\mathrm{bi,s\text{-}Si}} = V_{\mathrm{bi,Si}} + (\Delta V_{\mathrm{bi}})_{\text{s-Si}}, \tag{5}$$

where

$$V_{\mathrm{bi,Si}} = \frac{E_{\mathrm{g,Si}}}{2q} + \phi_{\mathrm{F,Si}},$$

$$(\Delta V_{\mathrm{bi}})_{\text{s-Si}} = \frac{-(\Delta E_{\mathrm{g}})_{\text{s-Si}}}{q} - V_{\mathrm{T}} \ln \frac{N_{\mathrm{V,Si}}}{N_{\mathrm{V,s\text{-}Si}}}.$$

3. Model formulation

3.1. Two-dimensional model for surface potential

The schematic cross-section view of an FD asymmetrical DMG DG strained-Si MOSFET is shown in Fig. 1(a), and that of symmetrical DG strained-Si MOSFET is shown in Fig. 1(b). In Fig. 1(a), the lengths of the gate metals M1 and M2 are L_1 and L_2, respectively. Assuming the channel doping to be uniform, the channel region is divided into two different zones since two kinds of gate materials are used. Neglecting the effect of the fixed oxide charges on the electrostatics of the channel, the Poisson's equation of the potential distribution in the two strained-Si zones before the onset of strong inversion can be written as[14–16]

$$\frac{\partial^2 \phi_1(x,y)}{\partial x^2} + \frac{\partial^2 \phi_1(x,y)}{\partial y^2} = \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{Si}}}, \quad 0 \leqslant x \leqslant L_1, 0 \leqslant y \leqslant t_{\text{s-Si}}, \tag{6}$$

$$\frac{\partial^2 \phi_2(x,y)}{\partial x^2} + \frac{\partial^2 \phi_2(x,y)}{\partial y^2} = \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{Si}}}, \quad L_1 \leqslant x \leqslant L, 0 \leqslant y \leqslant t_{\text{s-Si}}, \tag{7}$$

$$\frac{\partial^2 \phi_3(x',y')}{\partial x'^2} + \frac{\partial^2 \phi_3(x',y')}{\partial y'^2} = \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{Si}}}, \quad 0 \leqslant x' \leqslant L_1, 0 \leqslant y' \leqslant t_{\text{s-Si}}, \tag{8}$$

$$\frac{\partial^2 \phi_4(x',y')}{\partial x'^2} + \frac{\partial^2 \phi_4(x',y')}{\partial y'^2} = \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{Si}}}, \quad L_1 \leqslant x' \leqslant L, 0 \leqslant y' \leqslant t_{\text{s-Si}}, \tag{9}$$

where N_{A} is the doping density of the strained-Si layer, $\varepsilon_{\mathrm{Si}}$ is the dielectric constant of the strained-Si layer, $t_{\text{s-Si}}$ is the thickness of the strained-Si layer, L is the gate length, and $L = L_1 + L_2$, with the x-axis parallel to the channel and the y-axis perpendicular to the channel. The potential profile in the vertical direction in the strained-Si layer can be approximated by a parabolic function,

$$\phi_1(x,y) = \phi_{s1}(x) + c_{11}(x)y + c_{12}(x)y^2, \quad 0 \leqslant x \leqslant L_1, 0 \leqslant y \leqslant t_{\text{s-Si}}, \tag{10}$$

$$\phi_2(x,y) = \phi_{s2}(x) + c_{21}(x)y + c_{22}(x)y^2, \quad L_1 \leqslant x \leqslant L,\ 0 \leqslant y \leqslant t_{\text{s-Si}}, \tag{11}$$

$$\phi_3(x',y') = \phi_{\mathrm{b1}}(x') + c_{31}(x')y' + c_{32}(x')y'^2, \quad 0 \leqslant x' \leqslant L_1, 0 \leqslant y' \leqslant t_{\text{s-Si}}, \tag{12}$$

$$\phi_4(x',y') = \phi_{\mathrm{b2}}(x') + c_{41}(x')y' + c_{42}(x')y'^2, \quad L_1 \leqslant x' \leqslant L,\ 0 \leqslant y' \leqslant t_{\text{s-Si}}, \tag{13}$$

where $\phi_{s1}(x)$ and $\phi_{s2}(x)$ are the front channel surface potential under M1, M2, respectively, and $\phi_{b1}(x')$ and $\phi_{b2}(x')$ is the back channel surface potential. The coefficients $c_{11}(x)$, $c_{12}(x)$, $c_{21}(x)$ and $c_{22}(x)$ are only functions of x, and $c_{31}(x')$, $c_{32}(x')$, $c_{41}(x')$ and $c_{42}(x')$ are only functions of x'. The Poisson's equations can be solved using the following boundary conditions.

(1) At the top side, the electric flux (displacement) at the gate-oxide/strained-Si layer interface is continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}y}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_{s1}(x)-V'_{GS1}}{t_f}, \tag{14}$$

$$\left.\frac{\mathrm{d}\phi_2(x,y)}{\mathrm{d}y}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_{s2}(x)-V'_{GS2}}{t_f}, \tag{15}$$

$$\left.\frac{\mathrm{d}\phi_3(x',y')}{\mathrm{d}y'}\right|_{y'=t_{s\text{-}Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V'_{GS1}-\phi_3(x',t_{s\text{-}Si})}{t_f}, \tag{16}$$

$$\left.\frac{\mathrm{d}\phi_4(x',y')}{\mathrm{d}y'}\right|_{y'=t_{s\text{-}Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V'_{GS2}-\phi_4(x',t_{s\text{-}Si})}{t_f}, \tag{17}$$

where ε_{ox} is the dielectric constant of the gate oxide, t_f is the gate oxide thickness and V_{GS} is the gate-to-source bias voltage, $V'_{GS1} = V_{GS} - (V_{FB1,f})_{s\text{-}Si}$, $V'_{GS2} = V_{GS} - (V_{FB2,f})_{s\text{-}Si}$, $(V_{FB2,f})_{Si} = \phi_{M2} - \phi_{Si}$, $(V_{FB1,f})_{Si} = \phi_{M1} - \phi_{Si}$.

(2) At the bottom side, the electric flux (displacement) of the gate-oxide/strained-Si layer interface is continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}y}\right|_{y=t_{s\text{-}Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V'_{GS2}-\phi_1(x,t_{s\text{-}Si})}{t_f}, \tag{18}$$

$$\left.\frac{\mathrm{d}\phi_2(x,y)}{\mathrm{d}y}\right|_{y=t_{s\text{-}Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V'_{GS2}-\phi_2(x,t_{s\text{-}Si})}{t_f}, \tag{19}$$

$$\left.\frac{\mathrm{d}\phi_3(x',y')}{\mathrm{d}y'}\right|_{y'=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_{b1}(x')-V'_{GS2}}{t_f}, \tag{20}$$

$$\left.\frac{\mathrm{d}\phi_4(x',y')}{\mathrm{d}y'}\right|_{y'=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_{b2}(x')-V'_{GS2}}{t_f}. \tag{21}$$

(3) At the source side, the channel potential must be equal to the built-in potential for the junction of the source and body,

$$\phi_1(0,0) = \phi_S(0) = V_{bi,\,s\text{-}Si} = \phi_b(0) = \phi_3(0,0). \tag{22}$$

(4) At the drain side, the channel potential must be equal to the built-in potential for the junction of the source and body plus the drain-to-source bias voltage,

$$\phi_2(L,t_{s\text{-}Si}) = V_{bi,\,s\text{-}Si} + V_{DS} = \phi_4(L,t_{s\text{-}Si}), \tag{23}$$

where V_{DS} is the drain-to-source bias voltage.

(5) The potential and the electric flux at the interface of M1and M2 are equal,

$$\phi_1(L_1,0) = \phi_2(L_1,0), \tag{24}$$

$$\phi_3(L_1,0) = \phi_4(L_1,0), \tag{25}$$

$$\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}x}|_{x=L_1} = \frac{\mathrm{d}\phi_2(x,y)}{\mathrm{d}x}|_{x=L_1}, \tag{26}$$

$$\frac{\mathrm{d}\phi_3(x',y')}{\mathrm{d}x'}|_{x'=L_1} = \frac{\mathrm{d}\phi_4(x',y')}{\mathrm{d}x'}|_{x'=L_1}. \tag{27}$$

Using the boundary condition equations. (10)–(13), one can obtain the coefficients $c_{11}(x)$, $c_{12}(x)$, $c_{21}(x)$, $c_{22}(x)$, $c_{31}(x')$, $c_{32}(x')$, $c_{41}(x')$ and $c_{42}(x')$, and then obtain the expressions for $\phi_1(x,y)$, $\phi_2(x,y)$, $\phi_3(x',y')$ and $\phi_4(x',y')$. Substituting $\phi_1(x,y)$, $\phi_2(x,y)$, $\phi_1(x,y)$ and $\phi_2(x,y)$ into Eqs. (6)–(9), respectively, and substituting $y=0$ or $y'=0$, one obtains

$$\frac{\mathrm{d}^2\phi_{s1}(x)}{\mathrm{d}x^2} - \alpha^2\phi_{s1}(x) = \beta_1, \tag{28}$$

$$\frac{\mathrm{d}^2\phi_{s2}(x)}{\mathrm{d}x^2} - \alpha^2\phi_{s2}(x) = \beta_2, \tag{29}$$

$$\frac{\mathrm{d}^2\phi_{b1}(x')}{\mathrm{d}x'^2} - \alpha^2\phi_{b1}(x') = \beta_3, \tag{30}$$

$$\frac{\mathrm{d}^2\phi_{b2}(x')}{\mathrm{d}x'^2} - \alpha^2\phi_{b2}(x') = \beta_4, \tag{31}$$

where

$$\alpha^2 = \frac{2\varepsilon_{ox}}{\varepsilon_{si}t_f t_{si}},$$

$$\beta_1 = \frac{qNA}{\varepsilon_{si}} - \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V'_{GS2}+(1+a_1)V'_{GS1}}{t_f t_{si}\left(1+\frac{1}{2}a_1\right)},$$

$$\beta_2 = \frac{qNA}{\varepsilon_{si}} - \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{2V'_{GS2}}{t_f t_{si}} = \beta_4,$$

$$\beta_3 = \frac{qNA}{\varepsilon_{si}} - \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V'_{GS1}+(1+a_1)V'_{GS2}}{t_f t_{si}\left(1+\frac{1}{2}a_1\right)}.$$

Here, $a_1 = \frac{\varepsilon_{ox}t_{si}}{\varepsilon_{Si}t_f}$.

The solutions for Eqs. (28)–(31) are simple second-order non-homogenous differential equations with constant coefficients, which can be written as

$$\phi_{s1}(x) = A\exp(\alpha x) + B\exp(-\alpha x) - \frac{\beta_1}{\alpha^2}, \tag{32}$$

$$\phi_{s2}(x) = C\exp[\alpha(x-L_1)] + D\exp[-\alpha(x-L_1)] - \frac{\beta_2}{\alpha^2}, \tag{33}$$

$$\phi_{b1}(x') = E\exp(\alpha x') + F\exp(-\alpha x') - \frac{\beta_3}{\alpha^2}, \tag{34}$$

$$\phi_{b2}(x') = G\exp\left[\alpha(x'-L_1)\right] + H\exp\left[-\alpha(x'-L_1)\right] - \frac{\beta_4}{\alpha^2}. \tag{35}$$

Now, using boundary conditions (3), (4) and (5) to solve for A, B, C, D, E, F, G and H, one obtains

$$\begin{aligned} A = &\left[\frac{\beta_2-\beta_1}{2\alpha^2}\exp(\alpha L_2) + \frac{\beta_2-\beta_1}{2\alpha^2}\exp(-\alpha L_2) - \frac{\beta_2}{\alpha^2}\right. \\ &\left. + \left(V_{bi,\,s\text{-}Si} + \frac{\beta_1}{\alpha^2}\right)\exp(-\alpha L) - V_{bi,\,s\text{-}Si} - V_{DS}\right] \\ &\times[\exp(-\alpha L) - \exp(\alpha L)]^{-1}, \end{aligned} \tag{36}$$

$$\begin{aligned} B = &\left[\frac{\beta_2-\beta_1}{2\alpha^2}\exp(\alpha L_2) + \frac{\beta_2-\beta_1}{2\alpha^2}\exp(-\alpha L_2) - \frac{\beta_2}{\alpha^2}\right. \\ &\left. + \left(V_{bi,\,s\text{-}Si} + \frac{\beta_1}{\alpha^2}\right)\exp(\alpha L) - V_{bi,\,s\text{-}Si} - V_{DS}\right] \\ &\times[\exp(\alpha L) - \exp(-\alpha L)]^{-1}, \end{aligned} \tag{37}$$

$$C = A\exp(\alpha L_1) + \frac{\beta_2 - \beta_1}{2\alpha^2}, \tag{38}$$

$$D = B\exp(-\alpha L_1) + \frac{\beta_2 - \beta_1}{2\alpha^2}, \tag{39}$$

$$E = \left[\frac{\beta_4 - \beta_3}{2\alpha^2}\exp(\alpha L_2) + \frac{\beta_4 - \beta_3}{2\alpha^2}\exp(-\alpha L_2) - \frac{\beta_4}{\alpha^2} + \left(V_{\text{bi,s-Si}} + \frac{\beta_3}{\alpha^2}\right)\exp(-\alpha L) - V_{\text{bi,s-Si}} - V_{\text{DS}}\right] \times \left[\exp(-\alpha L) - \exp(\alpha L)\right]^{-1}, \tag{40}$$

$$F = \left[\frac{\beta_4 - \beta_3}{2\alpha^2}\exp(\alpha L_2) + \frac{\beta_4 - \beta_3}{2\alpha^2}\exp(-\alpha L_2) - \frac{\beta_4}{\alpha^2} + \left(V_{\text{bi,s-Si}} + \frac{\beta_3}{\alpha^2}\right)\exp(\alpha L) - V_{\text{bi,s-Si}} - V_{\text{DS}}\right] \times \left[\exp(\alpha L) - \exp(-\alpha L)\right]^{-1}, \tag{41}$$

$$G = E\exp(\alpha L_1) + \frac{\beta_4 - \beta_3}{2\alpha^2}, \tag{42}$$

$$H = F\exp(-\alpha L_1) + \frac{\beta_4 - \beta_3}{2\alpha^2}. \tag{43}$$

The minimum potential of the front-channel and back-channel can be calculated from Eqs. (32)–(35) as

$$\phi_{\text{s1, min}} = 2\sqrt{AB} - \frac{\beta_1}{\alpha^2}, \tag{44}$$

$$\phi_{\text{s2, min}} = 2\sqrt{CD} - \frac{\beta_2}{\alpha^2}, \tag{45}$$

$$\phi_{\text{b1, min}} = 2\sqrt{EF} - \frac{\beta_1}{\alpha^2}, \tag{46}$$

$$\phi_{\text{b2, min}} = 2\sqrt{GH} - \frac{\beta_4}{\alpha^2}. \tag{47}$$

The minimum occurs at

$$x_{\text{min, f1}} = \frac{1}{2\alpha}\ln\frac{B}{A}, \tag{48}$$

$$x_{\text{min, f2}} = \frac{1}{2\alpha}\ln\frac{D}{C}, \tag{49}$$

$$x_{\text{min, b1}} = \frac{1}{2\alpha}\ln\frac{E}{F}, \tag{50}$$

$$x_{\text{min, b2}} = \frac{1}{2\alpha}\ln\frac{G}{H}. \tag{51}$$

The electric field pattern along the channel determines the electron transport velocity through the channel. The electric field horizontal components under the front gates and back gate are given as

$$E_{1,\text{f}}(x) = A\alpha\exp(\alpha x) - B\alpha\exp(-\alpha x), \tag{52}$$

$$E_{2,\text{f}}(x) = C\alpha\exp\left[\alpha(x - L_1)\right] - D\alpha\exp\left[-\alpha(x - L_1)\right], \tag{53}$$

$$E_{1,\text{b}}(x) = E\alpha\exp(\alpha x) - F\alpha\exp(-\alpha x), \tag{54}$$

$$E_{2,\text{b}}(x) = G\alpha\exp\left[\alpha(x - L_1)\right] - H\alpha\exp\left[-\alpha(x - L_1)\right]. \tag{55}$$

3.2. Two-dimensional model for threshold voltage

The threshold voltage V_{TH} is the value of the gate voltage V_{GS} at which a conducting channel of an SOI MOSFET is induced. In a fully depleted thin film SOI, it is desirable that the front channel turns on before the back channel. Therefore, the threshold voltage is taken to be that value of gate source voltage for which $\phi_{\text{s1, min}} = 2\phi_{\text{F, Si}}$, where $\phi_{\text{F, Si}}$ is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level. For the strained-Si SOI MOSFET, the threshold condition under the front gate is modified as[9,10]

$$\phi_{\text{s, min}} = 2\phi_{\text{F, Si}} + \Delta\phi_{\text{s-Si}} = \phi_{\text{th}}, \tag{56}$$

where

$$\Delta\phi_{\text{s-Si}} = -\frac{(\Delta E_{\text{g}})_{\text{s-Si}}}{q} + V_{\text{T}}\ln\frac{N_{\text{V, Si}}}{N_{\text{V, s-Si}}}.$$

ϕ_{th} is the value of surface potential at which the volumetric inversion electron charge density in the strained-Si device is the same as that in the unstrained-Si at threshold, i.e., equal to the body doping.

For an FD asymmetrical DMG DG structure, because of the different metal material M1 and M2, the threshold voltage is defined as the value of V_{GS} in which the minimum between of the maximum of the front channel surface potential $\phi_{\text{s1, min}}$ and $\phi_{\text{s2, min}}$ equals ϕ_{th}, and the maximum of the back channel surface potential $\phi_{\text{b1,min}}$ and $\phi_{\text{b1,min}}$ equals ϕ_{th}. Hence, one can determine the value of the threshold voltage as the value of V_{GS} by solving Eqs. (44)–(47).

The front gate threshold voltages can be expressed as

$$V_{\text{TH, f1}} = \frac{qNA}{\varepsilon_{\text{si}}\alpha^2} - \frac{-b_{\text{f1}} + \sqrt{b_{\text{f1}}^2 - 4a_{\text{f1}}c_{\text{f1}}}}{2a_{\text{f1}}} + (V_{\text{FB1, f}})_{\text{s-Si}}, \tag{57}$$

$$V_{\text{TH, f2}} = \frac{qNA}{\varepsilon_{\text{si}}\alpha^2} - \frac{-b_{\text{f2}} + \sqrt{b_{\text{f2}}^2 - 4a_{\text{f2}}c_{\text{f2}}}}{2a_{\text{f2}}} + \frac{(V_{\text{FB1, f}})_{\text{s-Si}} + (1 + a_1)(V_{\text{FB2,f}})_{\text{s-Si}}}{2 + a_1}, \tag{58}$$

where

$$a_{\text{f1}} = 2 - \eta - \frac{h}{4},$$

$$b_{\text{f1}} = -Z - Y + m + \frac{V_1}{\alpha^2}(2 - \eta) - \frac{h}{2}\phi_{\text{th}},$$

$$c_{\text{f1}} = W_1 - \frac{h}{4}\phi_{\text{th}}^2 h = 2 - \exp(2\alpha L) - \exp(-2\alpha L),$$

$$W_1 = ZY - (Z + Y)\frac{V_1}{\alpha^2} + \frac{V_1^2}{\alpha^4},$$

$$Z = \frac{V_1}{2\alpha^2}\left[\exp(\alpha L_2) + \exp(-\alpha L_2)\right] + V_{\text{bi, s-Si}}\exp(-\alpha L) - V_{\text{bi, s-Si}} - V_{\text{DS}},$$

$$Y = \frac{V_1}{2\alpha^2}\left[\exp(\alpha L_2) + \exp(-\alpha L_2)\right] + V_{\text{bi, s-Si}}\exp(\alpha L) - V_{\text{bi, s-Si}} - V_{\text{DS}},$$

$$\eta = \left[\exp(\alpha L) + \exp(-\alpha L)\right] m = Z\exp(\alpha L) + Y\exp(-\alpha L),$$

$$a_{\text{f2}} = 2 - \eta - \frac{h}{4},$$

$$b_{f2} = -Z - Y + m + \frac{V_1}{\alpha^2}\eta - \frac{2V_1}{\alpha^2} + h\frac{V_1}{2\alpha^2} - \frac{h}{2}\phi_{th},$$

$$c_{f2} = W_2 - \frac{h}{4}\phi_{th}^2,$$

$$W_2 = ZY - \frac{V_1}{\alpha^2}m + \frac{V_1^2}{\alpha^4} + K\frac{V_1}{2\alpha^2}n + \frac{V_1^2}{2\alpha^4}\left[\exp(\alpha L_2) - \exp(-\alpha L^2)\right] + h\frac{V_1^2}{4\alpha^4}$$

$$V_1 = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{1 + a_1}{t_f t_{si}\left(1 + \frac{1}{2}a_1\right)}\Delta\phi_M,$$

$$n = Z\exp(\alpha L_1) - Y\exp(-\alpha L_1),$$

$$\Delta\phi_M = \phi_{M2} - \phi_{M1},$$

$$K = \exp(\alpha L) - \exp(-\alpha L).$$

So the front gate threshold voltage is the maximum of the front channel threshold voltage,

$$V_{TH,f} = \max[V_{TH,f1}, V_{TH,f2}]. \tag{59}$$

The back gate threshold voltage can be expressed as

$$V_{TH,b1} = \frac{qNA}{\varepsilon_{si}\alpha^2} - \frac{-b_{b1} + \sqrt{b_{b1}^2 - 4a_{b1}c_{b1}}}{2a_{b1}} + (V_{FB1,f})_{s\text{-}Si}, \tag{60}$$

$$V_{TH,b2} = \frac{qNA}{\varepsilon_{si}\alpha^2} - \frac{-b_{b2} + \sqrt{b_{b2}^2 - 4a_{b2}c_{b2}}}{2a_{b2}} + \frac{(V_{FB2,f})_{s\text{-}Si} + (1 + a_1)(V_{FB1,f})_{s\text{-}Si}}{2 + a_1}, \tag{61}$$

where

$$a_{b1} = 2 - \eta - \frac{h}{4},$$

$$b_{b1} = -Z - Y + m + \frac{V_2}{\alpha^2}(2 - \eta) - \frac{h}{2}\phi_{th},$$

$$c_{b1} = W_3 - \frac{h}{4}\phi_{th}^2,$$

$$V_2 = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\Delta\phi M}{t_f t_{si}\left(1 + \frac{1}{2}a_1\right)},$$

$$W_3 = ZY - (Z + Y)\frac{V_2}{\alpha^2} + \frac{V_2^2}{\alpha^4},$$

$$a_{b2} = \left(2 - \eta - \frac{h}{4}\right)b_{b2} = -Z - Y + m + \frac{V_2}{\alpha^2}\eta - \frac{2V_2}{\alpha^2} + h\frac{V_2}{2\alpha^2} - \frac{h}{2}\phi_{th},$$

$$b_{b2} = -Z - Y + m + \frac{2V_2}{\alpha^2} + \frac{V_2}{\alpha^2}\eta + \frac{V_2}{2\alpha^2}h - \frac{h}{2}\phi_{th},$$

$$c_{b2} = W_4 - \frac{h}{4}\phi_{th}^2,$$

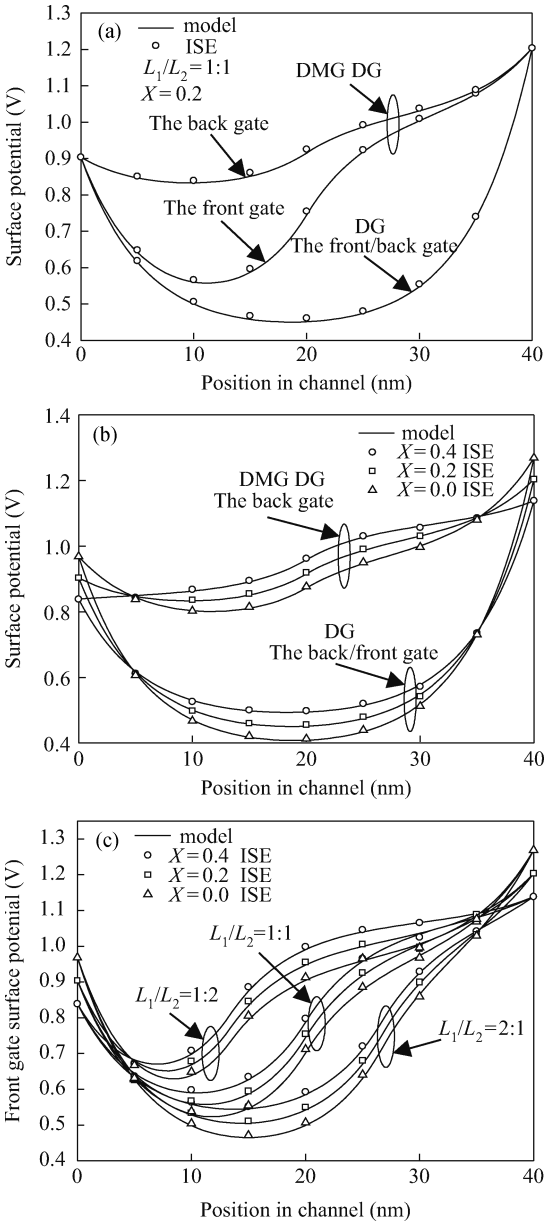

Fig. 2. Variation in the surface potential along the channel for the 40 nm DMG DG and DG strained-Si MOSFET. (a) Potential distribution of the front gate and back gate surface of the DMG DG and DG MOSFETs. (b) Potential distribution of the back gate surface of the DMG DG and DG MOSFETs. (c) Potential distribution of the front gate surface of the DMG DG MOSFETs.

$$W_4 = ZY - \frac{V_2}{\alpha^2}m + \frac{V_2^2}{\alpha^4} + K\frac{V_2}{2\alpha^2}n + \frac{V_2^2}{2\alpha^4}\left[\exp(\alpha L_2) - \exp(-\alpha L_2)\right] + h\frac{V_2^2}{4\alpha^4}.$$

So the back gate threshold voltage is the maximum of the back channel threshold voltage,

$$V_{TH,b} = \max[V_{TH,b1}, V_{TH,b2}]. \tag{62}$$

So the threshold voltage is the minimum of the front channel threshold voltage and the back channel threshold voltage,

$$V_{TH} = \min[V_{TH,f}, V_{TH,b}]. \tag{63}$$

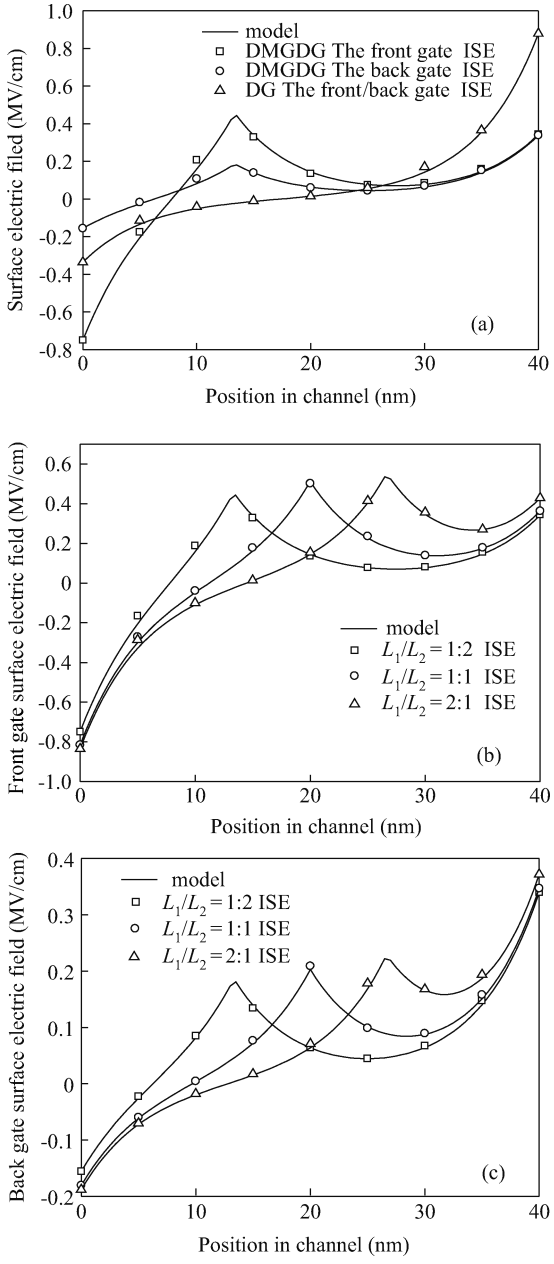

Fig. 3. Variation in the surface electric field within the channel for the 40 nm DMG DG and DG MOSFETs. (a) Surface electric field distribution of the front gate and the back gate surface of the DMG DG and DG MOSFETs. (b) Surface electric field distribution of the front gate of the DMG DG and DG MOSFETs. (c) Surface electric field distribution of the back gate of the DMG DG and DG MOSFETs.

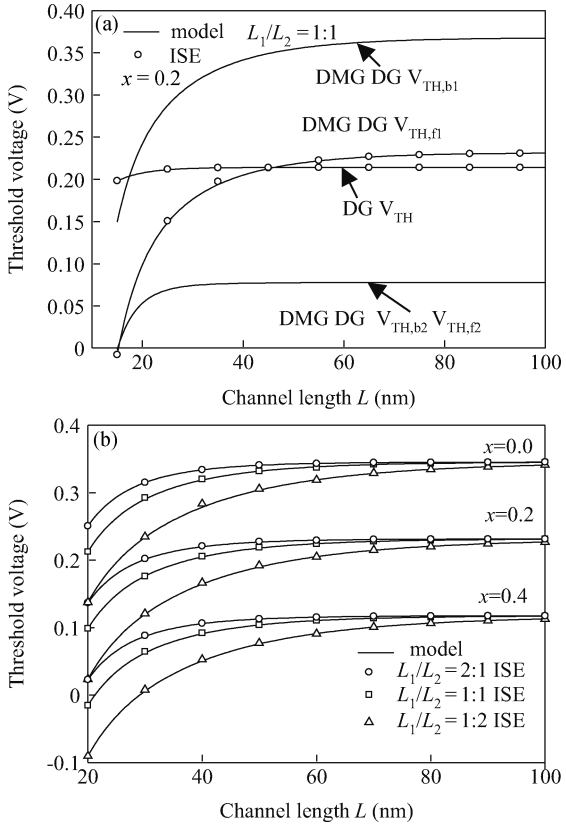

Fig. 4. Variation in threshold voltage along the channel for 100 nm DMG DG and DG MOSFETs. (a) Threshold voltage of DMG DG and DG MOSFETs. (b) Threshold voltage of DMG DG MOSFET changes with the gate length ratio and strain X.

4. Results and discussion

To verify the proposed analytical model, an FD n-channel asymmetry DMG DG structure, as shown in Fig. 1(a), was used. Typical values of the work function for gate metals M1 and M2 are chosen as 4.70 eV and 4.35 eV, respectively. t_f = 2 nm, $t_{s\text{-}Si}$ = 10 nm, $N_A = 1 \times 10^{17}$ cm^{-3}.

In the following figures, the lines represent the results from the derived analytical models, and the symbols represent those from ISE.

Figure 2(a) shows the curve of the front gate surface potential and the back gate surface potential of the DMG DG strained-Si MOSFET and the front/back surface potential of the DG strained-Si MOSFET against the horizontal distance in the channel for L = 40 nm. It is clearly seen that the DMG DG structure exhibits a step function in the surface potential along the channel. Due to this unique feature, the area under M1 ploy front gate of the DMG structure is essentially screened from the drain-potential variations. This means that the drain-potential has very little effect on the drain current after saturation reducing the DIBL. Figure 2(b) shows the variation in the back gate surface potential of the DMG DG strained-Si MOSFET and the variation in the surface potential of the DG strained-Si MOSFET with the values of the effective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer. At the source and drain end, the surface potential decreases with an increase in the values of the effective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer. However, in the middle of the channel there is an increase in the potential barrier with increasing values of the effective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer. Figure 2(c) shows the variation in the front gate surface potential of the DMG DG strained-Si MOSFET with the values of the effective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer and the gate length ratio (L_1/L_2). As the gate length ratio decreases, the step change of the potential moves toward the source end. We can see that at the source and drain end the surface potential decreases with increasing values of the effective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer. However, in the middle of the channel, the potential barrier increases with increasing values of the ef-

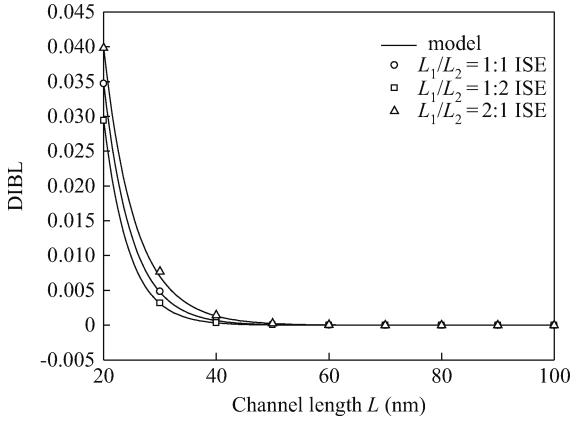

Fig. 5. Drain induced barrier lowing (DIBL) versus channel length L.

fective Ge mole fraction in the relaxed $Si_{1-x}Ge_x$ buffer.

Figure 3(a) shows the variation in the front gate and back gate electric field of the DMG DG and DG strained-Si MOSFET along the normalized channel portion with the gate length L = 40 nm. There is a peak electric field at the interface of M1 and M2 within the channel of the DMG DG MOSFET, and it accelerates the carrier transit speed. Figures 3(b) and 3(c) show the variation in the front gate and back gate electric field of the DMG DG strained-Si MOSFET with the gate length ratio. It can be seen that the peak electric field moves toward the source side as the gate length ratio decreases.

Figure 4(a) shows the variation in threshold voltage of the DMG DG and the DG strained-Si MOSFET with the gate length. It is observed that SCE become serious with decreasing channel length. Figure 4(b) shows the variation in threshold voltage with the gate length for different Ge mole fractions. It is observed that the threshold voltage is lower for higher strain in the silicon film and small gate length ratio (L_1/L_2) for a given channel length. The change with increasing Ge content x is due to the decrease in the flatband voltage, the decrease in the built-in potential barrier, and an earlier onset of inversion due to a decrease in ϕ_{th}.

Figure 5 shows the variation in DIBL with channel length ratio for x = 0.2 Ge mole fraction for the DMG DG strained-Si MOSFET. The DIBL is obtained from the difference between the threshold voltage at high drain–drain source voltage (V_{ds} = 0.5 V) and the threshold voltage value at low drain–drain source voltage (V_{ds} = 0.05 V). It is observed that DIBL is significant for small channel lengths (40–50 nm), while it is negligible for longer channel lengths.

5. Conclusion

Based on the two-dimensional solution of Poisson's equation, the analytical model for asymmetrical DMG DG strained-Si MOSFET comprising surface potential, surface electric field and threshold voltage has been developed. It has been shown that the FD asymmetrical DMG DG strained-Si MOSFET reduces SCE and DIBL. The obtained results are in good agreement with the simulation results.

References

[1] Frank D J, Dennard R H, Nowak E, et al. Device scaling limits of Si MOSFET's and their application dependencies. Proc IEEE, 2001, 89(3): 259
[2] Venkatesan S, Neudeck G W, Pierret R F. Dual-gate operation and volume inversion in n-channel SOI MOSFET's. IEEE Electron Device Lett, 1992, 13(1): 44
[3] Djeffal F, Meguellati M, Benhaya A. A two-dimensional analytical analysis of subthreshold behavior to study the scaling capability of nanoscale graded channel gate stack DG MOSFETs. Physica E, 2009, 41(8): 1872
[4] Kumar M J, Chaudhry A. Two-dimensional analytical modeling of fully depleted DMG SOI MOSFET and evidence for diminished SCEs. IEEE Trans Electron Devices, 2004, 51(4): 569
[5] Chiage T K, Chen M L. A new analytical threshold voltage model for symmetrical double-gate MOSFETs with high-k gate dielectrics. Solid State Electron, 2007, 51(3): 387
[6] Goel K, Saxena M, Gupta M, et al. Two-dimensional analytical threshold voltage model for DMG epi-MOSFET. IEEE Trans Electron Devices, 2005, 52(1): 23
[7] Li J, Liu H X, Li B, et al. Two-dimensional threshold voltage analytical model of DMG strained-silicon-on-insulator MOSFETs. Journal of Semiconductors, 2010, 31(8): 084008
[8] Yin H Z, Hobart K D, Peterson R L. Ultrathin strained-SOI by stress balance on compliant substrates and FET performance. IEEE Trans Electron Devices, 2005, 52(10): 2207
[9] Mizuno T, Sugiyama N, Kurobe A, et al. Advance SOI p-MOSFETs with strained-Si channel on SiGe-on-insulator substrate fabricated by SIMOX technology. IEEE Trans Electron Devices, 2001, 48(10): 1612
[10] Zhou X. Exploring the novel characteristics of hetero-material gate field-effect transistors (HMGFETs) with gate material engineering. IEEE Trans Electron Devices, 2000, 47(1): 113
[11] Venkataraman V, Nawal S, Kumar M J. Compact analytical threshold-voltage model of nanoscale fully depleted strained-Si on silicon-germanium-on-insulator (SGOI) MOSFETs. IEEE Trans Electron Devices, 2007, 54(3): 554
[12] Kumar M J, Venkataraman V, Nawal S. A simple analytical threshold voltage model of nanoscale single-layer fully depleted strained-silicon-on-insulator MOSFETs. IEEE Trans Electron Devices, 2006, 53(3): 2500
[13] Yong K K. Short-channel effect in fully depleted SOI MOSFETs. IEEE Trans Electron Devices, 1989, 36(2): 399
[14] Sharma R K, Gupta M, Gupta R S. Two-dimensional analytical subthreshold model of graded channel DG FD SOI n-MOSFET with gate misalignment effect. Superlattices and Microstructures, 2009, 45(1): 91
[15] Rim K, Anderson R, Boyd D. Strained Si CMOS (SS CMOS) technology: opptunities and challenges. Solid State Electron, 2003, 47(7): 1133
[16] Yang L F, Watling J R. Si/SiGe heterostructure parameters for device simulations. Semicond Sci Technol, 2004, 19(8): 1174