Simple and low-cost fabrication of a metal nanoplug on various substrates by electroless deposition*

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Abstract: An electroless deposition (ELD) method is introduced to fabricate a metal nanoplug for its advantages of simplicity, low cost and auto-selectivity. It was demonstrated that nanoplugs of less than 50 nm in diameter can be fabricated by ELD nickel on various substrates, such as silicon, tungsten and titanium nitride. The main composition of the ELD nanoplug was characterized as nickel by an energy dispersive X-ray microanalyzer. A functional vertical phase-change random access memory (PCRAM) device with a heater diameter of around 9 μm was fabricated by using the ELD method. The I–V characteristics demonstrated that the threshold current is only 90.8 μA. This showed that the ELD process can satisfy the demands of PCRAM device application, as well as device performance improvement. The ELD process provides a promising method for the simple and low-cost fabrication of metal nanoplugs.

Key words: electroless deposition; nanoplug; anodic aluminum oxide template
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1. Introduction

One-dimensional (1D) nanostructures, such as nanowires, nanorods and nanotubes, have become the research hotspots for the assembly of electronic, photonic and magnetic devices[1−3]. Recently, the metal nanoplug has become particularly interesting due to the device performance improvement caused by its dimensions and it has been widely applied in various devices[4], especially in memory devices, such as phase-change random access memory (PCRAM)[5−7] and resistance random access memory (RRAM)[8]. For PCRAM application, many methods have been developed to fabricate the metal nanoplug and reduce its dimensions, such as utilizing a doped germanium (Ge) nanowire pn-junction diode as a heater[5], developing advanced ring type technology[6], and fabricating a 50 nm bottom electrode heater pillar by lithography[7].

Current technologies for fabricating 1D nanostructures mainly include physical vapor deposition (PVD)[9], chemical vapor deposition (CVD)[3], pulse laser deposition (PLD)[10], sputter deposition[11], electron-beam evaporation[12], atomic-layer deposition (ALD)[4], electrodeposition (ED)[1]and electroless deposition (ELD)[13]. However, all of these methods except for the ED method are non-selective where metal is deposited everywhere. A process such as etching or chemical mechanical planarization (CMP) are needed. The ED method offers selectivity, but the substrate should be conductive to serve as a cathode, which limits its application.

ELD is one of the preferred methods for 1D nanostructure fabrication because of several distinct advantages. First, the method is a simple, low-cost process and allows for wafer scale application. The ELD method is well known as an autocatalytic process that is carried out through the redox reaction of an oxidizer and a reductant in an electrolyte solution. Secondly, it is a kind of selective deposition method. Without special treatment, ELD generally only happens on an "active" surface, such as metal, while on the "inert" surface, such as SiO_2, SiN or other insulating materials, ELD cannot proceed. Thirdly, ELD shows excellent via filling ability. It has been reported that it can be used to fabricate a metallic nanowire through an anodic aluminum oxide (AAO) template[13]. Recently, it has been reported that the barrier layer in the Damascene Cu process can also be fabricated by using the ELD method[14]. Furthermore, Shingubara[15] reported direct ELD fabrication of a Damascene Cu interconnection on a tantalum nitride (TaN) barrier layer with a via diameter of 100 nm.

Although the ELD method has been used for the preparation of a Damascene Cu interconnection, which can be considered as a Cu nanoplug on a TaN substrate, there has been no report on the fabrication of other metal nanoplugs on various substrates. Here, the ELD method was used to fabricate

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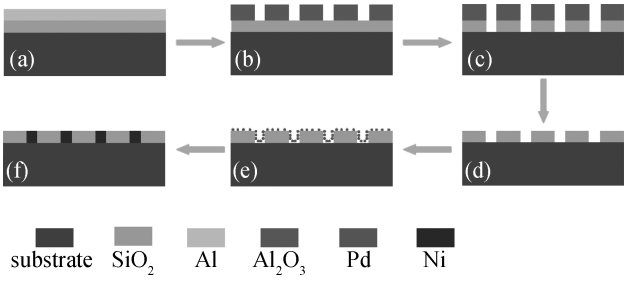


Fig. 1. Schematic process for metal nanoplug fabrication. (a) Al and SiO_2 deposition, the substrate can be Si, W/Si or TiN/Si. (b) Formation of AAO template by two-step anodization. (c) Dry etching of SiO_2. (d) Chemical dissolution of AAO template. (e) Activation of the surface before deposition and (f) ELD Ni.

a nickel (Ni) nanoplug. It is well known that for modern microelectronics, Ni is one of the most important materials that can serve as an ohmic contact. To demonstrate the flexibility of this method, metal nanoplugs have been fabricated on silicon (Si) substrate, tungsten (W) substrate and titanium nitride (TiN) substrate. Furthermore, we have demonstrated a functional vertical PCRAM device with a heater diameter of around 9 μm by using the ELD method without the CMP process. Our process can lead to simple and low-cost fabrication of metal nanoplugs.

2. Experiment

Figures 1(a)–1(f) show the process flow diagrams of our process. First, 100 nm SiO_2 was deposited on a substrate by plasma-enhanced chemical vapor deposition (PECVD) at 300 ℃ as the dielectric layer. Then a 1.5 μm aluminum (Al) film was deposited on the SiO_2 layer by magnetron sputtering, as shown in Fig. 1(a). The substrate can be Si, W or TiN. After that, a 500 nm nanoporous AAO template as the etching mask was formed by two-step anodic oxidation (Fig. 1(b)). Then the deposited SiO_2 was patterned by an inductively coupled plasma (ICP) dry etch (STS multiplex AOE system), resulting in the vias opening, as shown in Fig. 1(c). After this step, the AAO template was dissolved in order to reveal the ordered nanoporous array of SiO_2 (Fig. 1(d)). After the vias opening, the wafer was first cleaned and immersed in an aqueous solution of $SnCl_2$ (10 g/L) for 1 min at room temperature. Then the wafer was washed with deionized water 2 or 3 times and kept in an aqueous solution of $PdCl_2$ (1 g/L) for 30 s at room temperature. Next the wafer was rinsed with deionized water 2 or 3 times again (Fig. 1(e)). Finally, Ni nanoplugs were deposited from a solution of 15 g/L $NiSO_4{\cdot}6H_2O$, 22 g/L $NaH_2PO_2{\cdot}H_2O$, and 40 g/L sodium citrate at 80 ℃ with stirring (Fig. 1(f)). Because of the selectivity of the ELD method, Ni deposition starts on the substrate instead of SiO_2, and, as a result, Ni generally fills the vias and metal nanoplugs can be obtained without an additional CMP process.

The experimental procedures of the nanoscale AAO template with 500 nm in thickness formatted by two-step anodic oxidation are as follows. First, the wafer with 1500 nm Al was soaked in 0.3 mol/L oxalic acid aqueous solution with a water bath at 15 ℃ and anodized at a constant voltage of 40 V for 15 min. Then the wafer was dipped in the mixed solution (6% phosphoric acid and 1.8% chromic acid) at 60 ℃ for 5 min

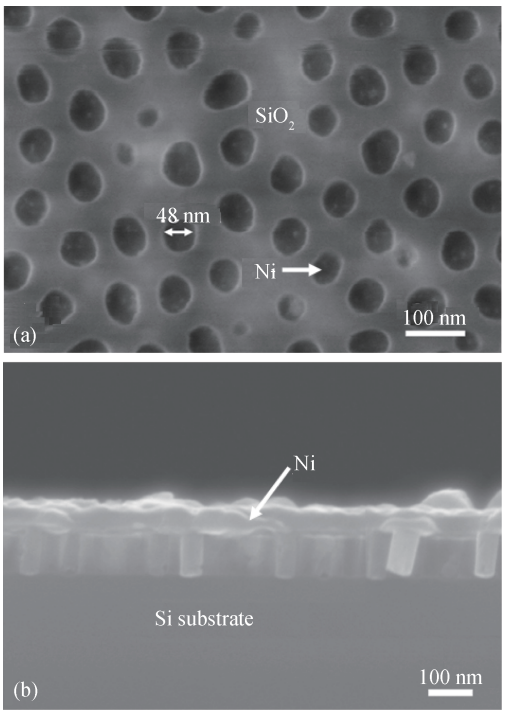


Fig. 2. (a) Top view SEM image of an ELD Ni nanoplug on Si substrate. (b) Cross-sectional SEM image of an ELD Ni nanoplug on Si substrate.

35 s to remove the first porous anodic aluminum film. Subsequently, the two-step anodic oxidation was carried out under the same conditions. The aluminum film was completely anodized until the direct current fell to 0 V. Finally, the wafer was immersed in 5% phosphoric acid for 15 min 30 s at 30 ℃ to remove the barrier layer under the pores of the AAO template.

To characterize the result of the ELD process, a Hitachi S4800 scanning electron microscope (SEM) was used. The composites were also calibrated by a Horiba energy dispersive X-ray microanalyzer (EDXM). The I–V characteristics of the vertical PCRAM device were tested by using an Agilent B1500A semiconductor device analyzer at room temperature.

3. Results and discussion

Figure 2(a) shows a top view SEM image of ELD Ni nanoplugs on a Si substrate. In Fig. 2(a) it can be seen that the nanoscale vias are filled selectively by the ELD Ni, but there is no Ni deposition on the SiO_2 surface. The reason is that the ELD solution is added by bias (3-sulfopropyl) disulfide (SPS) with a very small amount that can accelerate Ni growth inside the vias. So there is no need for the CMP process compared with common CMP-based processes. To further demonstrate the filling ability of the ELD Ni, a sample was also prepared in the ELD solution without adding SPS. Figure 2(b) shows the corresponding cross-sectional SEM image. Figure 2(b) shows that all of the nanoscale vias are filled completely on the Si substrate while on the SiO_2 surface there is also Ni deposition for the lack of SPS in the ELD solution. Although Figure 2(b) shows that the ELD time is a little excessive, it can demonstrate the good filling ability of the nanoscale vias of our ELD

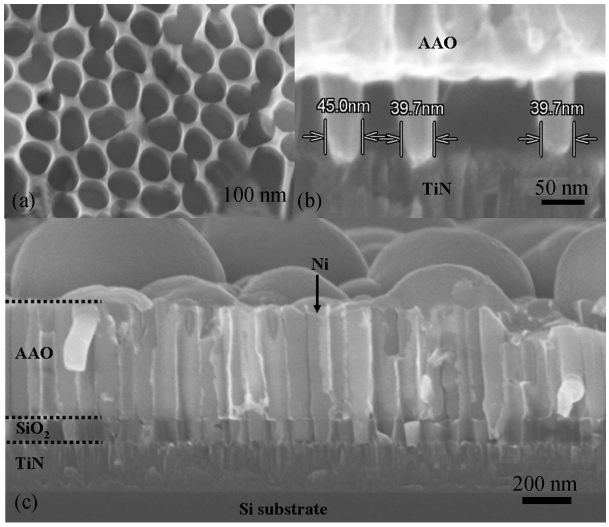


Fig. 3. (a) Top view SEM image of an ELD Ni nanoplug on TiN substrate. (b) Cross-sectional SEM image of an ELD Ni nanoplug on TiN substrate. (c) Full view cross-sectional SEM image of an ELD Ni nanoplug on TiN substrate.

method. Therefore, ELD Ni demonstrates a good filling ability for nanoscale vias.

Figures 3(a)–3(c) show a top view SEM image, a cross-sectional SEM image and a full view cross-sectional SEM image of ELD Ni nanoplugs on a TiN substrate. After dry etching of SiO_2, the AAO template is not dissolved in this experiment, because the acid solution that removes the AAO template can etch TiN. In Fig. 3(a) it can be seen that not only the ordered nanoporous array of SiO_2, but the nanoscale AAO film can also be covered by ELD Ni. Figures 3(b) and 3(c) show that despite a 14 : 1 aspect ratio (the depth of AAO film is 460 nm and that of SiO_2 is 100 nm), all of the nanoscale vias are filled completely. In Fig. 3 it can be seen that ELD Ni can fill the vias with even less than 40 nm in diameter on TiN substrate through 460 nm AAO film.

Figure 4(a) shows a top view SEM image of ELD Ni nanoplugs on the test structure with a via diameter of 90 nm by using a standard CMOS process for PCRAM application. Figure 4(b) is the SEM image with high magnification, and it shows that there are three different filling results: fully filled via, via with small hole and via with big hole. The statistical chart is shown based on SEM images taken from 60 vias. It shows that 57% are fully filled, and the remaining 43% are with a small or big hole. According to this result, the ELD method shows promising via filling ability. Figure 4(c) shows a top view SEM image of ELD Ni nanoplugs in nanoporous alumina film on W substrate, which has a smaller diameter and bigger aspect ratio compared to the above PCRAM structure. Further, it can be seen that despite the 10 : 1 aspect ratio (via depth 500 nm), via with a diameter of around 50 nm can also be filled completely.

Figure 5 shows EDXM results of ELD Ni nanoplugs on a Si substrate. From the embedded table, it can be seen that the atom percentages of Si, P and Ni are 63.24, 4.15 and 32.61, respectively. The large atom percentage of Si is caused by the Si substrate. Ni comes from the oxidizer of Ni sulfate hexahydrate, while P is from the reductant of sodium hypophosphite.

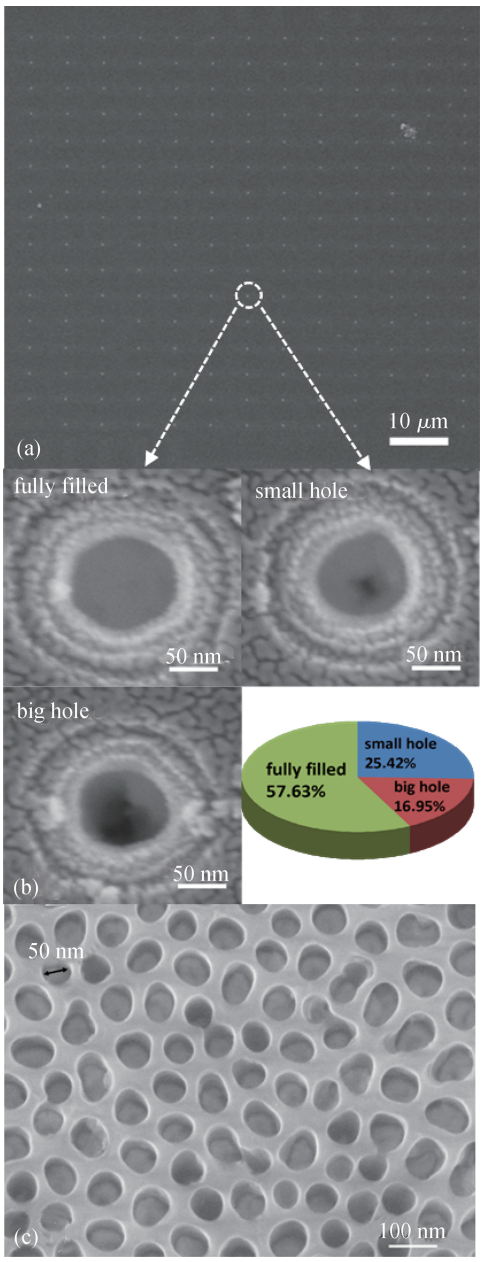
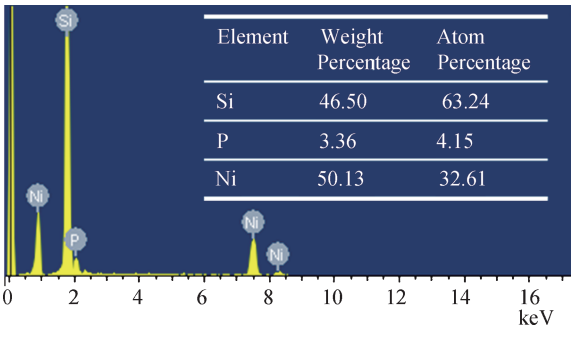


Fig. 4. (a) Top view SEM image of an ELD Ni nanoplug on W substrate in a test structure with a via size of 90 nm. (b) Top view SEM images and statistical chart of different filling results. (c) Top view SEM image of an ELD Ni nanoplug through an AAO template on W substrate. A thin layer of gold was sputtered on the surface before SEM observing in (a) and (b).



Element	Weight Percentage	Atom Percentage
Si	46.50	63.24
P	3.36	4.15
Ni	50.13	32.61

Fig. 5. EDXM results of an ELD Ni nanoplug on Si substrate.

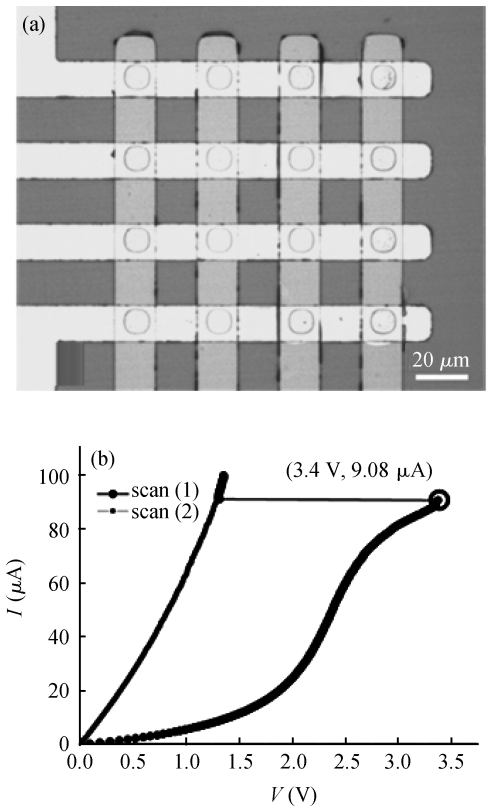


Fig. 6. (a) Microscope image of a vertical PCRAM device with an ELD Ni plug. (b) I–V characteristics of a vertical PCRAM device with an ELD Ni plug.

The atom proportion of Ni to P is calculated as about 8. The bigger the atom proportion of Ni to P, the better the quality of Ni due to the lower melting point of P.

From the above results, it is clear that the ELD method shows a good filling ability for nanoscale via. But to explore whether the ELD process can satisfy the demands of device applications where a metal nanoplug is needed, we fabricated a vertical PCRAM device with a heater diameter of around 9 μm by using the ELD method without an additional CMP process. In our PCRAM device, the phase change material is magnetron sputtered $Ge_2Sb_2Te_5$ (GST) and an ELD Ni plug is on W bottom electrode.

Figure 6(a) shows a microscope image of our vertical PCRAM device with a heater diameter of around 9 μm, and Figure 6(b) shows the I–V characteristics of the vertical PCRAM device with an ELD Ni plug. As the key feature of the PCRAM device, an S-shape negative differential resistance curve was successfully demonstrated. The threshold voltage ($V_{\rm th}$) is defined by the point where the negative differential resistance appears with increasing current. For our device, the threshold voltage is about 3.4 V, and the current is about 90.8 μA when the device is switched on. The DC power consumption is about 308.72 μW. It is worth noting that despite the large heater size (9 μm), the threshold current of our device is only 90.8 μA, which shows that the ELD fabricated Ni plug is promising to reduce the RESET current.

To give a comprehensive understanding of whether the ELD Ni is capable of PCRAM application, the physical characteristics of ELD Ni are summarized and compared with W and GST in Table 1. It should be noted that, to our knowledge, there are no reported data on the resistivity of ELD Ni. The value cited in Table 1 is from CoWBP, which is a similar material to ELD Ni. In fact, both ELD Ni and CoWBP can serve as a barrier material for the Damascene Cu interconnection[14]. From the table, it can be concluded that the resistivity of ELD Ni is larger than crystallized GST, but much smaller than amorphous GST. It should also be pointed out that the resistivity difference between ELD Ni and crystallized GST is not so large. Therefore, the thermal generation efficiency in GST can be preserved. On the other hand, the thermal conductivity of ELD Ni is about 40 times smaller than that of W, which probably means that the thermal loss through the heater of ELD Ni is 40 times less than the device with a W heater. This could be the reason why the threshold current of our device with a heat diameter of 9 μm is only 90.8 μA.

Table 1. Physical characteristic summary of ELD Ni and PCRAM related materials.

Material	Thermal conductivity (W/(m·K))	Resistivity ($\mu\Omega$·cm)
ELD Ni	4.41–5.67[16]	20–32[14]
W	174	10^{-3}
Amorphous GST	0.24	10^{5}
Crystallized GST	0.28	1

From the above results, it is clear that the ELD process for metal plug fabrication can not only provide great advantages, such as simplicity, low cost and functionability, but also satisfy the demands of device applications where a metal nanoplug is needed.

In the experiment, we used an alkalescent electrolyte solution with sodium hypophosphite as the reductant because it's a general recipe for the ELD process. However, alkali ions contained in the electrolyte solution make it incompatible with current CMOS technologies. However, this problem can be solved thoroughly by choosing alkali ion-free electrolyte solution[17]. Moreover, the melting point of ELD Ni can be improved to around 700 ℃ or 800 ℃ if boron-containing reductant is used[16]. In addition, if hydrazine (N_2H_4)-containing reductant is used, pure Ni can be obtained[18]. Therefore, the thermal stability of ELD Ni can be good enough to meet the demands of device application.

4. Conclusion

In summary, we have introduced the ELD method to fabricate metal nanoplugs. It was demonstrated that the metal nanoplugs with less than 50 nm in diameter on Si substrate, TiN substrate and W substrate can be easily fabricated by the ELD Ni process. The main composition of the ELD Ni nanoplug on Si substrate has been determined to be Ni by EDXM. Finally, we successfully demonstrated a functional vertical PCRAM device with a heater diameter of around 9 μm by using the ELD method without an additional CMP process. The I–V characteristics show that the ELD fabricated Ni plug is promising to improve device performance. Therefore, our ELD process has great potential for the simple and low-cost fabrication of metal nanoplugs for the device applications.

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