Finite element simulation of hydrostatic stress in copper interconnects*

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Abstract: This work focuses on numerical modeling of hydrostatic stress, which is critical to the formation of stress-induced voiding (SIV) in copper damascene interconnects. Using three-dimensional finite element analysis, the distribution of hydrostatic stress is examined in copper interconnects and models are based on the samples, which are fabricated in industry. In addition, hydrostatic stress is studied through the influences of different low-k dielectrics, barrier layers and line widths of copper lines, and the results indicate that hydrostatic stress is strongly dependent on these factors. Hydrostatic stress is highly non-uniform throughout the copper structure and the highest tensile hydrostatic stress exists on the top interface of all the copper lines.

Key words: copper interconnects; hydrostatic stress; stress-induced voiding; finite element method

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1. Introduction

Due to the development of fabrication techniques in ultra large scale integrated circuits, the feature size of microelectronic devices has become smaller and the density of circuits higher, which has resulted in resistance–capacitance (RC) time delays and heavier failures. Copper (Cu) has been replacing aluminum (Al) as the metallization of choice for reduced RC delay in high-performance circuits[1]. In the meantime, the reliability of copper interconnects is deeply concerning.

Stress-induced voiding (SIV) is the most important intrinsic failure mechanism in copper interconnects. It has been found that large amount of stress builds up as a result of the difference in coefficients of thermal expansion (CTE) between metal lines and the surrounding dielectrics[2]. Hydrostatic tensile stress is generally believed to be the driving force for stress void nucleation[3−5]. Areas with the most concentrated hydrostatic tensile stress are thought to be the most probable areas where voids nucleate[6, 7]. Therefore, the maximum hydrostatic stress can be used to predict the reliability of copper interconnects[8]. It is difficult to measure the stress in copper interconnects exactly by experiment, so many papers use simulations instead. There have been some publications discussing hydrostatic stress in copper interconnects with respect to the material properties and geometrical features by simulation[8, 9]. However, their models are based on samples fabricated in the laboratory, which are different from ones made in industry.

In this work, a model based on the sample, which is fabricated in industry, is used and we perform calculations to reveal hydrostatic stress distribution in these interconnects using three-dimensional finite element analysis. The chip feature size is 65 nm. In addition, hydrostatic stress is studied by the influences of different low-k dielectrics, barrier layers and line widths of copper lines.

2. Finite element model description

Figures 1(a) and 1(b) show SEM images of the cross-section and surface depicting copper interconnects. The copper lines are fabricated using the damascene technique in SiO_2 using a Ta barrier layer. The thickness/width of the interconnect in Fig. 1(a) is 0.1 μm/0.78 μm and the spacing is 0.82 μm between the two lines. The thickness of the SiO_2 is 0.45 μm. Figures 1(c) and 1(d) show the model geometry and finite element mesh for the damascene structure in Fig. 1(a). The directions along the line-length, along the interconnect thickness and along the interconnect width are denoted by the x, y and z directions. The entire model has spans of 8.0, 1.7 and 1.61 μm along the x, y and z directions, respectively. The thickness of SiO_2 around the copper interconnect is 0.45 μm and the bottom layer is Si with a thickness of 1 μm. The thickness of Ta is 0.02 μm for the bottom and 0.01 μm for the sidewall, and that of the SiN is 0.05 μm. The thickness of the copper line is 0.1 μm and the width is 0.78 μm (only 0.39 μm included in the computational domain due to symmetry). In this simulation, the low-k dielectrics are SiLK (organic polymer-based low-k), FOx (flowable oxide), TEOS (tetraethyl orthosilicate) and PETEOS (plasma enhanced tetraethyl orthosilicate). The barrier layers are Ti, Ta and TaN, respectively.

Commercial finite element software, ANSYS, is used for the calculation. The bottom plane is assumed to be rigidly clamped onto the substrate, in such a way that no displacement is allowed in any direction. The top surface is free to move during deformation. Taking into consideration the damascene array structure along the x and z directions, mirror symmetry normal to each surface is imposed on the other four surfaces. All interfaces are assumed to have perfect adhesion. The discretizations use eight-noded linear brick-shape elements. Each material is assumed to be an isotropic linear elastic solid. This assumption is reasonable because it is known that copper lines, whose width is in the sub-micron range, continue to show linear elastic behavior even at temperatures as high as 400 ℃[6, 10]. Although Cu crystals are mechanically anisotropic, the orientation dependence and texture effects are ignored in the modeling, assuming sufficiently random crystal orientations for the

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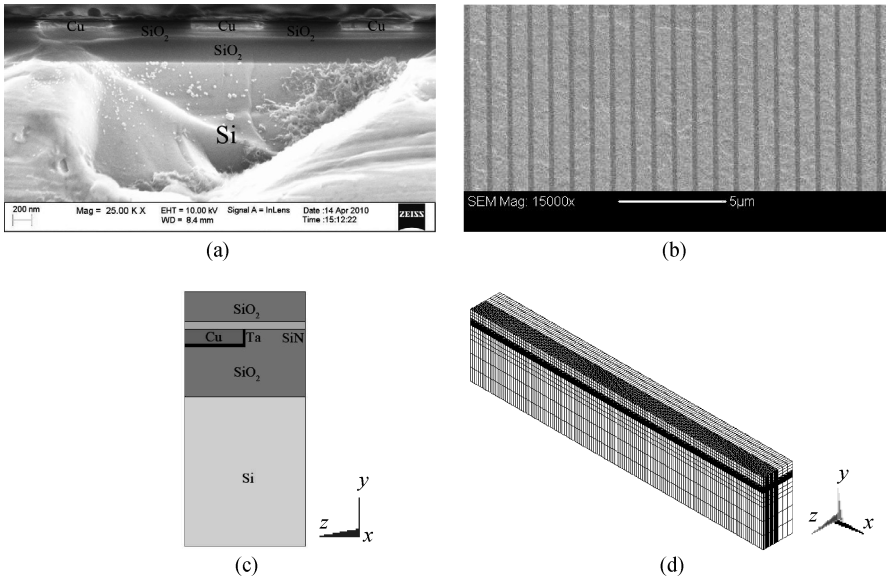

Fig. 1. SEM images depicting the damascene copper interconnects of the (a) cross-section and (b) surface and the model used for the damascene structure, description of (c) geometry and (d) finite element meshing.

Table 1. Thermo-mechanical properties of the materials used in the finite element calculations.

Property	Material	Modulus (GPa)	CTE (10^{-6}/℃)	Poisson's ratio
Substrate	Si	130 [a]	2.61 [e]	0.28 [a]
Line	Cu	110 (20 ℃) [b] 104 (350 ℃) [b]	17.0 (20 ℃) [b] 19.3 (350 ℃) [b]	0.30 [b]
Etch stop	SiN [a]	220.8	3.2	0.27
Barrier layers	Ti [c]	116	8.6	0.32
	Ta [a]	185.7	6.5	0.342
	TaN [b]	200	4.7	0.30
Low-k dielectrics	SiO_2 [d]	71.4	1.75	0.16
	PETEOS [e]	75	1	0.24
	TEOS [f]	59	1	0.16
	FOx [e]	8	20.5	0.19
	SiLK [g]	2.5	66	0.40

[a]Ref. [8]; [b]Ref. [11]; [c]Ref. [12]; [d] Ref. [13]; [e] Ref. [14] ; [f] Ref. [15] ; [g]Ref. [16].

damascene copper structure[11]. The properties of the materials used in this calculation are summarized in Table 1.

In Table 1, some material properties are shown as independent of temperature. This is mainly because the temperature dependence is either unclear or its inclusion will only affect the modeling result very slightly. Calculations are performed for cooling from the initial stress-free temperature, which is assumed to be 350 ℃, to room temperature (20 ℃). The annealed copper will be at a relatively stress-free state at about 350 ℃ as assumed in this work because this is supported by experimental X-ray diffraction measurements which have shown a zero stress state at about 300–350 ℃[6].

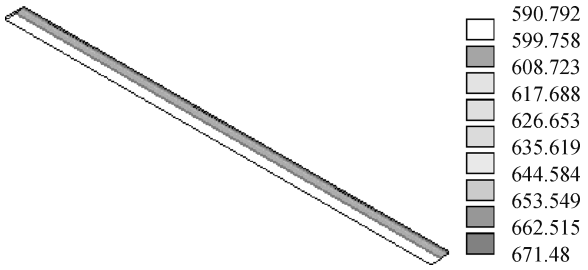

Fig. 2. Contour plot of hydrostatic stress σ_h (MPa) in the damascene copper interconnect for the SiO_2 model with a Ta barrier layer and line width of 0.78 μm.

3. Results and discussions

3.1. Hydrostatic stress distribution in the copper interconnect

Figure 2 shows the contour plot of hydrostatic stress (σ_h) developed in the copper line upon cooling, for the model of SiO_2 with Ta barrier layer and its line width is 0.78 μm. For easy visualization, all the other materials (including the barrier layers) are removed from the figure so the bare copper is shown. Hydrostatic stress, defined as $(\sigma_{xx} + \sigma_{yy} + \sigma_{zz})/3$, is non-uniform throughout the damascene copper line and the highest hydrostatic tensile stress is concentrated at the top surface, near the border. The calculated highest stress value is about 670 MPa. Although a hydrostatic tension stress of the order of 1 GPa would normally be needed to overcome the en-

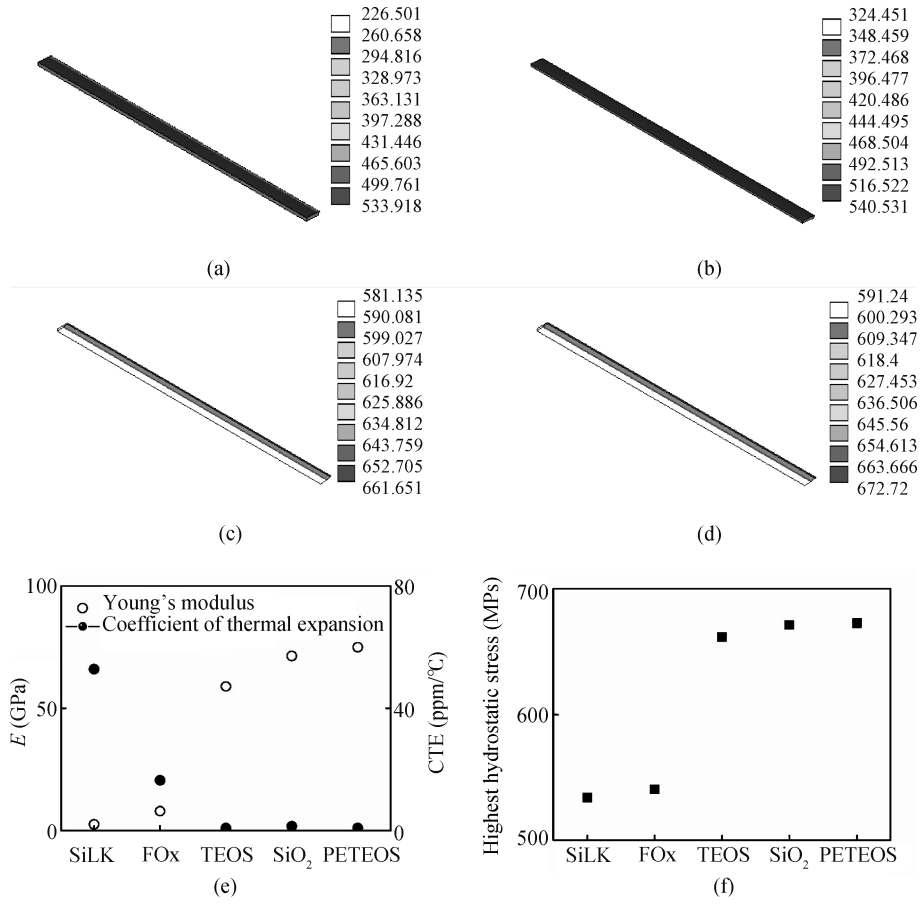

Fig. 3. Contour plots of hydrostatic stress (in MPa) in copper interconnects assembly for the models of (a) SiLK, (b) FOx, (c) TEOS and (d) PETEOS with a Ta barrier layer. (e) Comparison of Young's modulus and CTE of different low-k dielectrics and (f) the highest hydrostatic stress components in periodically arrayed copper interconnects with variations of low-k dielectrics and SiO_2 with Ta barrier layer, whose line widths are 0.78 μm.

ergy barrier for void nucleation[17], it can be lowered by the formation of a void at defects[18]. The top surface of the metal lines is likely to be contaminated during the CMP (chemical mechanical polishing) process and have a lot of defects or a high interfacial energy[19]. Therefore, voids are highly probable to nucleate at the top surface of the metal lines due to the high density of interfacial defects, as well as the high stress values in this region.

3.2. Effect of different low-k dielectrics and barrier layers

Figures 3(a)–3(d) show the contour plots of the stress component σ_h developed for the models of different low-k dielectrics with a Ta barrier layer. They show that the distribution of hydrostatic stress is non-uniform and that the highest hydrostatic stress exists on the top interface for these lines. Figure 3(e) shows a comparison of the Young's modulus and CTE of different low-k dielectrics. Figure 3(f) shows the highest hydrostatic stress components in periodically arrayed copper lines with variations of low-k dielectrics and SiO_2, and with Ta barrier layer. From them, we can conclude that with Young's modulus increasing and CTE decreasing, the hydrostatic stress increases. In addition, Figure 3(e) shows that Young's modulus in the PETEOS model is larger than that in the TEOS model and the CTE in two models is the same. Figure 3(f) shows that the hydrostatic stress in the PETEOS model is larger than that in the TEOS model. Thus, we consider that the stress is proportional to Young's modulus. The above results illustrate that high CTE and low Young's modulus of low-k dielectrics can decrease the highest hydrostatic stress on the top interface. Hydrostatic stress is smallest in lines with low-k dielectrics for SiLK.

Figures 4(a) and 4(b) show the contour plots of stress component σ_h developed for the models of different barrier layers in SiO_2. They reveal that the distribution of hydrostatic stress is non-uniform and the highest hydrostatic stress exists on the top interface for these lines. Figure 4(c) shows a comparison of the Young's modulus and CTE of different barrier layers. Figure 4(d) shows the highest hydrostatic stress components in periodically arrayed copper interconnect lines with variations of barrier layers. They show that the hydrostatic stress first decreases and then increases when Young's modulus increases and CTE decreases in the barrier layers. Thus, we can conclude that the hydrostatic stress is smallest in lines with a Ta barrier layer.

3.3. Effect of line width

Figure 5 shows SEM images depicting the damascene copper interconnects with different line widths in SiO_2 and the Ta

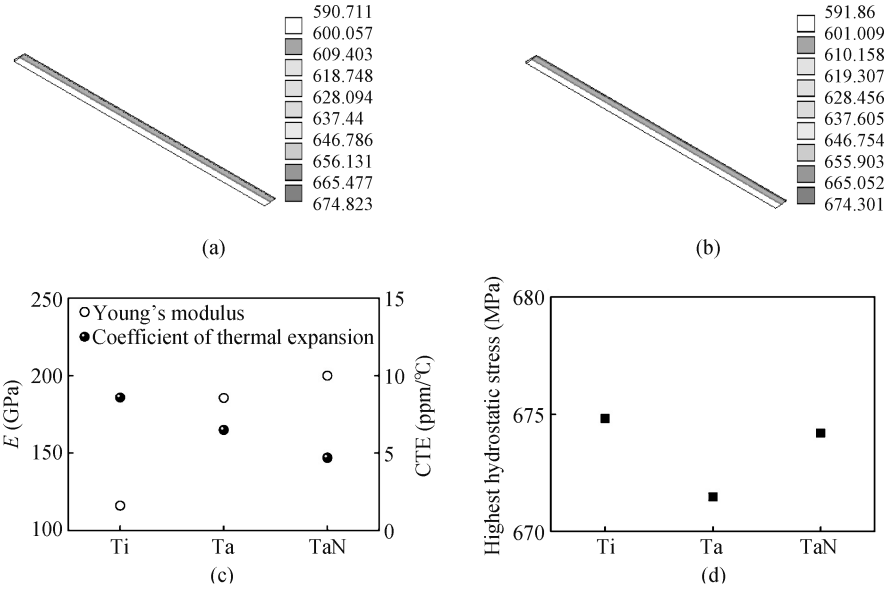

Fig. 4. Contour plots of hydrostatic stress (in MPa) in copper interconnects assembly for the models of (a) Ti and (b) TaN in SiO_2. (c) Comparison of Young's modulus (E) and CTE of different barrier layers and (d) the highest hydrostatic stress components in periodically arrayed copper lines with variations of barrier layers in SiO_2, whose line widths are 0.78 μm.

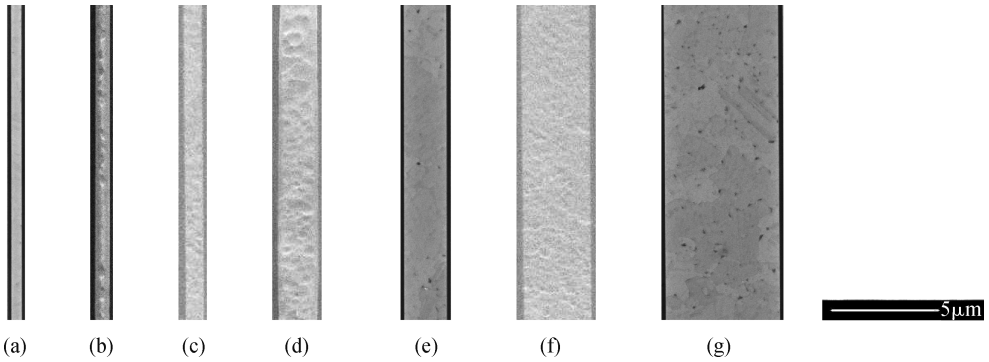

Fig. 5. SEM images depicting the damascene copper interconnects on the top surface with different line widths: (a) 0.51 μm, (b) 0.66 μm, (c) 0.78 μm, (d) 1.92 μm, (e) 2.09 μm, (f) 3.18 μm and (g) 5.33 μm in SiO_2 and Ta barrier layer.

barrier layer. The thickness is 0.1 μm for all of the copper lines. Figures 6(a)–6(g) show contour plots of hydrostatic stress in copper interconnects with different line widths. The spacing is 0.82 μm for all of the lines. Figure 6(h) shows the plots of the highest hydrostatic stress for copper interconnects against line width in different low-k dielectrics with a Ta barrier layer. In fact, the submicron-wide lines present purely thermo-elastic behavior upon cooling to room temperature[6].

Figures 6(a)–6(g) show that the distribution of hydrostatic stress is non-uniform and the highest hydrostatic stress exists on the top interface and near the border for all lines in SiO_2. From Fig. 6(h), for the SiLK and FOx models, we can see that with line width increasing, the hydrostatic stress increases. When the line width is 0.51 μm, the hydrostatic stress is at the minimum for them. Thus, we can conclude that copper interconnects with a line width of 0.51 μm is the most reliable for the models of SiLK and FOx. On the whole, for the SiO_2 and TEOS models, as line width increases, the hydrostatic stress first decreases and then subsequently increases. For them, hydrostatic stress is at a minimum when the line width is 0.66 μm. Therefore, we can conclude that copper interconnects with a line width of 0.66 μm are the most reliable for SiO_2 and TEOS models. Figure 6(h) also shows that the hydrostatic stress in the SiO_2 model is the largest among the copper interconnects, with line width increasing. In addition, hydrostatic stress in the SiLK model is at a minimum when the line width is smaller than 3 μm and stress in the FOx model is at its minimum when the line width is larger than 3 μm among copper lines. The above results illustrate that when the line width is 0.51 μm, the copper interconnect for the SiLK model is the most reliable of four models because the hydrostatic stress on its top surface is the smallest. Therefore, it can resist void nucleation and prolong the life time of electromigration best.

4. Conclusions

In the present work, hydrostatic stress and its distribution of copper damascene interconnects are calculated with different low-k electrics, barrier layers and line widths. It has been shown that hydrostatic stress is highly non-uniform through-

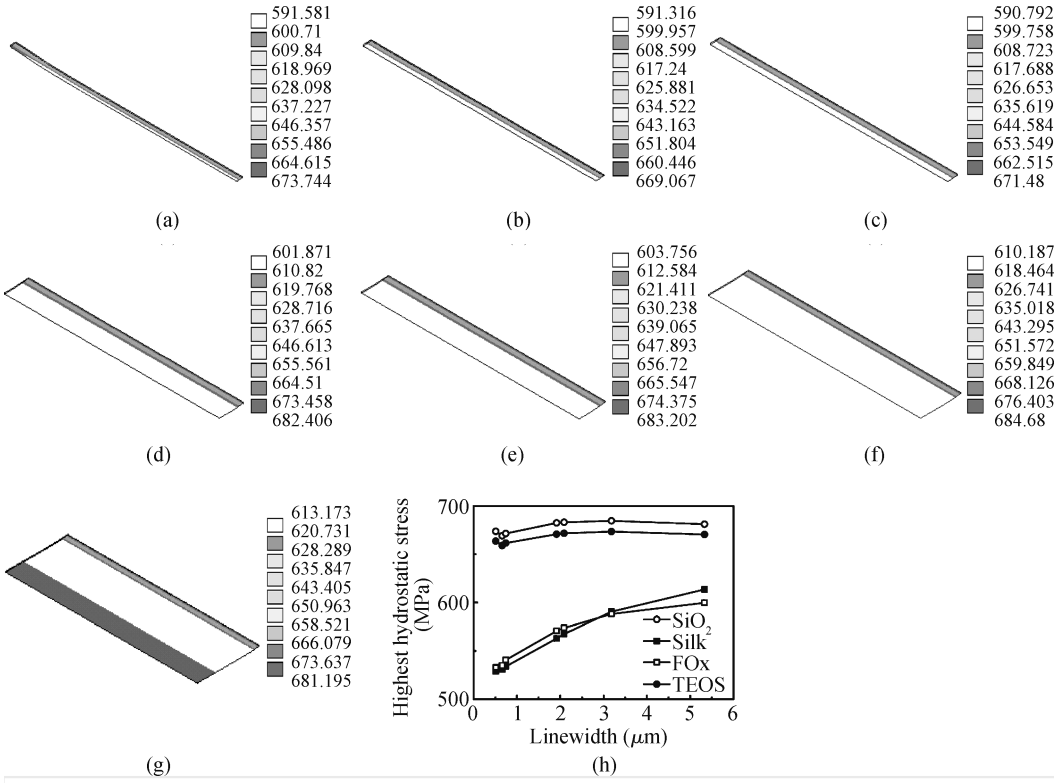

Fig. 6. Contour plots of hydrostatic stress (in MPa) in copper interconnects with different line widths: (a) 0.51 μm, (b) 0.66 μm, (c) 0.78 μm, (d) 1.92 μm, (e) 2.09 μm, (f) 3.18 μm and (g) 5.33 μm in SiO_2 and Ta barrier layer. (h) The plots of the highest hydrostatic stress against line width in the models of SiO_2, SiLK, FOx and TEOS with Ta barrier layer in copper interconnects.

out copper lines and the highest tensile hydrostatic stress exists on the top interface of all of the interconnects. The high CTE and low Young's modulus of the low-k dielectrics can decrease the highest hydrostatic stress on the top interface, which can improve the reliability of copper interconnects. In addition, the value of the highest hydrostatic stress is proportional to Young's modulus. SiLK is the most suitable low-k dielectric and Ta is the most suitable barrier material. As to the highest hydrostatic stress with line width increasing, hydrostatic stress increases in the SiLK and FOx models. Stress is at the minimum for them when the line width is 0.51 μm. For the SiO_2 and TEOS models, the hydrostatic stress first decreases and subsequently increases as line width increases. Stress is at a minimum for them when the line width is 0.66 μm. In addition, the copper interconnect for the SiLK model with a Ta barrier layer, whose line width is 0.51 μm, is the most reliable among the four models because the hydrostatic stress on its top surface is the smallest. Thus, it can resist void nucleation and prolong the life time of electromigration the best.

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