# Influence of substrate temperature on the performance of zinc oxide thin film transistor*

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**Abstract:** Top-contact thin film transistors (TFTs) using radio frequency (RF) magnetron sputtering zinc oxide (ZnO) and silicon dioxide ($SiO_2$) films as the active channel layer and gate insulator layer, respectively, were fabricated. The performances of ZnO TFTs with different ZnO film deposition temperatures (room temperature, 100 ℃ and 200 ℃) were investigated. Compared with the transistor with room-temperature deposited ZnO films, the mobility of the device fabricated at 200 ℃ is improved by 94% and the threshold voltage shift is reduced from 18 to 3 V (after 1 h positive gate voltage stress). Experimental results indicate that substrate temperature plays an important role in enhancing the field effect mobility, sharping the subthreshold swing and improving the bias stability of the devices. Atomic force microscopy was used to investigate the ZnO film properties. The reasons for the device performance improvement are discussed.

**Key words:** ZnO-TFT; bias stability; substrate heat; RF magnetron sputtering
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## 1. Introduction

Transparent electronics has potential opportunities to create next generation optoelectronic devices and invisible computing[1]. Zinc oxide (ZnO) is one of the most interesting II–IV compound semiconductors with a wide direct band gap of 3.34 eV, transparency in the visible range and high carrier mobility. Based on these characteristics, thin film transistors (TFTs) using ZnO as an active channel layer are being intensely explored[2−5]. The research trends of ZnO-TFTs have mostly focused on high device performance[6−9]. However, it is certainly necessary to obtain stable device characteristics under various bias, temperature and light conditions. The guarantee of device stability under external environments is considered to be an important subject for the buoyant development of oxide TFTs. And much attention has been paid to the investigation of bias stability for oxide-TFTs in the past few years[10−12].

In this work, ZnO-TFTs with ZnO films deposited at different substrate temperatures were fabricated. The influences of different substrate temperatures on device performance were investigated. Compared with room-temperature (RT) fabricated ZnO-TFT (device a), the device fabricated at 200 ℃ (device c) shows a much larger mobility (1.60 $cm^2/(V{\cdot}s)$ for the former and 3.11 $cm^2/(V{\cdot}s)$ for the latter) and the subthreshold swing decreases from 2.4 to 1.9 V/dec. Other than these improvements, device c shows a distinctly bias stress stability enhancement compared with device a. The experimental results indicate that proper substrate temperature can remarkably improve the performance of ZnO-TFTs.

## 2. Experimental details

Three kinds of TFTs with different substrate temperature deposited ZnO films as channel layers were constructed (as shown in Fig. 1(a)). The devices were fabricated by using indium tin oxides glasses (ITO-glass) as the substrates and gate electrodes. Initially, 300 nm thick $SiO_2$ films were deposited on the cleaned ITO-glass substrates (Corning 1737) by radio frequency (RF) magnetron sputtering at room temperature (RT) using a Si target (3 inch in diameter, 99.99% in purity). The deposition conditions for $SiO_2$ films were a sputtering pressure of $\sim$ 0.5 Pa, gas mixing ratio of 70 : 30 for Ar : $O_2$, and input power of $\sim$ 100 W. The 25 nm ZnO layers were deposited at three different substrate temperatures of room-temperature (device a), 100 ℃ (device b) and 200 ℃ (device c) using a ZnO target (3 inch in diameter, 99.99% in purity) at a lower input power of 40 W. The gas mixing ratio of Ar : $O_2$ was 100 : 4, and the total pressure was 1 Pa. After the deposition of ZnO layers, about 200 nm Al was deposited by vacuum evaporation to form the source and drain electrodes through a shadow-mask. The channel width ($W$) and length ($L$) were 500 $\mu$m and 230 $\mu$m, respectively. The thicknesses of the films were measured by the alpha step (Dektak 3st). Atomic force microscopy (AFM, nanonavi SPA-400 SPM) was used to investigate the ZnO film properties. The electrical characteristics of the ZnO-TFTs and $SiO_2$ dielectrics were measured using an Agilent E3647A dual output DC power supply and a Keithley 6485 picoammeter. The capacitance characteristics were measured using an Agilent E4980A LRC meter.

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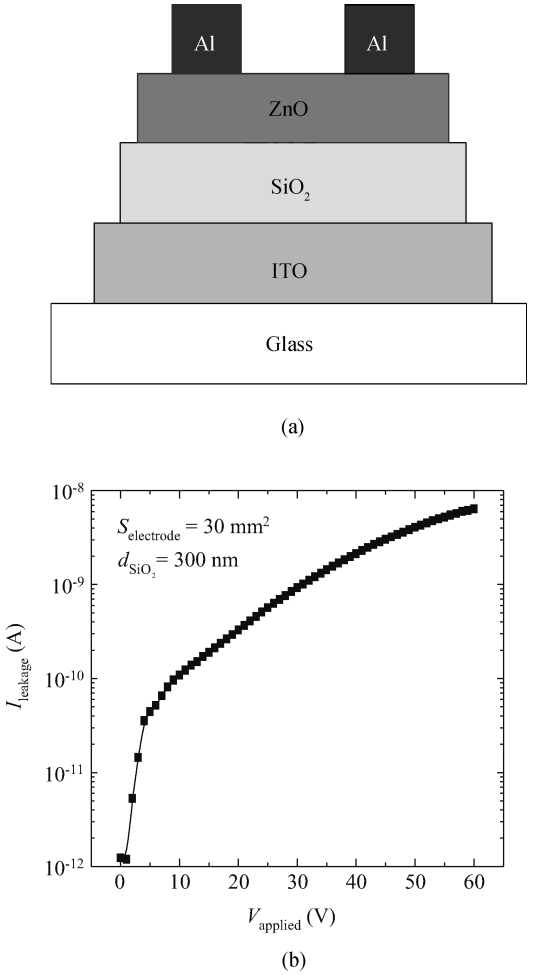


Fig. 1. (a) Schematic structure of the ZnO-TFT. (b) Leakage current of the sputtering $SiO_2$ films.

## 3. Results and discussion

Figure 1(b) shows the leakage current characteristics of the $SiO_2$ capacitor with ITO and Al as the electrodes. The electrode area was 30 $mm^2$ and the $SiO_2$ thickness was 300 nm. As can be seen from Fig. 1(b), the $SiO_2$ insulator layer shows a good insulation property. The leakage current is just of the order of $10^{-9}$ A, even if the applied voltage reaches 60 V. The measured capacitance is 10 $nF/cm^2$ for the 300 nm RF magnetron sputtering $SiO_2$ film.

Figures 2(a)–2(c) show the corresponding transfer characteristics of $I_{DS}$ versus $V_{GS}$ and the $I_{DS}^{1/2}$ versus $V_{GS}$ curves at a fixed $V_{DS}$ of 40 V for the ZnO-TFTs. We can see that the off-state current of the devices with the substrate temperature of RT, 100 ℃ and 200 ℃ deposited ZnO films as the channel layers is $1.17 \times 10^{-11}$, $1.04 \times 10^{-11}$ and $4.20 \times 10^{-12}$ A, respectively, and the on/off ratio is $3.40 \times 10^6$, $2.80 \times 10^6$ and $9.70 \times 10^6$, respectively. That is, with an increase in substrate temperature, the off-state current decreases accordingly. The 200 ℃ substrate temperature deposited ZnO film based device (device c) shows the smallest off-state current and the largest on/off ratio among the devices.

From the $I_{DS}^{1/2}$–$V_{GS}$ curves shown in Fig. 2, the channel mobility ($\mu_{sat}$) and threshold voltage ($V_{TH}$) can be extracted

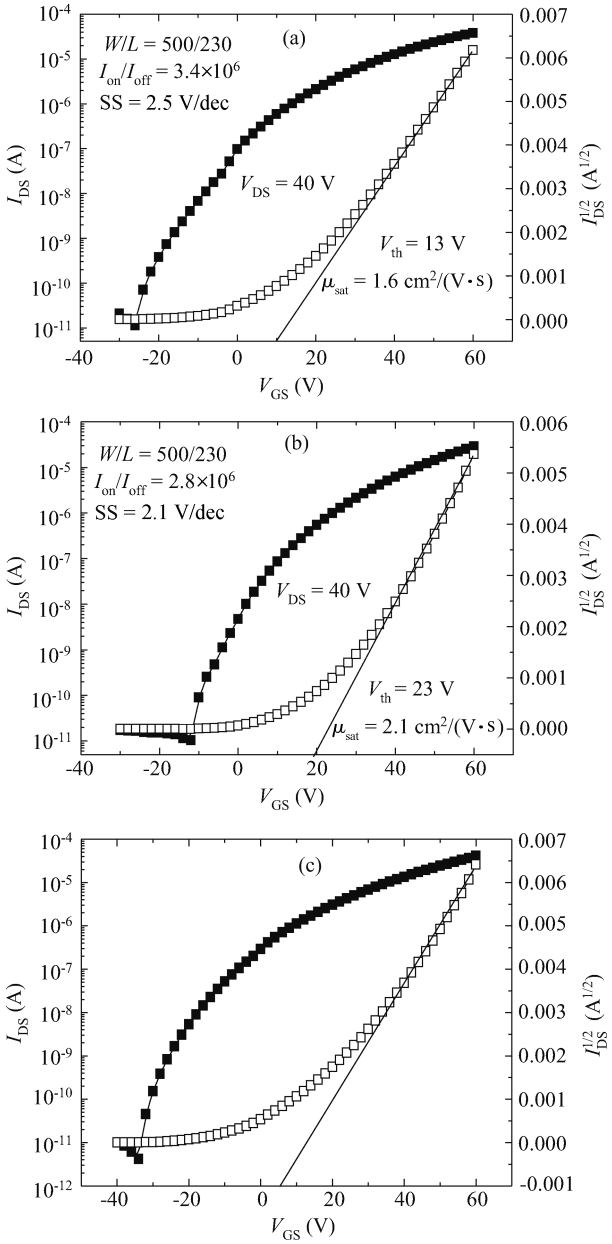


Fig. 2. Transfer characteristic curves of $I_{DS}$ versus $V_{GS}$ and $I_{DS}^{1/2}$ versus $V_{GS}$ at a fixed $V_{DS}$ = 40 V for the ZnO-TFTs with different substrate temperature deposition ZnO channel layers. (a) RT. (b) 100 ℃. (c) 200 ℃.

by fitting straight lines into the plots of the square root of drain current versus gate–source voltage, according to Eq. (1),

$$I_{DS} = \frac{C_i \mu W}{2L}(V_{GS} - V_{TH})^2, \quad V_{DS} > V_{GS} - V_{TH}, \quad (1)$$

where $C_i$ (10 $nf/cm^2$) is the capacitance per unit area of the insulator layer, $W$ and $L$ are the channel width and length, and $V_{DS}$ and $V_{GS}$ are the drain–source voltage and gate–source voltage, respectively. The calculated channel mobility is 1.60, 2.10 and 3.11 $cm^2/(V{\cdot}s)$ for devices a, b and c, respectively. That is, with an increase in the substrate temperature, the field effect mobility increases as well. The field effect mobility of device c shows a 94% enhancement as compared to device a.

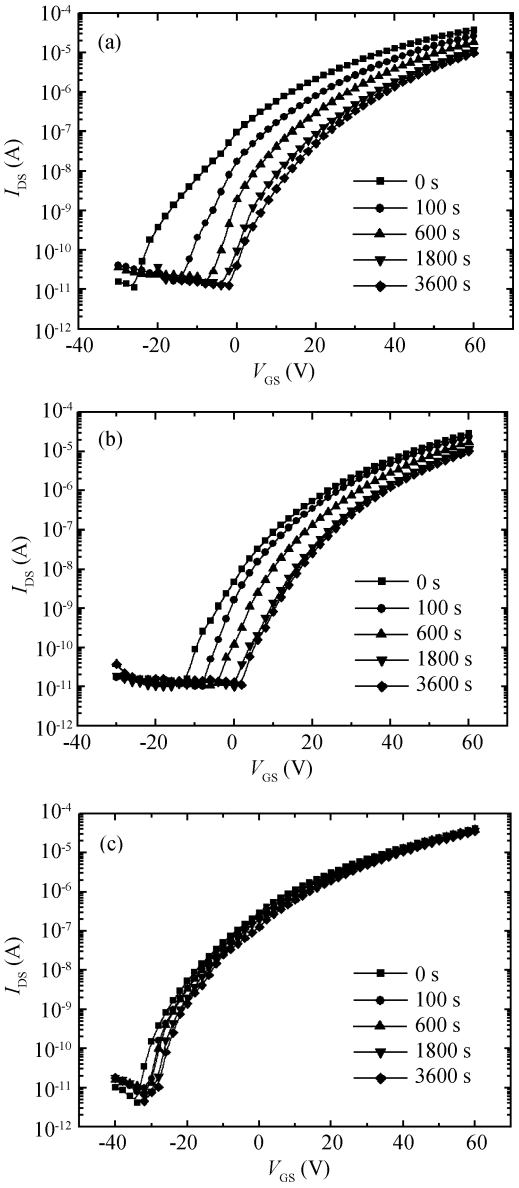


Fig. 3. Transfer curves of different temperature ZnO based ZnO-TFTs were obtained when a gate bias of 25 V was applied for an hour at room temperature in atmosphere. (a) RT. (b) 100 ℃. (c) 200 ℃.

The sub-threshold voltage swing (SS) is defined as the voltage that can make the drain current increase by a factor of 10. From the transfer characteristics, we can also determine the gate voltage swing (SS), through Eq. (2),

$$\mathrm{SS} = \frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}(\lg I_{\mathrm{DS}})}. \tag{2}$$

Here, we extracted the values of 2.5 V/dec, 2.1 V/dec and 1.9 V/dec for devices a, b and c under analysis. From SS we can infer the maximum density of surface states at the semiconductor/dielectric interface as

$$N_{\max}^{\mathrm{SS}} = \left[\frac{\mathrm{Slg}e}{kT/q} - 1\right]\frac{C_{\mathrm{i}}}{q}. \tag{3}$$

Taking into account the value of $C_{\mathrm{i}}$, the value of $2.52 \times 10^{12}$ cm$^{-2}$, $2.10 \times 10^{12}$ cm$^{-2}$ and $1.90 \times 10^{12}$ cm$^{-2}$ for $N_{\max}^{\mathrm{SS}}$ are calculated for the RT, 100 ℃ and 200 ℃ deposited ZnO films based devices, respectively. This indicates that with an increase in substrate temperature, the trap states at the semiconductor/dielectric interface decrease accordingly.

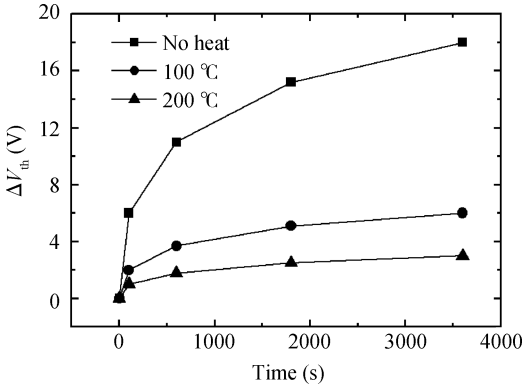


Fig. 4. Time dependent $\Delta V_{\mathrm{th}}$ under constant gate voltage (25 V) stress for different substrate temperature deposited ZnO film based TFTs.

Other than the improvements mentioned above, the most important result for this work is that the bias stability of the device is remarkably enhanced by the substrate temperature.

Figures 3(a)–3(c) indicates that all of the transfer curves show a positive shift by the positive gate voltage stress. Such a phenomenon indicates that charges are trapped at the insulator/channel interfacial layer and/or in the insulator with applied gate bias. However, as the substrate temperature increases, the shift decreases quickly. Compared with devices a and b, device c shows a much smaller shift. This phenomenon indicates that the charge trapping effect is effectively suppressed for the 200 ℃ deposited ZnO film based device. Before the stress, the saturation mobility ($\mu_{\mathrm{sat}}$) and SS value were 3.11 cm$^2$/(V·s) and 1.90 V/dec for device c, respectively, while those after the stress tests were 3.05 cm$^2$/(V·s) and 1.92 V/dec. This indicates that the gate voltage stress does not deteriorate the important TFT performance parameters, such as saturation mobility and subthreshold swing, but causes only the parallel shift of the transfer curves to the positive. These results indicate that there are no extra defect states that affect the SS value generated in the 200 ℃ substrate temperature deposited ZnO film based TFT during positive gate voltage stress. Quite the other way: degeneration in the SS value and $\mu_{\mathrm{sat}}$ were observed in the RT and 100 ℃ substrate temperature deposited ZnO film based devices. Especially for the RT deposited ZnO film based TFT, the SS value increases from 2.5 to 3.0 V/dec and $\mu_{\mathrm{sat}}$ decreases from 1.90 to 1.42 cm$^2$/(V·s) after the stress.

It can be seen from Fig. 4 that with the increase in the substrate temperature, $\Delta V_{\mathrm{th}}$ decreases sharply. For example, at the time of 3500 s, the $\Delta V_{\mathrm{th}}$ is 18 V, 6 V and 3 V for the RT, 100 ℃ and 200 ℃ substrate temperature deposited ZnO films based TFTs, respectively. The results show that substrate temperature during the deposition of ZnO films can markedly improve the bias stability for RF magnetron sputtering ZnO-TFTs.

In order to find the reasons for the enhancement of the device performances, AFM was used to investigate the ZnO films deposited at different substrate temperatures (as shown in Figs. 5(a)–5(c)).

From Fig. 5, we can see that with an increase in substrate temperature, the surface morphology of the ZnO films

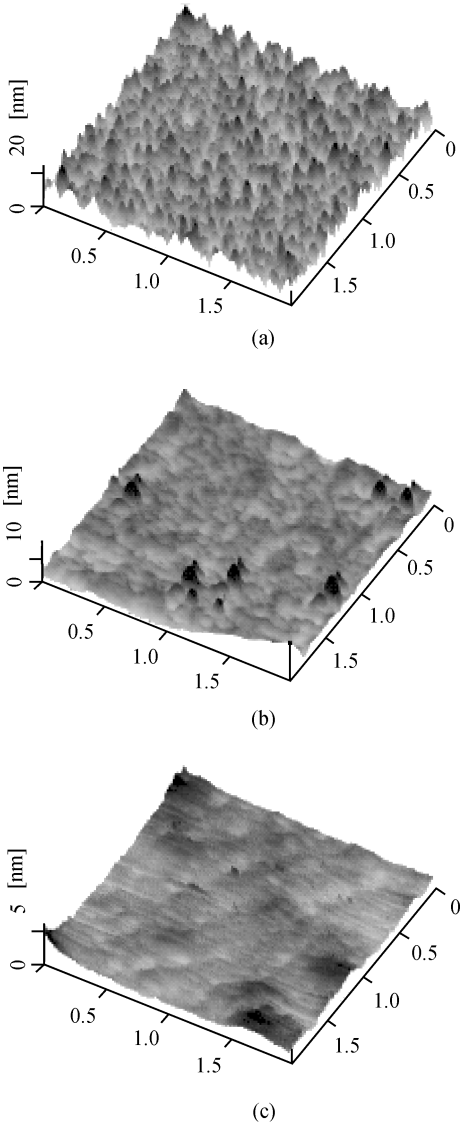


Fig. 5. Top-view AFM images of surface morphology for 25 nm thick ZnO films with different substrate temperatures deposited on 300 nm $SiO_2$ insulators. (a) RT. (b) 100 ℃. (c) 200 ℃.

is clearly improved. The overall surface roughness for RT, 100 ℃ and 200 ℃ deposited ZnO films is 3.09, 1.44 and 0.58 nm, respectively. We can also see that with increasing substrate temperature, the surface grains slowly changed from individual sharp "peak" to united cluster, which may result in fewer defects for the ZnO film (due to the reduction in the grain boundaries). As we know, electron trapping at the gate dielectric/channel interface or gate-field induced oxygen adsorption is determined to cause the positive $V_{th}$ shift under positive bias stress[13, 14]. The improvement in the ZnO film surface morphology may make the oxygen adsorption alleviative during the stressing process, which leads to the enhancement of the bias stability for the TFT device. Another reason is that substrate heating during the ZnO film deposition process will make the ZnO film have a better quality. If the substrate was heated at a higher temperature during the ZnO deposition process, the migration capability of the atom should be enhanced, which will result in better crystalline quality and better electric properties of the ZnO film, while ZnO thin films grown at room temperature show a deteriorated electrical performance due to the reduced crystalline quality and increased randomness of deposited atoms[15]. Furthermore, the enhanced atom migration capability can make a better insulator/channel layer interface for the higher substrate temperature deposited ZnO film (the smaller $N_{max}^{SS}$ for device c also supports this point of view), and this interface played a key role in the performance of the TFT devices[16−18].

## 4. Conclusions

In summary, top-contact TFTs using various substrate temperature deposited ZnO films as channel layers and RF magnetron sputtering $SiO_2$ as gate dielectrics were fabricated and investigated. As the substrate temperature gets higher, the performance and bias stability of the corresponding devices are enhanced accordingly. Overall, the device with ZnO film deposited on 200 ℃ substrate as the active layer offers the best performance, which shows a field effect mobility enhancement of 94%, on/off ratio improvement of 300%, sub-threshold swing reduction of 30% and threshold voltage shift decrease from 18 to 3 V, compared with the device with ZnO film deposited on RT substrate. AFM investigation indicates that with increasing temperature, the overall surface roughness decreases clearly and the surface grains slowly change from individual sharp "peak" to united cluster. Experimental results indicate that the appropriate substrate temperature can maximize the performance of ZnO-TFT.

## References

[1] Wager J F. Transparent electronics. Science, 2003, 300: 1245
[2] Hoffman R L, Norris B J, Wager J F. ZnO-based transparent thin-film transistors. Appl Phys Lett, 2003, 82: 733
[3] Nomura K, Ohta H, Ueda K, et al. Thin film transistor fabricated in single-crystalline transparent oxide semiconductor. Science, 2003, 300: 1269
[4] Fortunato E, Barquinha P, Pimentel A, et al. Fully transparent ZnO thin-film transistor produced at room temperature. Adv Mater, 2005, 17: 590
[5] Jackson W B, Hoffman R L, Herman G S. High-performance flexible zinc tin oxide field-effect transistors. Appl Phys Lett, 2005, 87: 193503
[6] Lee J M, Choi B H, Ji M J, et al. The improved performance of a transparent ZnO thin-film transistor with AlN/$Al_2O_3$ double gate dielectrics. Semicond Sci Technol, 2009, 24: 055008
[7] Chen M C, Chang T C, Huang S Y, et al. A low-temperature method for improving the performance of sputter-deposited ZnO thin-film transistors with supercritical fluid. Appl Phys Lett, 2009, 94: 162111
[8] Fortunato E M C, Barquinha P M C, Pimentel A C M B G, et al. Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature. Appl Phys Lett, 2004, 87: 2541
[9] Fortunato E, Pimentel A, Pereira L, et al. High field-effect mobility zinc oxide thin film transistors produced at room temperature. Journal of Non-Crystalline Solids 2004, 338: 806
[10] Lee K H, Jung J S, Son K S, et al. The effect of moisture on the photon-enhanced negative bias thermal instability in Ga–In–Zn–O thin film transistors. Appl Phys Lett, 2009, 95: 232106
[11] Liu P T, Chou Y T, Teng L F. Environment-dependent metastability of passivation-free indium zinc oxide thin film transistor after gate bias stress. Appl Phys Lett, 2009, 95: 233504

[12] Moon Y K, Lee S, Kim W S, et al. Improvement in the bias stability of amorphous indium gallium zinc oxide thin-film transistors using an $O_2$ plasma-treated insulator. Appl Phys Lett, 2009, 95: 013507
[13] Cross R B M, De Souza M M. Investigating the stability of zinc oxide thin-film transistors. Appl Phys Lett, 2006, 89: 263513
[14] Jeong J K, Yang H W, Jeong J H, et al. Origin of threshold voltage instability in indium–gallium–zinc oxide thin film transistors. Appl Phys Lett, 2008, 93: 123508
[15] Ahn C H, Seo D K, Woo C H, et al. Physics of condensed matter. Physica B, 2009, 404: 4853
[16] Vōlkel A R, Street R A, Knipp D. Carrier transport and density of state distribution in pentacene transistors. Phys Rev B, 2002, 66: 195336
[17] Verlaak S, Arkhipov V, Heremans P. Modeling of transport in polycrystalline organic semiconductor films. Appl Phys Lett, 2003, 82: 745
[18] Valletta A, Mariucci L, Fortunato G. Surface-scattering effects in polycrystalline silicon thin-film transistors. Appl Phys Lett, 2003, 82: 3119