Design of a 0.18 μm CMOS multi-band compatible low power GNSS receiver RF frontend

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Abstract: This paper presents the design and implementation of a fully integrated multi-band RF receiver frontend for GNSS applications on L-band. A single RF signal channel with a low-IF architecture is adopted for multi-band operation on the RF section, which mainly consists of a low noise amplifier (LNA), a down-converter, polyphase filters and summing circuits. An improved cascode source degenerated LNA with a multi-band shared off-chip matching network and band switches is implemented in the first amplifying stage. Also, a re-designed wideband double balance mixer is implemented in the down conversion stage, which provides better gain, noise figure and linearity performances. Using a TSMC 0.18 μm 1P4M RF CMOS process, a compact 1.27 GHz/1.575 GHz dual-band GNSS frontend is realized in the proposed low-IF topology. The measurements exhibit the gains of 45 dB and 43 dB, and noise figures are controlled at 3.35 dB and 3.9 dB of the two frequency bands, respectively. The frontend model consumes about 11.8–13.5 mA current on a 1.8 V power supply. The core occupies 1.91 × 0.53 mm^2 while the total die area with ESD is 2.45 × 2.36 mm^2.

Key words: low power; low IF; multi-band; noise figure; RF frontend; mixer

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1. Introduction

Due to constantly increasing and diversifying user demands, the single function GPS system can no longer satisfy users' multiple requirements. Moreover, the multi-path effect or urban canyon effect can easily result in a locating failure with a single functional GPS receiver. The multi-mode compatible GNSS (global navigation satellite system) receiver, which has been a popular research topic in recent years, can avoid these problems and be used in a global scope without blind spots.

However, the previous studies tended to focus on the parallel architecture that contains two or more RF channels operating separately[1−6]. In this paper, the possibility of employing a single RF channel with a multi-band frontend has been investigated. The dual-band is designed with the capability of operating at any two bands within the span of 1.1–1.7 GHz.

The research and practice show that the L-band and the C-band are the best frequencies for satellite navigation, although past research and practice showed that C-band navigation had still not become a strong competitor to the applications on the L-band (1164–1610 MHz). The differences among the four major international GNSSs are shown in Table 1. These four systems have occupied the best bands for satellite navigation. It is shown that only the GLONASS is different from the other three systems in access method (FDMA) and modulation (BPSK), which needs a more complicated PLL and VCO blocks. Other systems are only different in the values of the main parameters, which provide a possibility of sharing the signal channels and PLL blocks. The four systems use the same pseudo-range location algorithm theory, which means that they can share the same baseband processing block. Based on these ideas, the direction of compatibility design is clear.

The circuit solution needs to maintain low power consumption and high integration for the multi-band while simply switching to different mode controlling without a need of circuit complexity. The work presented in this paper describes a short overview of different RF frontend architectures. The best architecture for the GPS-like application is selected and further discussed. The solution of low-IF architecture with a single RF channel reused is given. The architecture selection and system definition and the details of the circuit design are discussed.

2. Architecture and system design

A comparison of mainstream RF receiver architectures[9] is shown in Table 2.

Conventional heterodyne architecture has superior performance in selectivity and sensitivity compared with other architectures. However, it requires high-Q discrete component filters, such as SAW (surface acoustic wave) or ceramic filters, which are impractically realized on the chip. Also, high drive capability requirements inevitably lead to more severe trade-offs among gain, noise figure, stability, and power dissipation. All of these make the heterodyne difficult to integrate on a chip, and thus it is rarely used commercially.

Homodyne architecture, also known as direct conversion or zero-IF architecture, employs low-pass filtering in the baseband to suppress nearby interference and to select the desired channel. The intermediary IF stages and IR filters are removed. However, the exacerbation of a number of issues, such as DC

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Table 1. System definition and compatibility of GNSSs[7, 8].

Navigation system	Beidou (Compass)	GPS	GALILEO	GLONASS
Frequency (MHz)	1207–1561 etc.	L1: 1575 L2: 1227 L5: 1176 etc.	L1: 1575 E5b: 1207 E5a: 1176 etc.	L1: 1602–1615 L2: 1240–1260 etc.
Channel access method	CDMA	CDMA	CDMA	FDMA
Radio polarization	Right-hand	Right-hand	Right-hand	Right-hand
Modulation	QPSK + BOC	QPSK + BOC	QPSK + BOC	BPSK
Clock frequency (mbps)	2.046	1.023	1.023	0.0511
Data rate	50/500 etc.	50 etc.	50/1000 etc.	50 etc.

Table 2. Architectures of RF receiver frontends.

Architecture	Heterodyne	Homodyne	Wideband-IF	Low-IF
IF location	High	Zero	Medium and Zero	Low
Image-rejection	External	None	Internal	Internal
DC-offset	No	High	Low	No
Required RF gain	Medium	High	Medium	Medium
Structural characteristics	Multi-filtering and multi-downconversion	Direct mownconversion	Dual-downconversion	Direct mownconversion
Integration ability	Low	High	High	High
Suitability for multi-band GNSS applications	No	No	Yes, but with a too complex structure	Yes

offsets, LO leakage and I/Q mismatch, are the challenges for the chip-design.

Wideband-IF[10] with double-conversion architecture is another alternative architecture for full integration. However, a second complex mixing is needed to convert the signal from IF to base band, which can be implemented as a variable-frequency crystal-controlled or voltage-controlled oscillator. This allows the possibility of a programmable integrated channel-select filter for multi standard receiver applications. Furthermore, since there are two LO operations being the RF carrier in the wideband-IF system, the LO leakage and time-varying DC offsets are minimized. However, it needs two or more PLL+VCO systems or multi crystal oscillators, which increases the design complexity and risk. In addition, by removing the channel-select filter at IF, strong adjacent channel interferers will become a concern for the second mixer stage as well as for the baseband blocks.

The low-IF[11, 12] topology combines the advantages of the three architectures above. Only one quandrature down conversion is implemented. The IF is chosen as low as one or two times the channel band-width, which is much lower than the first IF setting in wide-IF topology or RF section. It is more feasible to sample the low-IF signal after the first mixer stage with a high resolution analog-to-digital converter (ADC). The overall system structure has been simplified. Being different from zero-IF structure, the image frequency problem cannot be avoided. The image component should be separated from the complex signals and then be suppressed by extra circuits, such as polyphase filters or complex band-pass filters.

As discussed in Section 1, similar technologies are implemented in these variant navigation systems with only differences in some values of the parameters, which provide much convenience for our design of shared components. The low IF architecture with one RF signal path and two different IF signal paths is introduced. The proposed architecture is shown in Fig. 1.

The signal of the L-band is received by an active antenna with pre-amplifying and filtering functions, or received by a passive antenna and then pretreated with an on-chip optional pre-amplifier and an off-chip SAW filter. The antenna can be selected by control module. The cascode LNA is implemented as the first main stage, which is connected to two (I&Q) wide-band down-conversion mixers followed by the IF output buffer and IF channel selection switch. The LO (local oscillator) signal provided by a PLL and VCO system is variable in a certain frequency range for different IF needs by adjusting the capacitance of the VCO[13]. The RF section down converts the RF signal into differential I and Q signals, which are centered at different IFs for the bandwidth's needs. The following polyphase filter suppresses the image signal. And then the summing circuits are implemented to merge the differential I and Q signals into only differential signals. The signals are filtered further in order to extract the wanted signal from its neighbors with the IF band pass filters. With the adjustment of the AGC (automatic gain control) module, the IF signals are sampled by an ADC (analog-to-digital converter). The sampling frequency is switched according to the bandwidth and IF setting. The signals are converted to 2-bit or 4-bit 2 s complementary to the later demodulation in the baseband section. Also, the gain control feedback signals are judged by baseband section, which ensures the stability and the strength of the signal before the A/D process.

Our gain plan considers that the received signal power at the antenna port is about –133 to –130 dBm, which is much lower than the thermal noise level. The signal needs to be amplified to around 100–150 dB before the baseband process. Therefore, the total gain must be properly distributed to the RF band, IF band and baseband. In general, the gain in each

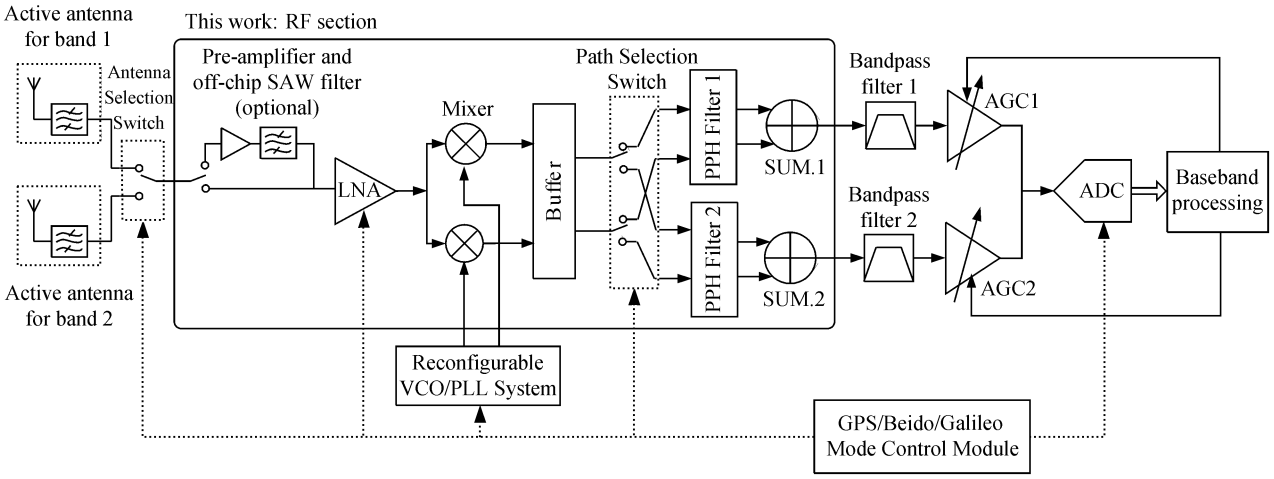

Fig. 1. Block diagram of proposed multi-band receiver architecture.

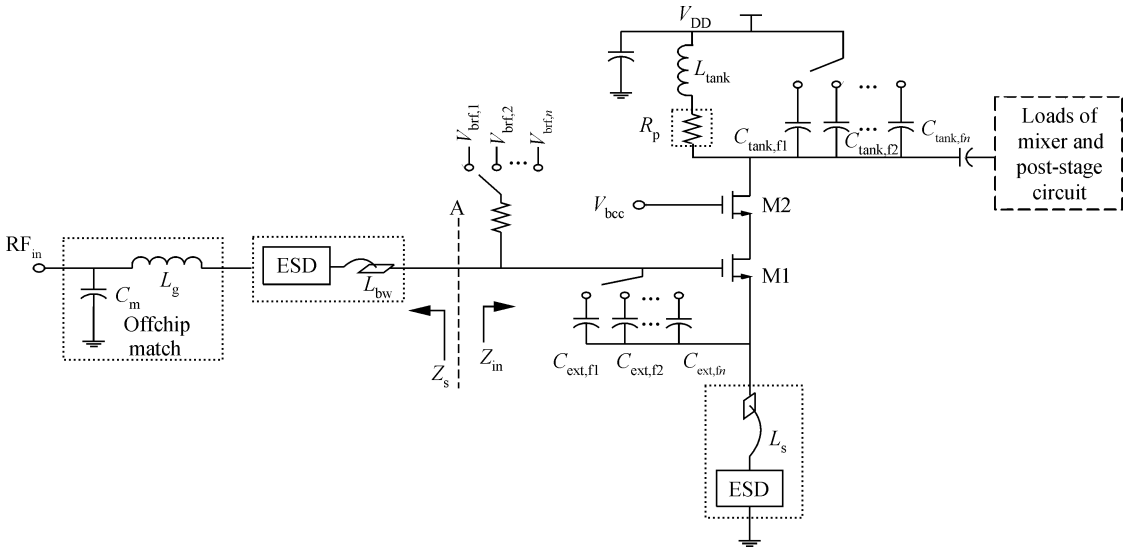

Fig. 2. Schematic of the proposed LNA.

band should be no more than 50–60 dB. In addition, in a fixed IF band, it is much easier to obtain narrow-band high-gain IF amplification than in the carrier frequency, so the IF band and baseband have larger gain distributions. The signal path needs to provide gain of 80–100 dB before the ADC, among which the LNA and mixer provide gain of about 25–35 dB. A certain level of the LNA's gain can minimize the noise impact of the mixers, IF amplifiers and improve the receiver's sensitivity, but too much gain will lead to the saturation and non-linearity of the mixer. Typically, the gain of the LNA stage is no more than 25 dB. Meanwhile, the noise figure of the first stage of the path determines the overall noise characteristics. Hence, if the overall RF frontend circuit's noise figure keeps being lower than 5 dB, the total noise figure of the LNA and mixer has to be lower than 3.5 dB[14, 15]. In addition, the difference between the GNSS receiver and other RF receiver systems lies in the fact that the received signal power is maintained at a certain level, so there is no need to consider that the distance to the signal source has impacts on the receiver's dynamic range. The different dynamic ranges caused by the mode switch can be adjusted by AGC, of which a 55 dB dynamic range is enough to meet the application's needs. It is also noted that the integrated image rejection ratio is not higher than 40 dB normally.

3. Circuit design

In this section, the design and the implementation of the RF front-end are described in details as three parts: the LNA, mixers and auxiliary circuits for image rejection and output to the filtering stage.

3.1. Low noise amplifier

The specifications of the LNA are a low noise figure, high voltage gain and enough linearity. The mainstream cascode LNA and its small signal model are widely discussed[16–19], which provides 50 Ω input impedance to the antenna, reduces the Miller effect, improves the reverse isolation and increases the stability. An improved single-end structure and single on-chip spiral inductor cascode structure prototype for the multi-band applications is proposed in our design[20]. An extra capacitor group $C_{ext,n}$ is added between the source and the gate

Table 3. Parameters for dual-band LNA sitting.

Parameter	Band 1 f_1 = 1.27 GHz	Band 2 f_2 = 1.575 GHz
L_{bw} (pH)	~ 600, provided by bondwire	~ 600, provided by bondwire
L_s (pH)	~ 600, provided by bondwire	~ 600, provided by bondwire
L_g (nH)	16.8	16.8
C_m (pF)	1.5	1.5
$V_{brf,n}$ (V)	$V_{brf,1}$ = 0.585	$V_{brf,2}$ = 0.549
$C_{ext,n}$ (fF)	$C_{ext,1}$ = 450	$C_{ext,2}$ = 96
L_{tank} (nH)	6.65	6.65
$C_{tank,n}$ (pF)	C_{tank1} = 2.134	C_{tank2} = 1.120
Tail current (mA)	3.62	2.17
Simulated/Measured noise figure (dB)	0.325/1.66	0.358 /1.62
Voltage gain (dB)	21.69	21.83

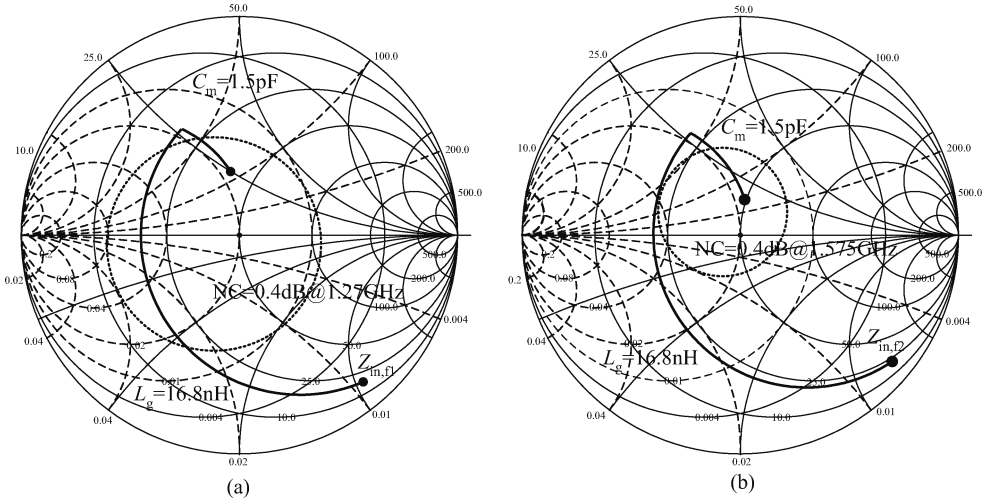

Fig. 3. Input impedance matching in the Smith chart for (a) 1.27 GHz operation and (b) 1.575 GHz operation.

of the short channel MOSFET M1 as the compensation for the downsizing of the MOSFET for the input match on different bands. The proposed LNA is shown in Fig 2. The appropriate band can be easily chosen by switching the settings.

As we discussed before in Ref. [20], the input impedance on frequency f_n (n = 1, 2, …), which is defined as $Z_{in,fn}$, can be adjusted for matching by switching the $C_{ext,fn}$ and $V_{brf,n}$ on different bands. Meanwhile, the $g_{m,n}$ of M1 is changed by switching the $V_{brf,n}$ (n = 1, 2, …) on different bands, which will lead to the change of tail current and the module power consumption.

The source impedance provided by the signal source, L-type matching network, ESD and bond wire is defined as Z_s. Z_s is decided by frequency ω_n, C_m, L_{bw} and L_g. Generally, the value of L_{bw} is fixed by the length of bondwire, and values of L_g and C_m are basically unchanged when the work frequency does not change significantly. The Z_s value only varies with a change in frequency.

When Z_s and Z_{in} reach a conjugate match, the optimal simultaneous power and noise matching are achieved by adjusting the combination of $C_{ext,fn}$ and $V_{brf,n}$. The equation set can be established for different bands' matching, The solutions are the best device parameters. It is noted that trade-offs between the best noise and power performances will lead to a little mismatch, which requires careful consideration by simulating and selecting the variables.

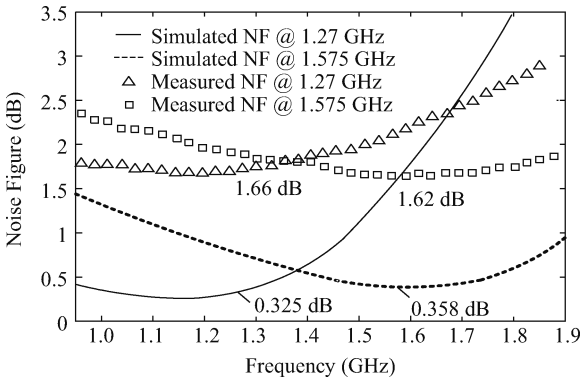

Fig. 4. Simulated and measured noise figure of 1.27 GHz operation and 1.575 GHz operation.

Our practical circuit is designed to work on two frequencies f_1 = 1.27 GHz and f_2 = 1.575 GHz. The value of parameters L_{bw}, L_s, L_g, C_m, $V_{brf,n}$ and $C_{ext,n}$ (n = 1, 2) are given in Table 3. The tail currents and noise figures can be easily determined. As shown in Figs. 3(a) and 3(b), the Smith charts depict the simulations of input impedance match from $Z_{in,fn}$ to $Z_{s,fn}$ (n = 1, 2) with the same values of L_g and C_m. Both matching points fall within the noise circle of 0.4 dB but are not far from 50 Ω, which are good trade-offs between the 50 Ω input impedance and best noise impedance. Figure 4 shows that both

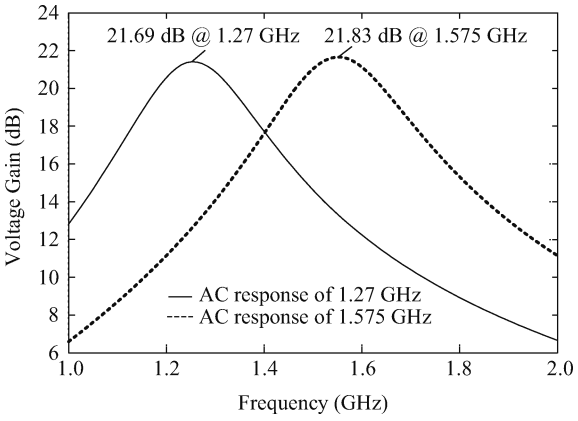

Fig. 5. Voltage gain of different frequency bands.

simulated and measured noise figures of two bands keep in the same level, even though the measured ones are much higher.

The parallel composition of an LC tank and mixer and post-stage circuit is implemented as the output load. The two mixers are capacitively coupled to the output of the LNA stage. The value of $C_{\text{tank},n}$ ($n = 1, 2$) can be switched to adjust the resonant point to the working band. The output load Z_{load} can be expressed as

$$Z_{\text{load},n} = \frac{1}{\dfrac{C_{\text{tank},n} R_{\text{p}}}{L_{\text{tank},n}} + \text{j}\left(\omega_n C_{\text{tank},n} - \dfrac{1}{\omega_n L_{\text{tank},n}}\right)} \Big|\Big| \text{Load}_{\text{mixer}}, \quad n = 1, 2, \tag{1}$$

where R_{p} is the equivalent serial parasitic resistance. The simulation shows that the impedance provided by mixers $\text{Load}_{\text{mixer}}$ are about (970 – j90) Ω on both bands, which can help to determine the value of $C_{\text{tank},n}$. The quality factor Q of the LC tank is mainly decided by L_{tank}, which is fixed by using the on-chip spiral inductor. The value of Q is much lower than the off-chip component, which ensures enough gain flatness on a span of about 200 MHz. When resonating, the LNA voltage gain can be expressed as

$$\begin{aligned}\text{Voltage Gain}_{\text{f}n} &= \left|\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}}\right| \\ &= \frac{g_{\text{m}} |Z_{\text{load},n}|}{\sqrt{\left[\omega_n^2 \left(C_{\text{gs}} + C_{\text{ext},n}\right) L_{\text{s}} - 1\right]^2 + \left(\omega_n L_{\text{s}} g_{\text{m}}\right)^2}} \\ &\approx g_{\text{m}} |Z_{\text{load},n}| = g_{\text{m}} \left|\frac{L_{\text{tank}}}{C_{\text{tank},n} R_{\text{p}}} \Big|\Big| \text{Load}_{\text{mixer}}\right| \\ &= \frac{W}{L} \mu C_{\text{ox}} \left(V_{\text{brf},n} - V_{\text{T}}\right) \left|\frac{L_{\text{tank},n}}{C_{\text{tank},n} R_{\text{p}}} \Big|\Big| \text{Load}_{\text{mixer}}\right|, n = 1, 2.\end{aligned} \tag{2}$$

This means that the voltage gain is the function of $V_{\text{brf},n}$, while other parameters are fixed. The value settings of L_{tank} and $C_{\text{tank},n}$ are also shown in Table 3. Figure 5 shows that the LNA can maintain a good gain on the same level on both bands.

The simulation and measurement results confirm the feasibility of the design. Compared to the structure discussed in Ref. [20], the additional bias voltage switch reduces the mismatching between the noise and power and keeps the output voltage gain on the same level, but results in different power consumptions on two bands.

3.2. Downconversion mixer

The downconversion mixer is used to convert the RF signal down to an intermediate frequency (IF) by mixing the RF signal from the LNA with the local oscillator (LO) signal. This allows channel selection and gain control at lower frequencies where high quality-factor (Q) filters and variable-gain amplifiers can be constructed economically. The mixer proposed here is an improved structure based on the traditional double balance Gilbert cell shown in Fig. 6. The mixer needs to be compatible with an adequate span in both RF and IF in our system for the multiply bands switching. What's more, the noise figure, linearity and voltage gain should not change dramatically on each band.

The LO signal connected to the mixer through a buffer is to isolate the LO noise and to strengthen the drive capability. In this way, the RF signal can be downcoverted to a certain IF. Meanwhile, the mixer is reused under different IF requirements. A RC network is used as the mixer's load due to its low-pass character. The transconductance stage consists of M1 and M2, and the current commutating switching pairs consist of M3–M6. In addition, the current bypass paths branch path1 and path2 are added to improve the performance.

The single-ended LNA output is capacitively coupled to one terminal of the mixer's differential RF input while another terminal of the mixer is capacitively coupled to AC ground. Compared to differential connection, this architecture reduces the current consumption and keeps the circuit simple, even though the equivalent differential input voltage,

$$U_{\text{id}} = \frac{U_{\text{RF}_{\text{IN}}}}{2}, \tag{3}$$

is half of the differential drive mode, indicating that there is a 3 dB gain loss of the entire RF frontend. However, the full advantages of the differential circuit are taken[21].

3.2.1. Convert gain

On the one hand, the conversion gain G_{v} of the double balance mixer, which is determined by the transconductance g_{m} of M5 or M6, can be given by

$$G_{\text{v}} = c g_{\text{m}} R_{\text{L}}, \tag{4}$$

where c is the conversion gain of the switch pair and R_{L} is the load of the mixer. There is

$$c \approx \frac{2}{\pi} \frac{\sin(\pi \cdot \Delta f_{\text{LO}})}{\pi \cdot \Delta f_{\text{LO}}}, \tag{5}$$

where Δf_{LO} is the time period of the U_{LO} turning from positive to negative threshold. For the larger LO signal, Δf_{LO} is smaller, and c approaches $2/\pi$. It is observed that c increases as the current I_{b} decreases and as the U_{LO} amplitude increases[22]. Thus, leaving the input driver stage current unchanged, decreasing the current of the switching pair improves the conversion gain.

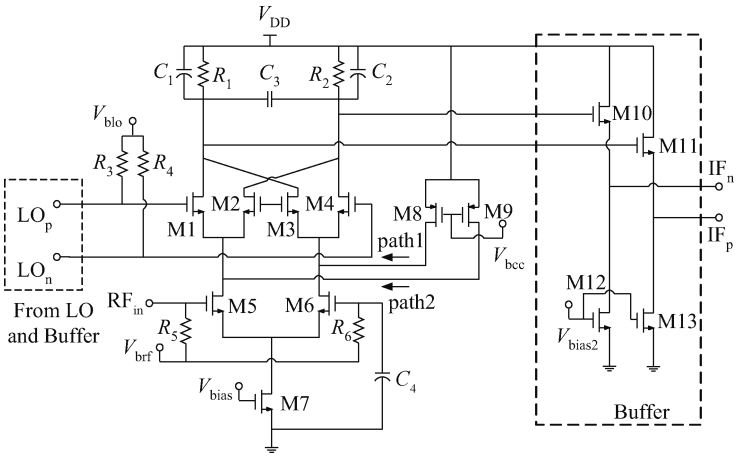

Fig. 6. Schematic of proposed down-conversion mixer.

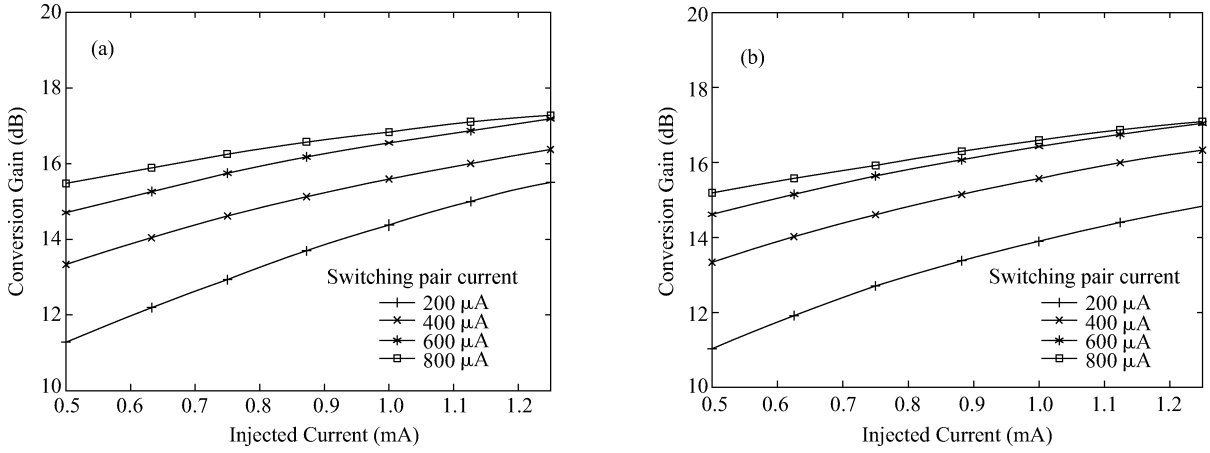

Fig. 7. Simulated conversion gain with fixed tail current but increasing ratio between injection bypass current and switching pair current of (a) 1.27 GHz-RF 50 MHz-IF operation and (b) 1.575 GHz-RF 2 MHz-IF operation.

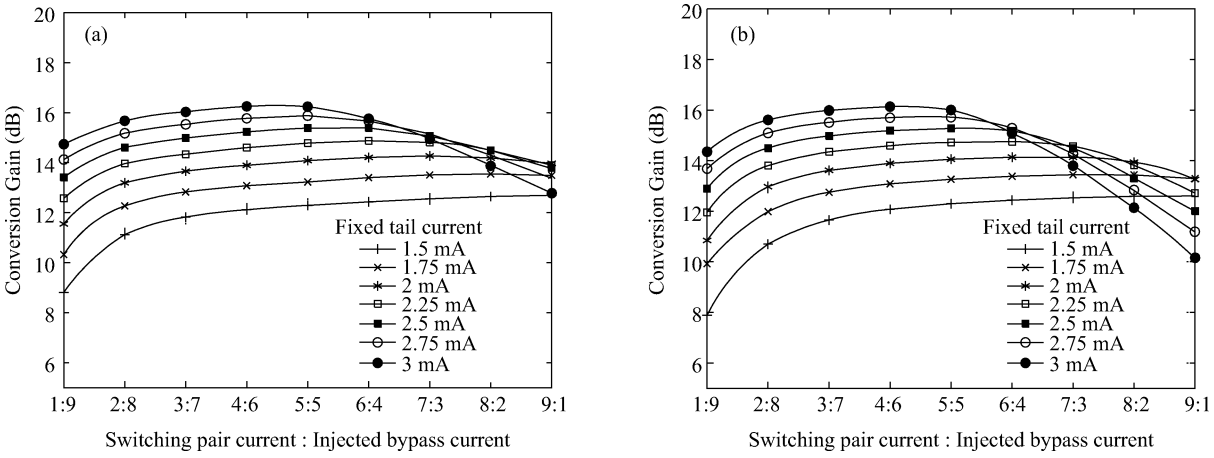

Fig. 8. Simulated noise figure with fixed switching pair current but increasing inject bypass current of (a) 1.27 GHz-RF 50 MHz-IF operation and (b) 1.575 GHz-RF 2 MHz-IF operation.

On the other hand, g_m is the transconductance of the driver stage. There is

$$g_m = \sqrt{2W\mu C_{ox} I_d}. \quad (6)$$

Without changing the bias condition of the switching pairs, increasing the inject bypass current of path1 and path2, I_d, g_m and conversion gain increases. By comparing Figs. 7(a) and 7(b), it should be noticed that the conversion gain is not sensitive to the frequency but to the ratio of the current. As shown in Figs. 8(a) and 8(b), when the tail current keeps a constant, we

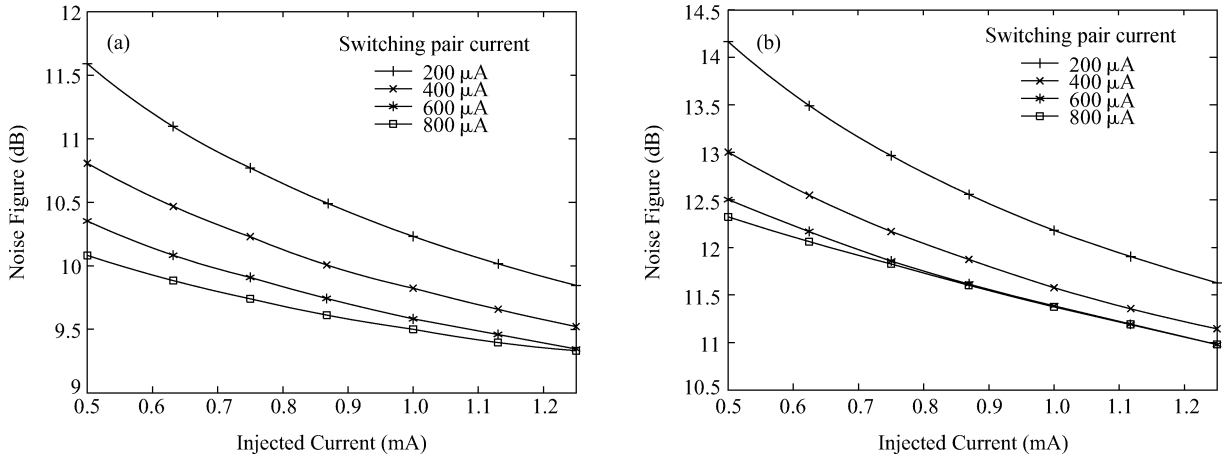

Fig. 9. Simulated noise figure with fixed switching pair current but increasing inject bypass current of (a) 1.27 GHz-RF 50 MHz-IF operation and (b) 1.575 GHz-RF 2 MHz-IF operation.

could select the appropriate ratio of bypass current and switching pair current. The optimum conversion gain can be achieved and located on a ratio of 3/7–4/6, in general. The simulation result shows agreement with our analysis.

3.2.2. Noise figure

Since the noise is transferred from multiple bands to IF output, the mixer is a significant noise contributor. The noise of the Gilbert cell mixer is composed of the noise from the driver stage, thermal noise from the switching pair and the noise from the LO port. The single-sideband noise of the double-balanced mixer can be derived from the single-balanced mixer, which is discussed in detail in Ref. [22].

The PSD of noise introduced by the driver stage transferred to the output is

$$S^{\mathrm{o}}_{\mathrm{v},56} = \alpha \cdot 4kT \left(R_{\mathrm{S}} + 2r_{\mathrm{g}} + \frac{2\gamma}{g_{\mathrm{m}}} \right) (g_{\mathrm{m}} R_{\mathrm{L}})^2 . \tag{7}$$

The PSD of thermal noise of switching pairs at the output is

$$S^{\mathrm{o}}_{\mathrm{v},12}(f) = \frac{32kT}{\pi} \frac{I_{\mathrm{B}}}{V_{\mathrm{O}}} R_{\mathrm{L}}^2 . \tag{8}$$

Of the extra current path path1, path2, the currents are controlled by the PMOS M8 and M9, which are the main contributors from where noise comes[23]. The noise of the extra path is considered as channel thermal noise in each path, which can be expressed as

$$S^{\mathrm{o}}_{\mathrm{v},8} = \alpha \cdot 4kT\gamma \sqrt{2\mu_{\mathrm{p}} C_{\mathrm{OX}} \frac{W}{L} I_{\mathrm{D}}} R_{\mathrm{L}}^2, \tag{9}$$

where I_{D} is the current of each path.

The PSD of total noise on the output port can be expressed as

$$\begin{aligned} S^{\mathrm{o}}_{\mathrm{v,total}} = {} & \alpha \cdot 4kT \left(R_{\mathrm{S}} + 2r_{\mathrm{g}} + \frac{2\gamma}{g_{\mathrm{m}}} \right) (g_{\mathrm{m}} R_{\mathrm{L}})^2 \\ & + \frac{32kT}{\pi} \frac{I_{\mathrm{B}}}{V_{\mathrm{O}}} R_{\mathrm{L}}^2 \\ & + \alpha \cdot 8kT\gamma \sqrt{2\mu_{\mathrm{p}} C_{\mathrm{OX}} \frac{W}{L} I_{\mathrm{D}}} R_{\mathrm{L}}^2 \\ & + 4kT(4r_{\mathrm{g1}}) \overline{g'^2_{\mathrm{m}}} R_{\mathrm{L}}^2 + 8kTR_{\mathrm{L}}, \end{aligned} \tag{10}$$

where

$$\begin{aligned} R_{\mathrm{L}} &= R_{1,2} \parallel \frac{1}{2\mathrm{j}\omega C_3} \parallel \frac{1}{\mathrm{j}\omega C_{1,2}} \\ &= \frac{R_{1,2}}{1 + \mathrm{j}\omega R_{1,2}(C_{1,2} + 2C_3)}. \end{aligned} \tag{11}$$

The last two items of the formula $4kT(4r_{\mathrm{g1}})\overline{g'^2_{\mathrm{m}}} R_{\mathrm{L}}^2$ and $8kTR_{\mathrm{L}}$ are the noise PSD provided by the LO and loads and are transferred to the output respectively. Increasing the bypass current without changing the switching pair current, the noise figure decreases due to the increase in the total current, as shown in Figs. 9(a) and 9(b).

However, since the tail current is constrained by the consuming plan, the addition of path1 and path2 increases the transconductance stage current but reduces the current in the switching pair. This means that choosing the appropriate bypass current percentage of the total bias current, the optimal noise figure can be achieved between the current ratio of 2/8 and 5/5, as shown in Figs. 10(a) and 10(b). The simulation helps to determine the selection of the current for the better noise figure.

3.2.3. Linearity

The large bias current improves the conversion gain but causes the large voltage drop on R_{L} and decreases the mixer linearity. The extra current paths in our design allow the bias current to be adjusted easily without affecting the current crossing the switching pair. This is a particular improvement on the linearity[24].

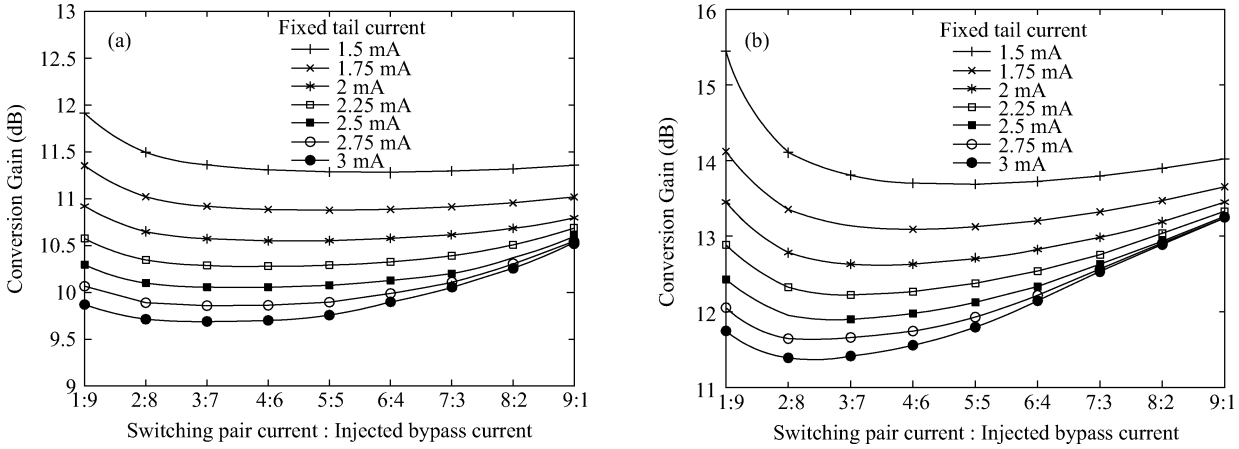

Fig. 10. Simulated conversion gain with fixed tail current but increasing ratio between inject bypass current and switching pair current of (a) 1.27 GHz-RF 50MHz-IF operation and (b) 1.575 GHz-RF 2 MHz-IF operation.

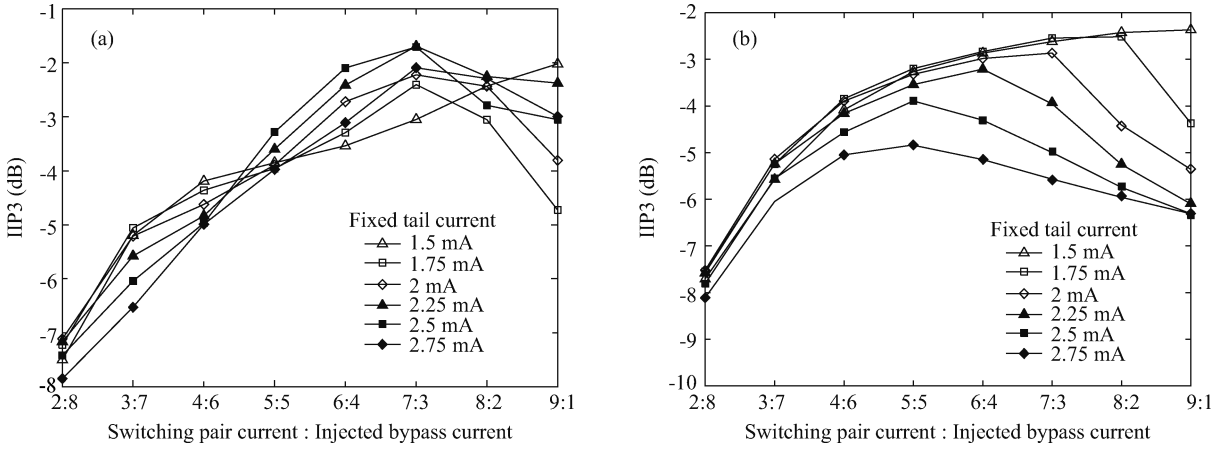

Fig. 11. Simulated IIP3 with fixed tail current but increasing ratio between inject bypass current and switching pair current of (a) 1.27 GHz-RF 50 MHz-IF operation and (b) 1.575 GHz-RF 2 MHz-IF operation.

In Ref. [25], the relation between the linearity and the tail current is discussed. There is

$$\mathrm{IIP_3} \approx \mathrm{dB}_{20}\sqrt{\frac{16I_{\mathrm{SS}}}{3K_3}}, \tag{12}$$

when the tail current I_{SS} is large, and a large signal model is implemented in the Gilbert mixer design. However, considering input nonlinear impedance components, capacitance C_{gs} and C_{gd}, nonlinearity of transconductance of the transistor for low current density and other factors, IIP3 changes slightly by adjusting the tail current. The simulations in Figs. 11(a) and 11(b) show that when the bypass current increases in proportion to the tail current, the linearity of the mixer increases slightly in some degree.

3.2.4. Wideband characters

The loads of the mixer are implemented by RC tanks, which filter the high-frequency harmonics on the IF band. The cutoff frequency can be expressed as

$$\omega_0 = \frac{1}{R_{1,2}(C_{1,2} + 2C_3)}. \tag{13}$$

As discussed above, this improved structure is well applicable up to the gigahertz frequency rage for our applications. We select different RF frequencies from 1.1 to 1.7 GHz and different IF frequencies from 2 to 50 MHz, respectively. The characteristics of noise, conversion gain and linearity are not sensitive to the range of RF and IF but to the ratio of the path currents.

3.3. Auxiliary circuits

A passive sequence asymmetric polyphase filter with following summing circuit, which splits the RF signal into components, is implemented for image rejection. And the image part is rejected as real and image parts have the same frequency but opposite phase sequence after quad differential quadrature down-conversion[26]. The image-suppressed signal is then sent to the intermediate frequency filter and other processes.

In Fig. 1, the current operating frequency is selected by a group of channel selection switches. For different IF channels, each polyphase filter sets a different number of stages. The higher the image-suppressed bandwidth and the larger the image rejection desired, the more stages are needed in cascade. For example, the 20 MHz bandwidth and 50 MHz IF appli-

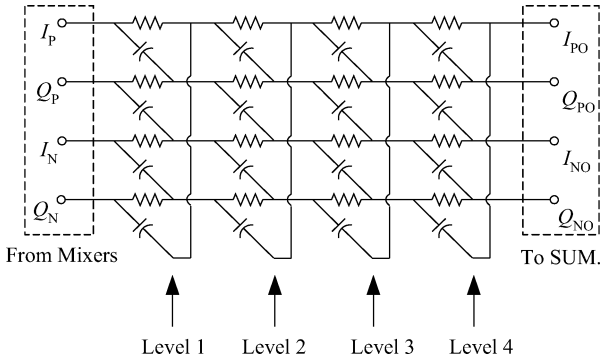

Fig. 12. Schematic of proposed polyphase filter.

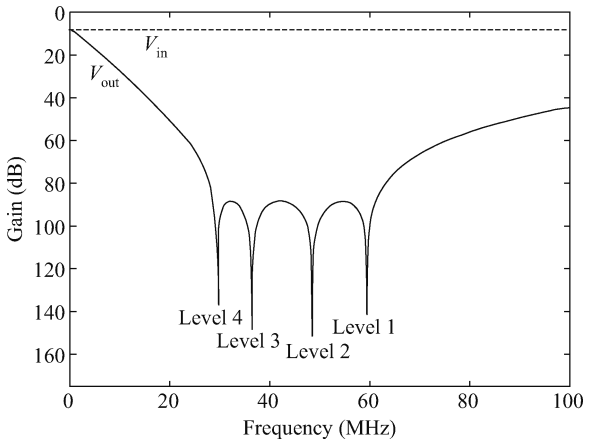

Fig. 13. Response of proposed four-stage RC polyphase filter.

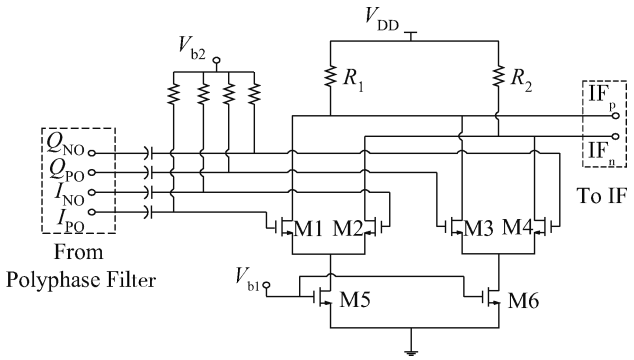

Fig. 14. Schematic of the proposed summing circuit.

cation needs a four-stage polyphase filter set. The polyphase filter circuit, as shown in Fig. 12, delivers better than 75 dB image rejection over the desired frequency band on simulation and achieves better than 30 dB in actual measurement. And the cascade response of the filter is shown in Fig. 13. For the on-chip RC time constant, it may have a 25% error. To offset this effect, the designed bandwidth of one channel must be with ±25% added on as a margin. Similarly, for a 2 MHz bandwidth GPS channel, only a two-stage polyphase filter can meet the needs.

There are two ways to terminate the polyphase filter cascade in order to obtain a differential output. One way is to terminate one outputting pair in dummies that will loss 3 dB of the gain. Consequently, an active summing circuit is used, which can provide an additional 6–10 dB gain, as shown in Fig. 14.

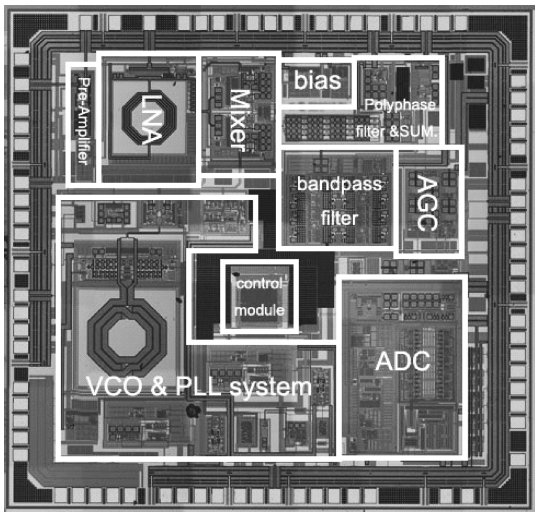

Fig. 15. Micrograph of the complete receiver chip.

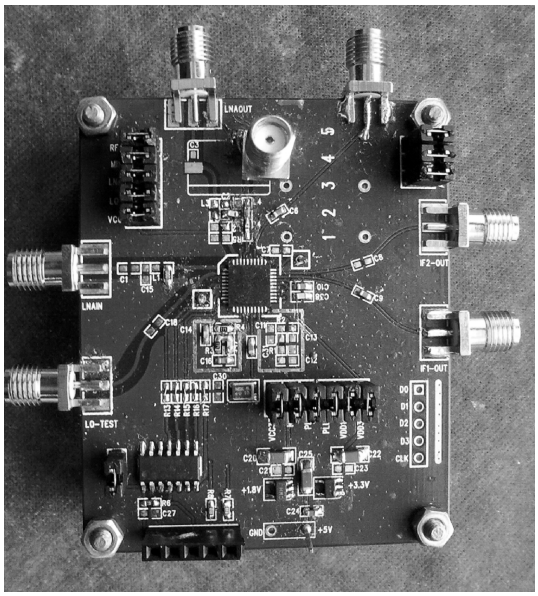

Fig. 16. Test board with the chip.

4. Measurement and discussion

The test chip is fabricated with 0.18 μm RF CMOS technology. Two typical frequency bands are adopted. One channel is 1575 MHz on the carrier frequency and 4 MHz on the IF with a 2 MHz bandwidth; another channel is 1270 MHz on the carrier frequency and near 50 MHz on the IF with a 20 MHz bandwidth. Figure 15 shows the micrograph of the chip with an area of 2.45 × 2.36 mm^2 with pads and ESD, of which the RF frontend only occupied 1.91 × 0.53 mm^2 with bias block. Figure 16 shows the test board with the chip.

The parameters of the single module are hard to measure directly in the whole chip. The working status can be evaluated from each module's current. It is seen from Table 4 that measured current values and simulated ones maintain good consis-

Table 4. Power consumption of frontend models.

Parameter	Working current (mA)	
	Simulated value	Typical measured value
Pre-amplifier (optional)	3.72	3.80
LNA	3.62 (1.27 GHz)	3.50 (1.27 GHz)
	2.17 (1.575 GHz)	2.03 (1.575 GHz)
Mixer	3.10 × 2	2.95 × 2
Polyphase filter & SUM	0.12	0.12
Total consumption	13.66 (1.27 GHz)	13.32 (1.27 GHz)
	12.21 (1.575 GHz)	11.85 (1.575 GHz)

Table 5. Correspondence value of MCy and yield.

Parameter	Ref. [2]	Ref. [3]	Ref. [4]	Ref. [5]	Ref. [6]	This work
Process	TSMC 1P6M 0.18 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	1P6M 0.18 μm CMOS (SoP)	0.13 μm CMOS	TSMC 1P4M 0.18 μm CMOS
Support voltage (V)	1.8	1.2	1.2	1.8	1.2	1.8
Architecture	Low-IF	Low-IF	Low-IF and wideband low-IF	Low-IF	Low-IF	Low-IF
RF section structure	Separated LNA, separated mixer, and separated IF	Separated LNA, separated mixer, and fixed LO	Separated LNA, shared mixer and a extra mixer, and separated IF	Separated LNA, shared mixer, and broadband IF	Separated LNA, separated mixer for each band	Shared LNA and mixers, variable LO and separated IF
Block noise figure (dB)	4.1/4.5/5.1	4.3/4.5	8 (total receiver)	2.4	2.3/2.2 (only LNA)	3.35/3.9
Gain (dB)	26/33/21.4	112/115 (total receiver)	27.9	> 40 Total 117	16 (LNA) Total 110	45/43
P_{1dB}	N/A	–75 dBm / –78dBm (input)	–25 dBm	–38 dBm	N/A	–42 dB / –44 dB
IIP3	–18.1 dBm / –20.4 dBm / –23.1 dBm	N/A	–15 dBm	> −9 dBm (LNA) / –30 dBm (LNA+Mixer)	N/A	–32 dB /–34 dB
Compatible bands (MHz)	GPS / WCDMA / Bluetooth	GPS L1 / GPS L2	1176–1278	GPS L1 / L5/ Galileo E1 / E5A	GPS L1 / L5 / Galileo L1F / E5a	GPS L1 / 1270 / etc.
IF frequency (MHz)	2/2/2	4.092/4.092	66–168	3.25/3.42	N/A	4.092/50
IF bandwidth (MHz)	N/A	2/2	2–50	9	4.53/24	2/20
Active area (mm^2)	2.4 × 2.4 (total die size)	N/A	20	N/A	3 × 3.8	1.91 × 0.53 of total 2.45 × 2.36
Power consumption (mW)	2.5–3.5	12 (total receiver)	100	54	12.3 mA × 1.2 V	24.0/21.3

tency, implying the right working conditions of the frontend.

The reserved test-port on the RF signal input and IF band output can help to confirm the characteristics of noise figure, conversion gain, linearity,etc. After optimal adjustment and trade-off of the off-chip matching network, the band noise figure can achieve an average level of 3.35 dB on 50 MHz ±10 Hz of band 1.27 GHz, and 3.9 dB on 4 MHz ± 1 Hz of band 1.575 GHz. The conversion gain can be adjusted in a span of 5 dB and centered at 45 dB of band 1.27 GHz and 43 dB of band 1.575 GHz by tuning on the working current. And the band flatness is better than 1.5 dB for band 1.27 GHz and better than 1 dB for band 1.575 GHz. The image rejection is about 32 to 29 dB for both bands. The P_{1dB} of the two bands is shown in Fig. 17, and the IIP3 of the frontend can be estimated to be about 10 dB higher than P_{1dBs}, which is about –32 dB for band 1.27 GHz and –34 dB for band 1.575 GHz.

Table 5 compares the proposed frontend and recently reported multi-band CMOS receiver's frontend. It can be seen that only the single RF path implemented in our design has less die area and less power consumption but shows a better or equal performance, which indicates the high flexibility and availability in the multi-band compatible receiver and GNSS applications.

5. Conclusion

In this study, the receiver requirements for multi-band GNSS on an L-band were derived. A simplified RF signal path

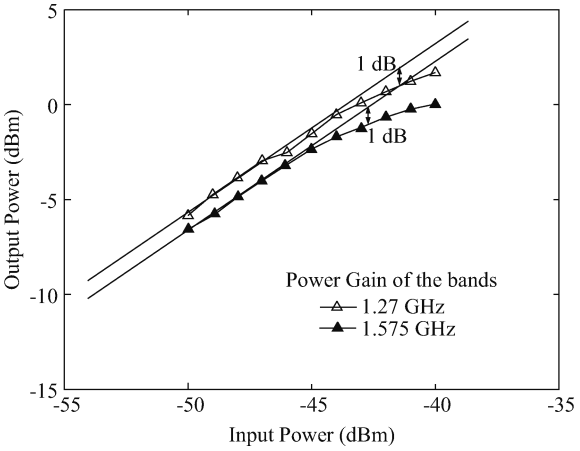

Fig. 17. Power gain and the $P_{1\mathrm{dB}}$ of the frontend blocks.

with an improved cascode LNA and a wideband downconversion mixer was implemented in a low-IF architecture. The image was rejected by different polyphase filters and IF signals were processed in different channels for the different bandwidth requirements by selecting switches. All of these reduced the die area and power consumption significantly. An experimental dual-band receiver chip on 1.27 GHz (50 MHz bandwidth) and 1.575 GHz (2 MHz bandwidth) was fabricated by a CMOS 0.18 μm RF process. The experimental results show that the proposed frontend structure can satisfy the demands of GNSS multi-band applications.

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