A low power and low distortion rail-to-rail input/output amplifier using constant current technique*

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Abstract: A rail-to-rail amplifier with constant transconductance, intended for audio processing, is presented. The constant transconductance is obtained by a constant current technique based on the input differential pairs operating in the weak inversion region. MOSFETs working in the weak inversion region have the advantages of low power and low distortion. The proposed rail-to-rail amplifier, fabricated in a standard 0.35 μm CMOS process, occupies a core die area of 75 × 183 μm^2. Measured results show that the maximum power consumption is 85.37 μW with a supply voltage of 3.3 V and the total harmonic distortion level is 1.2% at 2 kHz.

Key words: amplifier; constant transconductance; low distortion; low power; rail-to-rail
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1. Introduction

The development of portable audio systems has been towards low voltage, low power and low total harmonic distortion (THD) in recent years. Operational amplifiers as the fundamental building blocks restrict the performance of the systems. To widen the dynamic range and obtain an acceptable signal-to-noise ratio (SNR), a rail-to-rail amplifier is required in many audio applications. The general method to realize rail-to-rail input common mode range utilizes a complementary input stage with both NMOS and PMOS differential pairs in parallel. However, the transconductance of the complementary input stage varies with different input common mode voltage. The large variation in the input stage transconductance prevents frequency compensation, and induces large fluctuations in unity-gain bandwidth and severe signal distortion[1].

In order to keep transconductance constant, several design schemes have been developed, such as 1 : 3 current mirror circuit[2], bulk-driven circuit[3] and floating-gate MOSFET[4]. However, for a 1 : 3 current mirror circuit, the input stage must be operated in the active region, which increases the power consumption; a bulk-driven circuit has low transconductance, huge noise and bad AC performance; and a floating-gate MOSFET requires expensive non-standard processing steps. In this work, a constant current technique depending on the input stage operating in the weak inversion region is proposed. Using this method, the rail-to-rail amplifier possesses low power and low distortion, occupies a small chip area, and can be used in a Hz to kHz frequency audio system.

2. The proposed constant current technique

The basic structure of a rail-to-rail input and constant-g_m control stage circuit is shown in Fig. 1. The PMOS pair is composed of transistors M1 and M2 while the NMOS pair is formed by M3 and M4. The constant-g_m control circuit is achieved through transistors M7–M12. This circuit maintains a constant tail current when either of the two differential pairs goes off.

In order to describe the operation of the constant-g_m control circuit, first, it is supposed that PMOS and NMOS differential pairs are both in operation, and the transistors M5 and M6 as the tail current source provide the same current for PMOS and NMOS differential pairs, respectively. The current mirrors (M7–M12) are disabled. Next, when the PMOS differential pair (M1–M2) is on and the NMOS (M3–M4) differential pair is off, the total tail current decreases. Therefore an equal current is needed to maintain the tail current constant, which is realized by the current mirror (M10–M11). Similarly, when the NMOS (M3–M4) pair is on and the PMOS (M1–M2) pair is off, the current mirror (M7–M8) supplies the compensated tail current. Through adjusting the ratio of the width to length of the input differential pairs, the tail current can be kept constant and stable. The input differential pairs are kept biased in the weak inversion region under all conditions.

When a MOSFET works in weak inversion, the transconductance is proportional to the drain current, given by

$$g_{m,\,weak} = \frac{I_{Drain}}{nV_t}, \tag{1}$$

where I_{Drain} is the drain current of the transistor, V_t is the thermal voltage, and the weak inversion slope factor n is equal to $(C_{ox} + C_{dep})/C_{ox}$ [5]. In this paper, the constant-g_m is realized since the total tail current of the differential pairs is invariable during the whole input common mode range.

According to the description above, the transconductance can be explained by

$$g_{mp} = \frac{I_{P,\,tail}}{nV_t}, \tag{2}$$

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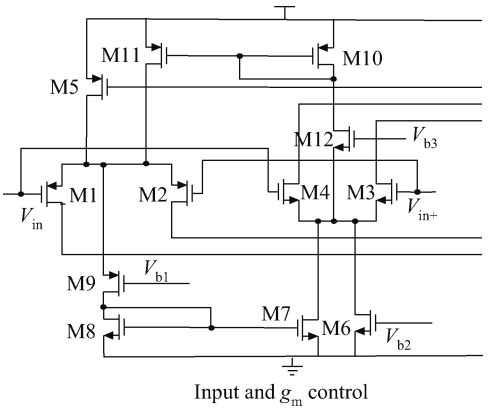

Fig. 1. Rail-to-rail input and constant-g_m control stage.

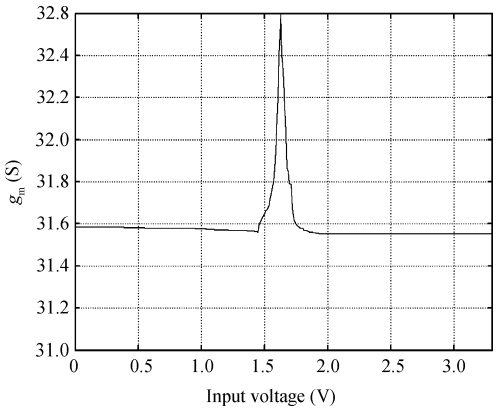

Fig. 2. Transconductance versus input common mode voltage.

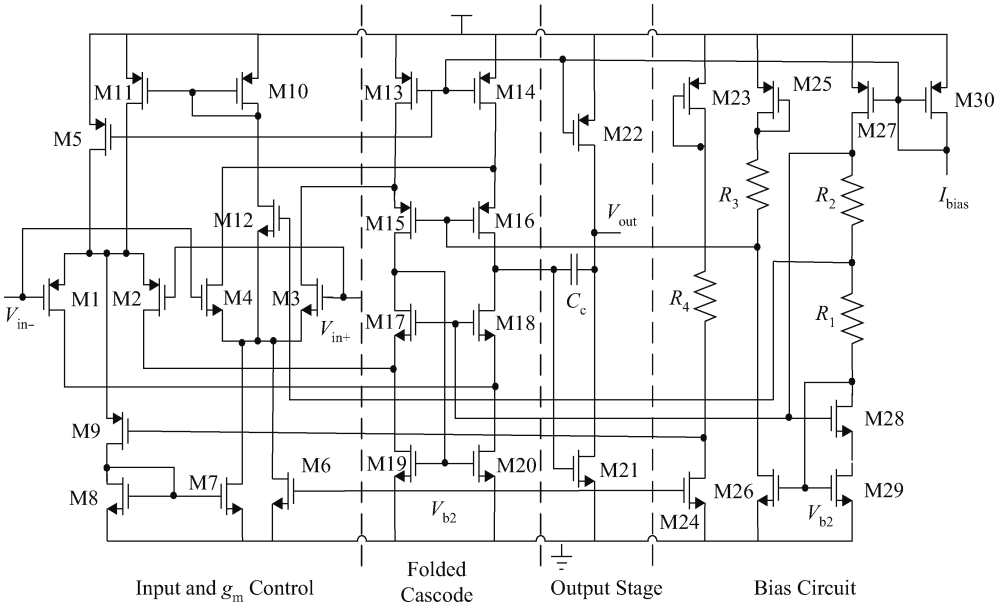

Fig. 3. Rail to rail operational amplifier application circuit architecture.

$$g_{mn} = \frac{I_{N,\,tail}}{nV_t}, \tag{3}$$

$$g_{m,\,tol} = g_{mn} + g_{mp} = \frac{I_{P,\,tail} + I_{N,\,tail}}{2nV_t} = \frac{I_{tail}}{nV_t}, \tag{4}$$

where

$$I_{P,\,tail} = I_{N,\,tail} = I_{tail}. \tag{5}$$

The simulated amplifier transconductance with different input common mode voltages is shown in Fig. 2. The variation of g_m is less than $\pm 3\%$ in the whole 0 to 3.3 V input range.

3. Circuit implementation

The overall circuit of rail-to-rail amplifier is shown in Fig. 3. It consists of a rail-to-rail input stage with constant-g_m control circuit, a high gain cascade stage, a rail-to-rail output stage and a bias circuit. The high gain cascode stage is used to enhance the gain, which comprises a common cascode stage M13–M16 and a high-swing current mirror M17–M20. The output stage, which delivers the signal effectively and decreases the distortion, is composed of a common-source amplifier with a PMOS current mirror load.

A bias circuit, as shown in Fig. 3, provides a quiescent operation point for the proposed amplifier. Usually amplifiers consume more power because of complicated bias circuits. The proposed bias circuit contains a few resistors and transistors. There are two major reasons for employing the bias circuit design. One is that the bias structure with a transistor and resistor is relatively simple. The other is that the self-cascade transistor doesn't need an additional branch to provide bias voltage for itself. Thus the power consumption of the circuit is reduced.

The rail-to-rail amplifier with the proposed constant current technique has been simulated in a standard 0.35 μm CMOS process. The open loop AC characteristics and frequency response of the rail-to-rail amplifier with input common mode voltage ($V_{i,cm}$) of 1.65 V are shown in Fig. 4.

The presented circuit is manufactured by a standard 0.35 μm CMOS process. Figure 5 shows the microscopic image of the proposed rail-to-rail amplifier with a constant current technique. The total circuit area is $75 \times 183\ \mu m^2$. With the specified load of 15 pF, the measured DC transfer characteristic of the amplifier in non-inverting unity-gain configuration is shown in Fig. 6. The results manifest that the input/output

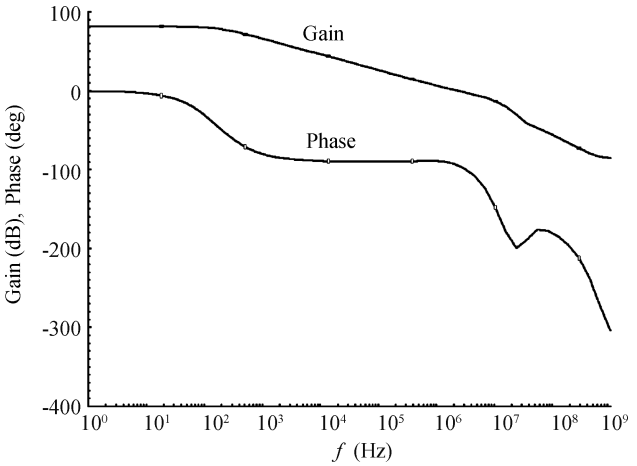

Fig. 4. AC characteristic and frequency response of the amplifier ($V_{i,cm}$ = 1.65 V).

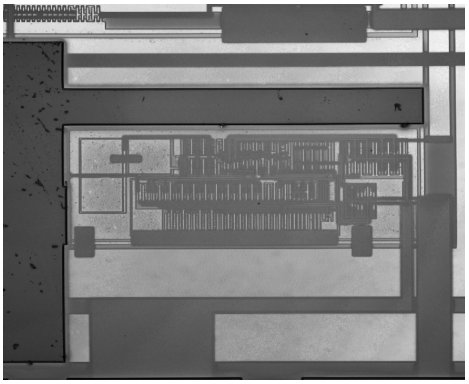

Fig. 5. Micrograph of the rail-to-rail chip.

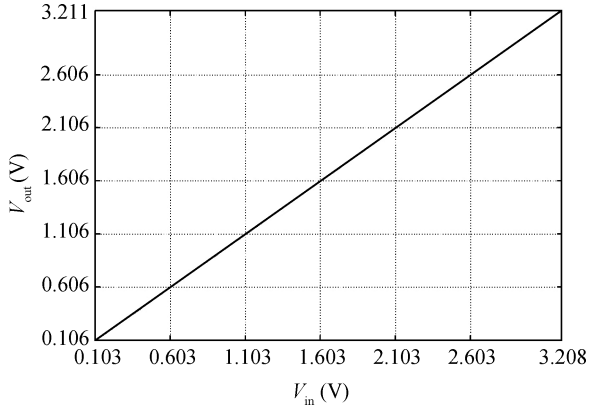

Fig. 6. Measured DC transfer characteristic of the amplifier in non-inverting unity-gain configuration.

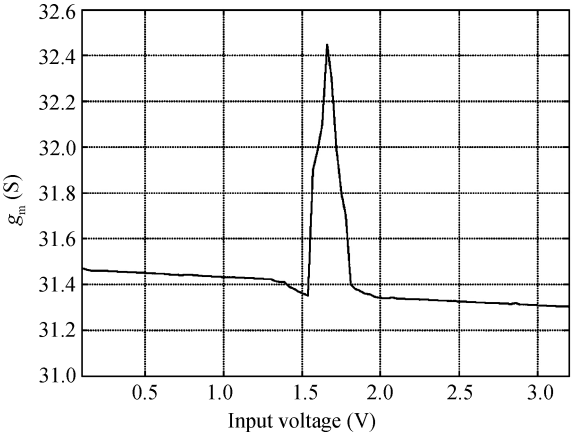

Fig. 7. Measured result of the g_m with the input voltage.

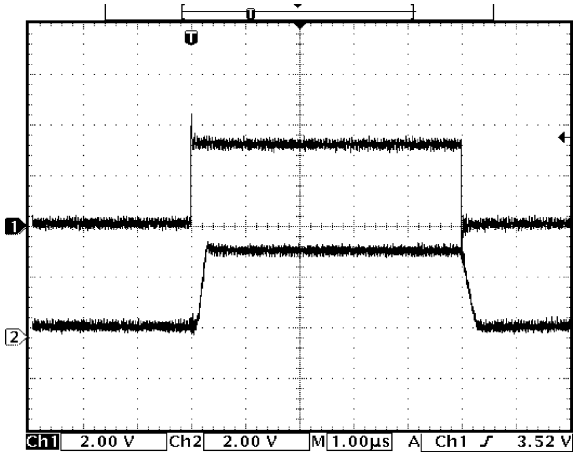

Fig. 8. Step response (upper trace: input; lower trace: output).

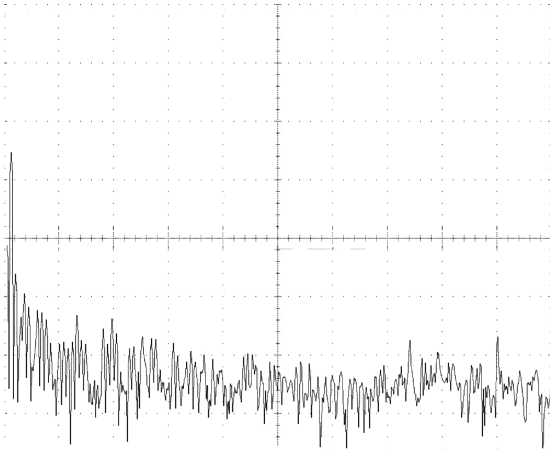

Fig. 9. Measured spectrum with a 2 kHz sinusoidal input waveform.

voltage is rail-to-rail and there is a 3 mV deviation between the output voltage with the input voltage, which causes the input offset voltage of the amplifier. Compared with the simulated result, the measured transconductance with different input voltages is shown in Fig. 7. Measurement results of step response with the input of a 3.3 V and 100 kHz square wave is shown in Fig. 8. Figure 9 shows the measured spectrum with a 2 kHz sinusoidal input signal. The measured result of THD is 1.2%. The measurement results show that the total power consumption is 85.37 μW under the supply voltage of 3.3 V.

4. Measured results and discussion

The performance of the proposed rail-to-rail amplifier compared with other circuits is summarized in Table 1. The

Table 1. Comparison of the rail-to-rail amplifiers.

Parameter	Structure in Ref. [6]	Structure in Ref. [7]	Structure in Ref. [8]	Proposed structure
Process (μm)	0.6	0.35	0.18	0.35
Supply power (V)	3	1	1.8	3.3
Constant g_m control method	1 : 3 current mirror	Bulk-drive circuit	Floating gate MOSFET	Constant current
Open-loop gain (dB)	75	76.2	40	81.5 @ $V_{i,cm}$ = 1.65 V
Phase margin (°)	70	–	77	85 @ $V_{i,cm}$ = 1.65 V
Gain bandwidth, GBW (M)	1.5	8.1	1.2	2.3
Input common mode range (V)	0–3	0–1	0–1.8	0–3.3
Output swing (V)	–	0.02–0.95	–	0–3.3
Common mode rejection ratio (dB)	–	70.5	146	130.4 @ $V_{i,cm}$ = 1.65 V
Power supply rejection ratio (dB)	–	45	69.5	82.3 @ $V_{i,cm}$ = 1.65 V
Load capacitance, C_L (pF)	5	17	10	15
FOM $\left(=\frac{\text{GBW}\times C_L}{\text{Power}}\right)$	42	385	211	405

figure of merit (FOM) of the proposed amplifier is larger than previous circuits. However, because the input stage is operated in the weak inversion region, the frequency response is relatively low. Overall, the circuit has sufficient performance for low-speed applications.

5. Conclusion

In this paper, a rail-to-rail amplifier with the input transistors operating in weak inversion is presented. This circuit has been verified in a standard 0.35 μm CMOS process. Experimental results show that the presented rail-to-rail amplifier consumes power dissipation of 85.37 μW and exhibits a total harmonic distortion of 1.2%. Measurement results have good agreement with the simulated data. The proposed rail-to-rail amplifier can be applied widely for low speed and ultra low supply voltage portable audio electronics.

References

[1] Yan S, Hu J, Song T, et al. A constant-g_m rail-to-rail op amp input stage using dynamic current scaling technique. IEEE International Symposium on Circuits and Systems, 2005, 3: 2567

[2] Hogervorst R, Tero J P, Eschauzier R G H. A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries. IEEE J Solid-State Circuits, 1994, 29(12): 1505

[3] Carrillo J M, Duque-Carillo J F, Torelli G. 1-V quasi constant-g_m input/output rail-to-rail CMOS op-amp. IEEE International Symposium on Circuits and Systems, 2003, 1(4): 161

[4] Raisanen-Ruotsalainen E, Lasanen K, Kostamovaara J. 1.2 V micropower CMOS op amp with floating-gate input transistors. IEEE Midwest Symposium on Circuits and Systems, 2000, 2: 794

[5] Hogervorst R, Tero J P, Huijsing J H. Compact CMOS constant-g_m, rail-to-rail input stage with g_m-control by an electric zenor diode. IEEE European Solid-State Circuits Conference, 1995: 78

[6] Shi Guangyuan, Mei Dangmin. Design and simulate of an amplifier with rail to rail input stage. Journal of Liaoning University Natural Sciences Edition, 2009, 36(3): 212

[7] Carrillo J M, Torelli G, Pérez Aloe R. 1-V rail-to-rail CMOS opamp with improved bulk-driven input stage. IEEE J Solid-State Circuits, 2007, 42(3): 508

[8] Farzan R, Azhari S J. Ultra low-voltage, rail-to-rail input/output stage operational transconductance amplifier (OTA) with high linearity and its application in a G_m–C filter. IEEE International Symposium on Quality Electronic Design, 2010: 231