A fully monolithic 0.18 μm SiGe BiCMOS power amplifier design*

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Abstract: A fully monolithic power amplifier (PA) for multi-mode front end IC integration is presented. The PA is fabricated in an IBM 7WL 0.18 μm SiGe BiCMOS process with all the matching networks integrated on a chip. After load-pull test to find the best power stage size and layout optimization, the measured results show that the PA can obtain a 24 dBm maximum output power at 2.4 GHz, the output 1 dB compression point is 21 dBm at 5 dBm input, and the PAE is 18%. This PA is complete on-chip tested without any bonding wires and on-board matching, targeting fully power module integration in multi-mode system on chip.

Key words: SiGe; BiCMOS; power amplifier; monolithic; multi-mode

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1. Introduction

In recent years, mobile communication handsets such as mobile phones, smart phones and personal navigation devices (PND) have followed the growing trend of multi-mode, multi-band integration in order to meet the needs of the consumer electronics market. As a key component of the front end IC (FEIC), the power amplifier (PA) has been in urgent demand for multi-mode, multi-band integration applications.

Traditional PA processes are dominated by compound semiconductors such as GaAs, InP and Si-based RFCMOS, which all offer high-speed and high-breakdown transistors. Due to the hungry power dissipation, 60%–70% battery life of mobile devices is largely shortened by the traditional PA found in an RF handset system. The main reason is that almost all the compound PAs and former Si-based PAs require off-chip matching components[1−3] (e.g. an on-board RF-choke inductor for GaAs processes), which inevitably increases cost and power consumption. Due to considerations of full integration, many monolithic multi-mode CMOS PAs have been proposed[4, 5], but they suffer from a low breakdown voltage and a lossy substrate.

In low-end constant-modulation 2G mobile applications, PAs are dominated by GaAs and RF CMOS processes. However, when 3G and 4G standards with OFDM or other linear modulation standards begin to predominate[4−7] and have been included in a multi-mode system, the trade-off with linearity, frequency margin, breakdown voltage and peak current is becoming more and more concerning.

As multi-mode monolithic FEIC and their products become increasingly popular, SiGe BiCMOS processes can provide a proper alternative to GaAs. Even up to a frequency of 10 GHz, SiGe HBT devices can operate well. Recently, several SiGe multi-band and multi-standard PA products and research works have been presented[7, 8], for example, a MIMO (multiple input multiple output) 802.11a/b/g FEIC monolithic power module includes two 5 GHz PAs, two 2.4 GHz PAs and a Rx/Tx switch integrated on one single chip[8]. A SiGe BiCMOS process is very suitable to fully integrate the multi-PA module due to its excellent thermal performance compared to GaAs, its excellent passive components for on-chip matching and the convenience of integrating the controlling digital part in the same chip.

This paper presents a fully integrated 2.4 GHz PA in IBM 7WL 0.18 μm SiGe BiCMOS process for full power module integration in a multi-mode SOC. The design fulfils the dual-mode 802.11b/g standard in order to meet the stringent linearity and power requirements. The PA integrates all matching on chip, without any external components. By topology optimization and the use of high quality passive components, we obtain a maximum output power of 24 dBm and P_{1dB} of 21 dBm at 5 dBm input, the PAE is 18%.

2. Power stage load pull test

The process offers 3 kinds of HBTs: high speed, standard performance and high voltage; the main process difference between them is the doping density. Higher collector doping extends the frequency response by increasing the current level at which unity current gain occurs (Kirk effect), but lowers BVCBO (collector–base breakdown voltage, emitter open) and BVCEO (collector–emitter breakdown, base open). So we chose a high voltage HBT for the power transistor in the power amplifying stage, whose breakdown voltage is 6 V and the peak f_T is 29 GHz, emitter current density is 0.8 mA/μm^2 at peak f_T, as shown in Table 1.

The last stage in a PA determines the output power level. Therefore the first step in PA design is, based on the corresponding power requirements and power level, to select the output stage power transistor size by load-pull simulation and test. When the monolithic PA is operating in a large signal condition, the optimal load impedance of the transistor changes as

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Table 1. SiGe HBT performance.

Parameter	Peak f_T (GHz)	I_c @ Pk f_T (mA/μm^2)	β	B_{vceo} (V)	I_e @ Pk f_T (mA/μm^2)
Value	29	0.4	140	6.0	0.8

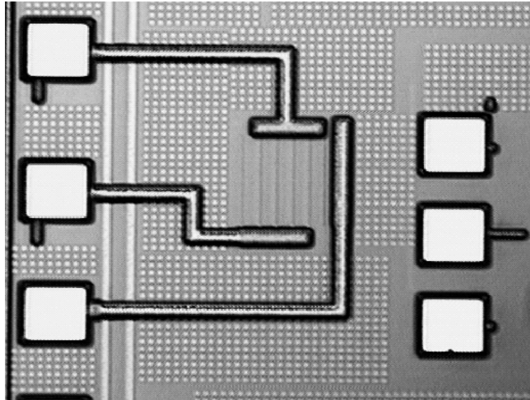


Fig. 1. Output power transistor die photo for the load-pull test.

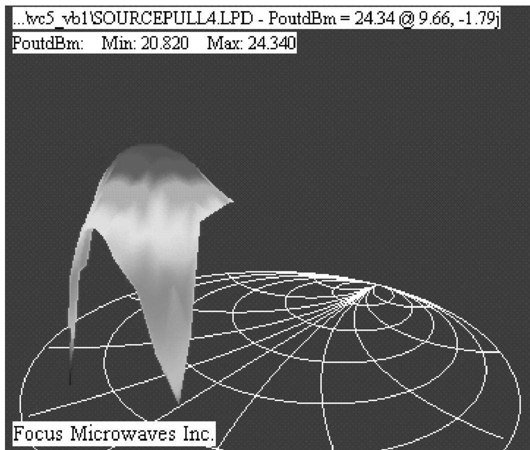


Fig. 2. Load-pull curve.

the input signal power varies. According to the WiFi standard, we simulated the source-pull and load-pull point using ADS software and took successive approximations to the matching point. Meanwhile, the peak PAE point was figured out in order to find the best matching point. Finally, the device is set to 0.48 μm × 20 × 16multi, as shown in Fig. 1. At this point we take load-pull measurements at 2.4 GHz, based on a Focus 1808 tuner system at maximum input power. The load-pull result is shown in Fig. 2. The optimized load is set to 9.66 Ω to obtain a maximum power output of about 24 dBm.

3. Circuit design

For a long time, monolithic PAs have been limited by their lossy on-chip matching networks and low-Q inductors, which dissipate most of the power and destroy output power. In addition, without good shielding, the noisy transmit spectrum will couple from the substrate to another part of the transceiver and degrade the sensitivity of FEIC. In this work, the PA is designed in the IBM 7WL 0.18 μm SiGe BiCMOS process featured in

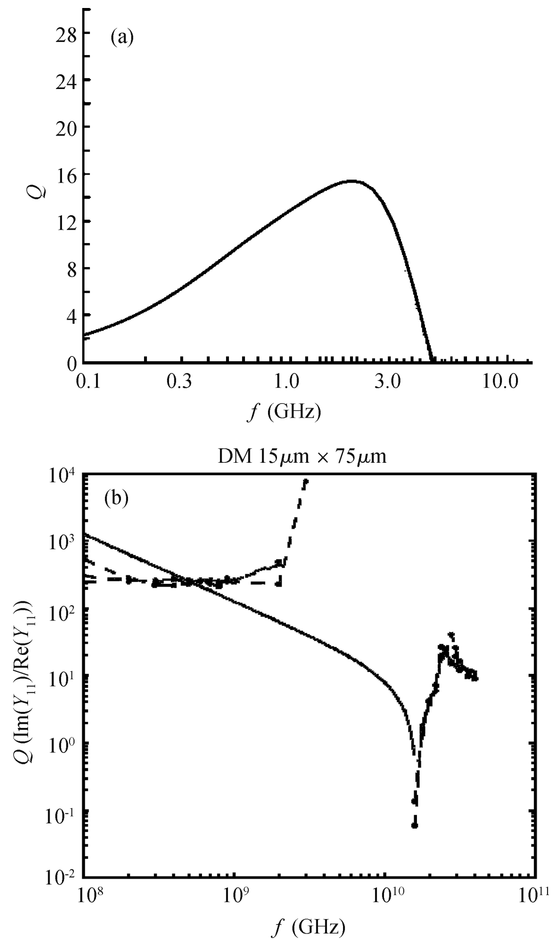


Fig. 3. Passive device performance. (a) Inductor Q value versus frequency. (b) Capacitance Q value versus frequency.

high quality passive devices. The inductor used in this work has improved skin effect loss and proximity loss, offering two kinds of shielding, and results in a high Q value (as shown in Fig. 3(a), the Q value varies with frequency and temperature is set to 27 ℃). It can be seen that, at 2.4 GHz, Q exceeds 14 at room temperature; when a special layer, of high-density MIM capacitance is used, there is a relatively high unit value of 4 fF and a high Q (Fig. 3(b)). Therefore, a monolithic PA can operate under excellent matching conditions and occupies a very small area compared to discrete matching PAs.

An adaptively linear biasing technology is adopted to realize the compensation function in this PA, whose purpose is to compensate the voltage variation of ΔV_{BE} as the input signal slightly increases.

As shown in Fig. 4, the current reference has the relationship below:

$$I_0 = I_{c1} + I_{b1} + I_{b3}, \tag{1}$$

$$V_A = V_{CC} - I_0 R_{q1}, \tag{2}$$

$$V_{BEq3} = V_A - I_{e3} R_{q3}, \tag{3}$$

$$V_{BEq1} = V_A - I_{b1} R_{q2} - V_{BEq2}. \tag{4}$$

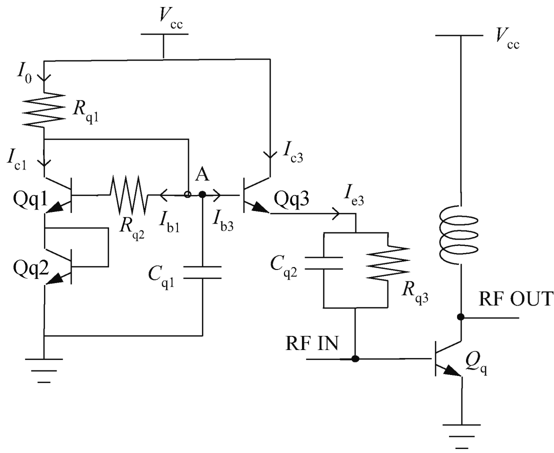


Fig. 4. Linear biasing.

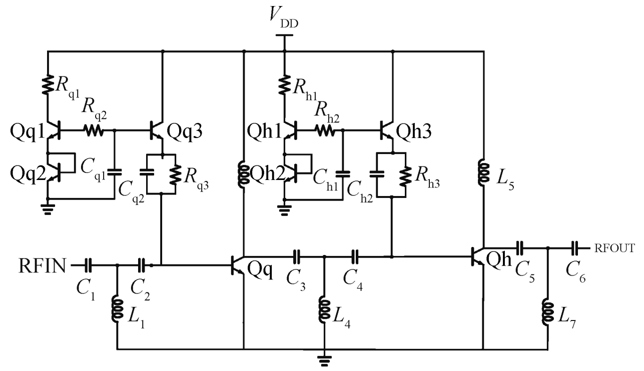
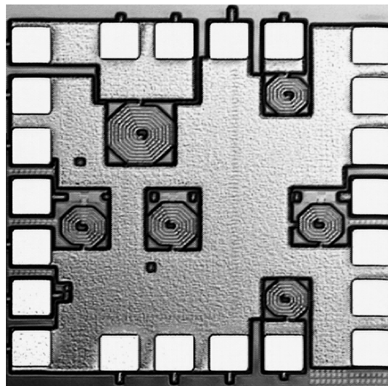
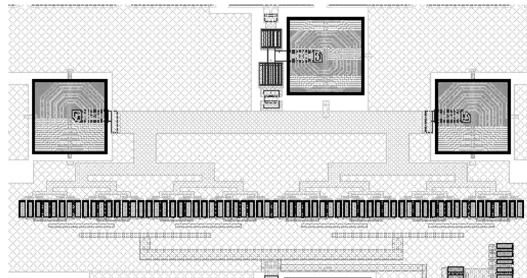


Fig. 5. Detailed monolithic PA circuit.



(a)



(b)

Fig. 6. Layout optimization. (a) Optimized layout. (b) One-side fishbone structure.

Table 2. Device size list.

Device name	Size	Device name	Size
Qq	0.48 μm × 20 × 16multi	C_5	2.4 pF
Qh	0.48 μm × 20 × 64multi	C_6	1.4 pF
C_1	1.5 pF	L_1	1.4 nH
C_2	3 pF	L_4	2 nH
C_3	1.1 pF	L_7	2.1 nH
C_4	1.6 pF		

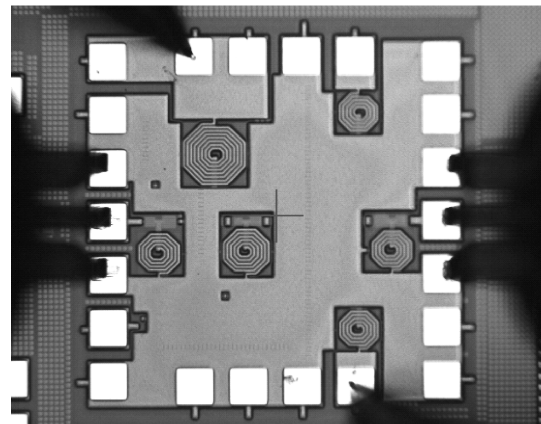


Fig. 7. On-wafer measurements.

So, when the RF signal increases, the base current of Qq3 and its base–emitter voltage decrease when the input power increases, then there is a slight increase in Qq's $V_{\rm BE}$ and the $V_{\rm A}$ is at its approximate stability due to bypass capacitor Cq1 and Qq3.

A detailed circuit diagram of the proposed monolithic PA is shown in Fig. 5. It is a two-stage power amplifying structure. The former bias network (including Qq1, Qq2, Qq3, Rq2, Cq1 and Cq2) provide the appropriate bias current to the preamplifier stage (Qq and L_3), similarly, Qh and L_5 is the power stage which provides the power output. The power stage bias network comprises of Qh1, Qh2, Qh3, Rh2, Ch1 and Ch2. So the small-signal input from the RFIN is passed through two amplifying stages and output from the port RFOUT. $C_1/C_2/L_1$ forms on-chip input matching, $C_3/C_4/L_4$ is the inter-stage matching and $C_5/C_6/L_7$ is the output matching network.

The size of the main HBT and matching devices are listed in Table 2.

The ideal maximum output power can be calculated by:

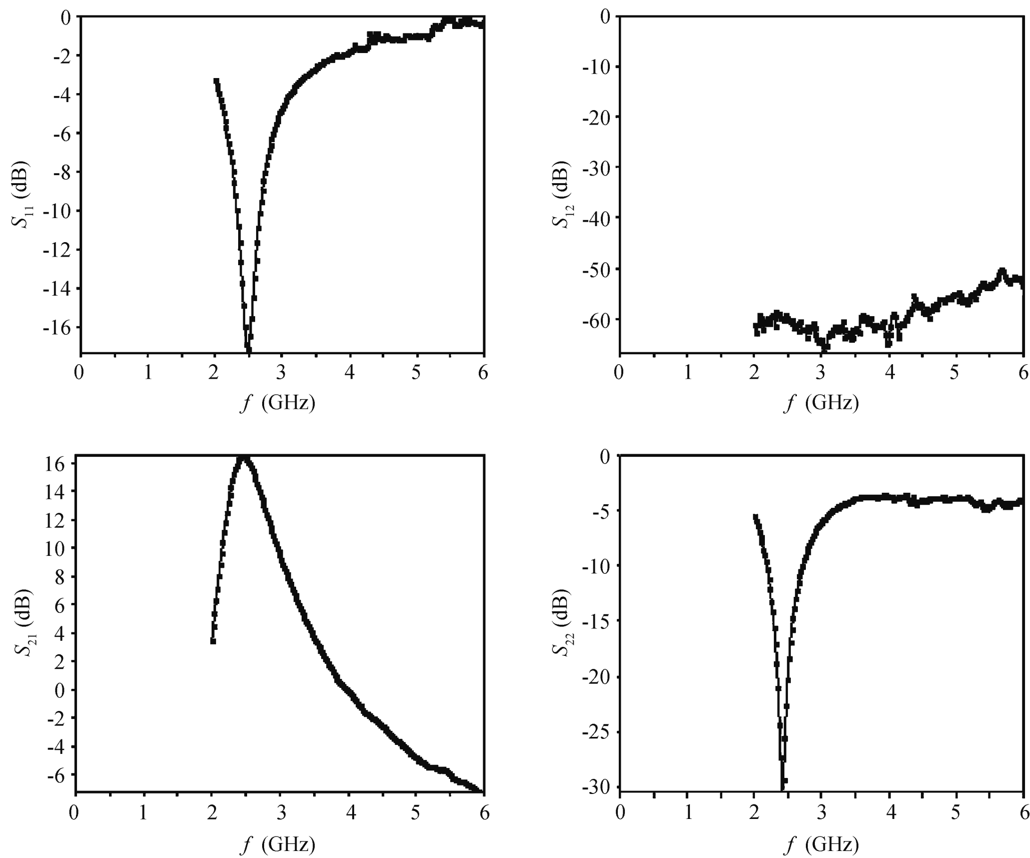


Fig. 8. Measured S parameters at 5 dBm input power.

$$Z_{\mathrm{LOAD}} = \frac{V_{\mathrm{dd}}^2}{2P_{\max}}, \tag{5}$$

$$P_{\max} = \frac{3.3^2}{2 \times 9.66} = 564\,\mathrm{mW} = 27.5\,\mathrm{dBm}. \tag{6}$$

The actual output power will be lower than that due to parasitic and matching loss.

4. Layout optimization

Layout is critical for PA design, a bad layout will destroy half of the output power or more. When not optimized at the emitter, a parasitic resistance of 5 Ω appears, and at 200 mA current bias will cause a 1 V voltage drop. Several special processes use through wafer via (TWV)[8] or sinkers[7] to obtain a low resistance substrate. In this work, we do not use a special low resistance substrate and several layout structures are implemented to reduce emitter resistance and improve power transmission.

First of all, without multiple bonding frames to reduce resistance, grounding pads are calculated by the maximum sustained current at the power stage. At the extreme condition of 600 mA, every 65 × 80 μm pad can handle a 50 mA current with a 4 μm thick top metal. We set 14 grounding pads and all the pads are connected together to further decrease emitter resistance and degeneration, and improve power gain and linearity, as shown in Fig. 6(a). Secondly, all the critical power paths are designed in a "binary feed line" or "one side fishbone" structure, which can conduct the current evenly to every HBT. Stacked metal layers and intensive vias are used to lower parasitic resistance and optimize the current crowding effect, as illustrated in Fig. 6(b). Finally, the monolithic PA has a two-stage structure, to suppress back or forward current coupling, the distributed multiple pads can form 4 RF signal rings, so the coupling can be reduced to a negligible level.

5. Experimental results

The on-wafer test photograph of the monolithic PA is shown in Fig. 7. The total occupied die area is only 1.1 m × 1.1 mm including all the passive devices and RF chokes. The PA is tested on a Cascade Microtech S300 probe station with an Agilent E4438C signal generator and an E4440A spectrum analyzer. All cable losses are included in measurements results.

An Agilent E8363B network analyzer is used for the S parameter test. Figure 8 gives a small signal gain at 2.4 GHz for a 5 dBm input read by the E8363B, which is 5 dBm higher for linear maximum power back off. The S_{21} is still higher than 16 dB and the S_{11} and S_{22} show very sharp peaks and excellent matching at 2.4 GHz below –20 dB, the S_{12} is below –50 dB, shows good isolation.

The input power is varied to find power gain, maximum power, output $P_{1\mathrm{dB}}$ and PAE. Figure 9 shows the output power at 0 dBm input and 17.15 dBm out at 2.4 GHz, 2 dB loss of cable line is calibrated. Figure 10 shows the measured P_{out}/power gain versus P_{in}, calculated output $P_{1\mathrm{dB}}$ and power added efficiency (PAE). The saturation power is about 24 dBm at 3.3 V power supply, the $P_{1\mathrm{dB}}$ is about 21 dBm at 5 dBm input and

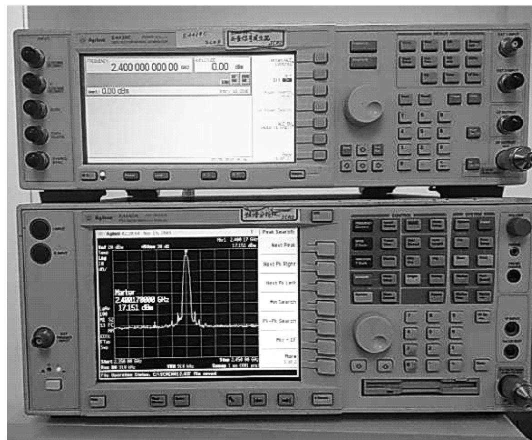


Fig. 9. Power sweep to find power gain, power out and OP_{1dB}.

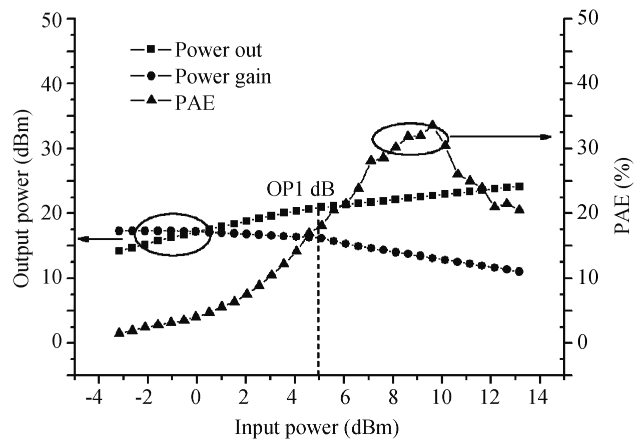


Fig. 10. Measured monolithic PA power sweep results.

Table 3. Performance comparison.

Spec	This work	Ref. [10]	Ref. [9]	Ref. [8]
Output P_{1dB} (dBm)	21	20	16.3	18.5
P_{out} (max) (dBm)	24	25	20	—
Power gain (dB)	18	26	18	30
PAE @ OP_{1dB} (%)	18	19.2	—	19
Process	0.18 μm SiGe BiCMOS	0.35 μm SiGe BiCMOS	0.13 μm RF CMOS	0.18 μm SiGe BiCMOS
Stages	2	2	2	3
Type	Monolithic	On-board matching	On-board matching	Monolithic

the PAE is 18% at this point.

The main performance of the presented monolithic PA is summarized in Table 3. From the performance comparison we find that the presented PA has highest OP1dB, which is critical for system performance. Without any bond wire RFCs and on-board matching, the output power is a little less than Ref. [10], but is better than a CMOS process[9]. Compared to more stage work[8], the PA has more room for improvement in PAE and power gain.

6. Conclusions

This paper has reported the design and performance of a fully integrated power amplifier design in an IBM 0.18 μm SiGe BiCMOS process. Based on the analysis and detailed simulation results, a two-stage amplifier IC for multi-band applications is fabricated and exhibited a P_{1dB} of 21 dBm and a power gain of 18 dB for one-tone excitation. The PA has not required any off chip matching with an 18% PAE at OP_{1dB} and a maximum PAE of 34%.

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