An analytical model for the surface electrical field distribution of LDMOSFETs with shield rings

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Abstract: An analytical model of an LDMOSFET with a shield ring is established according to the 2D Poisson equation. Surface electrical field distribution along the drift region is obtained from this model and the influence of shield length and oxide thickness on the electrical field distribution is studied. The robustness of this model is verified using ISE TCAD simulation tools. The breakdown voltage of a specific device is also calculated and the result is in good agreement with experimental data.

Key words: RF LDMOS; shield ring; RESURF; surface electrical field; drift region

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1. Introduction

With the wide use of high voltage, high power lateral double diffused metal oxide semiconductor transistors (LDMOS)[1], a lot of effort has been spent on numerical analysis of the influence of device structure and process parameters on performance, especially the trade off between on-resistance and breakdown voltage. In Ref. [2] the effect of the length, doping concentration and depth of the drift region has been carefully studied. Some derivative device structures, such as thin epitaxial reduced surface field (RESURF) LDMOS, step doped drift region LDMOS and resistive field plate LDMOS, have been developed and their analytical models presented[3–5].

The shield ring structure is another widely applied RESURF technology in power RF LDMOSFETs. With this structure, the on-resistance of a device can be reduced while the breakdown voltage remains unchanged. In addition, it has the capability of reducing feedback capacitance between gate and drain, which is very important in RF devices[6]. However, to our knowledge, there has been no analytical solution to that problem. In this paper, an analytical model of the surface electrical field distribution (SEFD) in the drift region of an LDMOS with a shield ring is obtained from the 2D Poisson equation. The influence of shield length and oxide thickness on electrical field distribution is discussed. Verification of this model is carried out using ISE TCAD simulation tools and a breakdown voltage test.

2. Analytical model

The cross-section of a simplified RESURF LDMOSFET with a shield ring is shown in Fig 1. As can be seen from Fig. 1, there is a WSi shield between the gate and the drain, which can change the SEFD and reduce feedback capacitance $C_{\rm gd}$ as mentioned above. For simplicity, the drift region is considered to be uniformly doped and the epitaxial layer is assumed to be thick enough to deplete the drift region. S, G, D and shield represent source, gate, drain and shield region, respectively; L is the length of the n-type drift region between the P-body and the drain, and $L_{\rm s}$ is the length of the shield region; $t_{\rm ox}$, t_1, t_2 are the thickness of oxide under the shield region, drift region and depletion region of a p-type epitaxial layer, respectively; $N_{\rm d}$ is the constant doping concentration of the drift region, and $N_{\rm sub}$ is that of the substrate. In an off-state configuration, the substrate, source and gate are grounded, while the drain is biased to $V_{\rm D}$.

Assuming $\phi(x, y)$ is the potential function in the drift region, which satisfies Poisson equation[7]:

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=-\frac{qN_{\rm d}}{\varepsilon_{\rm si}}, \tag{1}$$

where $\varepsilon_{\rm si}$ is the dielectric constant of Si and q is the elementary charge.

Integrating Eq. (1) over the y direction results in[2]:

$$\int_0^{t_1}\frac{\partial^2\phi(x,y)}{\partial x^2}{\rm d}y+E_y(x,0)-E_y(x,t_1)=-\frac{qN_{\rm d}}{\varepsilon_{\rm si}}t_1. \tag{2}$$

Assuming a 1D electrical field in the SiO_2 material and the continuity boundary condition of an electric displacement field perpendicular to the Si/SiO_2 interface:

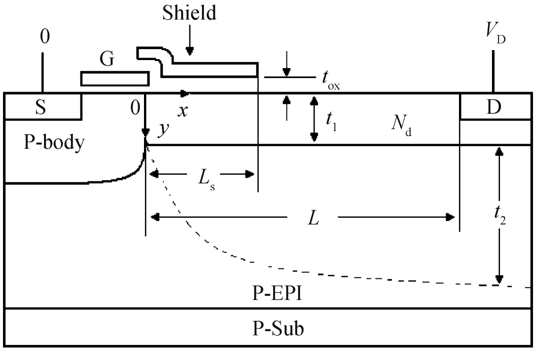

Fig. 1. Cross-section of an LDMOSFET with a shield ring.

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$$E_y(x,0)=\begin{cases}-\dfrac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}}\dfrac{\phi(x,0)}{t_{\rm ox}}, & x\leqslant L_{\rm s},\\ 0, \quad L_{\rm s}<x\leqslant L.\end{cases} \tag{3}$$

For the abrupt junction, it yields[2, 8]:

$$E_y(x,t_1)=\frac{2\phi\,(x,t_1)}{t_2}=\frac{2\,[\phi\,(x,0)-\phi\,(x,t_1)]}{t_1}. \tag{4}$$

Following the assumption given in Ref. [2] and substituting Eqs. (3) and (4) into Eq. (2), a 1D differential equation for the surface potential can be given by[9]:

$$\frac{{\rm d}^2\phi_{\rm f}(x)}{{\rm d}x^2}-\alpha_{\rm f}\phi(x)=\beta_{\rm f}, \tag{5}$$

$$\text{where } \alpha_{\rm f}=\begin{cases}\dfrac{1}{A}\left(\dfrac{\varepsilon_o x}{t_1 t_{\rm ox}\varepsilon_{\rm si}}+\dfrac{2}{t_1(t_1+t_2)}\right)\equiv\alpha_{{\rm f}_1}, \quad x\leqslant L_{\rm s},\\ \dfrac{2}{t_1(t_1+t_2)}\equiv\alpha_{{\rm f}_2}, \quad L_{\rm s}<x\leqslant L,\end{cases}$$

$$\beta_{\rm f}=-B\frac{qN_{\rm a}}{\varepsilon_{\rm si}},$$

$$A=1-\frac{t_1}{2}\frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}t_{\rm ox}},$$

$$B=\begin{cases}\dfrac{1}{A}, & x\leqslant L_{\rm s},\\ 1, \quad L_{\rm s}<x\leqslant L.\end{cases}$$

Solving Eq. (5) with boundary conditions $V(0)=0$ and $V(L)=V_{\rm D}$, defining $\theta_{\rm fi}=-\frac{\beta_{\rm f}}{\alpha_{\rm fi}}$ and $\tau_{\rm fi}\equiv\left(\frac{1}{\alpha_{\rm fi}}\right)^{1/2}$ $(i=1,2)$, it gives:

$$\phi_{\rm f}(x)=\begin{cases}\theta_{\rm f1}+\dfrac{(V_{\rm LS}-\theta_{\rm f1})\sinh\dfrac{x}{\tau_{\rm f1}}-\theta_{\rm f1}\sinh\dfrac{L_{\rm s}-x}{\tau_{\rm f1}}}{\sinh\dfrac{L_{\rm s}}{\tau_{\rm f1}}},\\ \qquad x\leqslant L_{\rm s},\\ \theta_{\rm f2}+\\ \dfrac{(V_{\rm D}-\theta_{\rm f2})\sinh\dfrac{x-L_{\rm s}}{\tau_{\rm f2}}+(V_{\rm LS}-\theta_{\rm f2})\sinh\dfrac{L-x}{\tau_{\rm f2}}}{\sinh\dfrac{L_{\rm s}}{\tau_{\rm f2}}},\\ \qquad L_{\rm s}<x\leqslant L.\end{cases} \tag{6}$$

The SEFD in the drift region can be obtained by differentiating Eq. (6):

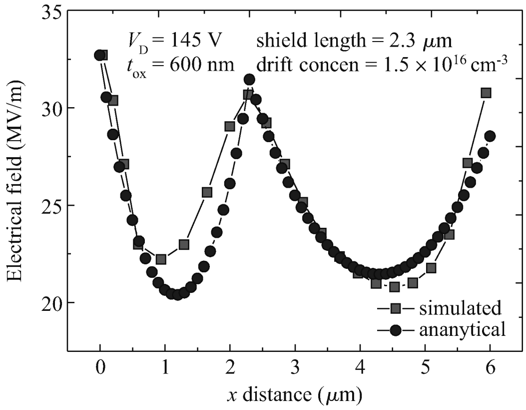

Fig. 2. Comparison between the simulated and analytical surface electrical field.

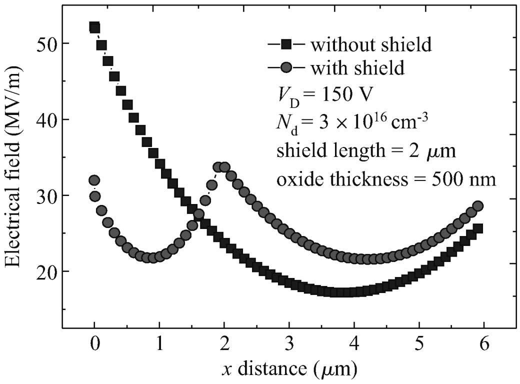

Fig. 3. SEFD of the LDMOSFET with a shield ring.

$$E(x,0)=-\frac{{\rm d}\phi(x,0)}{{\rm d}x}$$
$$=\begin{cases}-\dfrac{(V_{\rm LS}-\theta_{\rm f1})\cosh\dfrac{x}{\tau_{\rm f1}}+\theta_{\rm f1}\cosh\dfrac{L_{\rm s}-x}{\tau_{\rm f1}}}{\tau_{\rm f1}\sinh\dfrac{L_{\rm s}}{\tau_{\rm f1}}},\\ \qquad x\leqslant L_{\rm s},\\ -\dfrac{(V_{\rm D}-\theta_{\rm f2})\cosh\dfrac{x-L_{\rm s}}{\tau_{\rm f2}}-(V_{\rm LS}-\theta_{\rm f2})\cosh\dfrac{L-x}{\tau_{\rm f2}}}{\tau_{\rm f2}\sinh\dfrac{L-L_{\rm s}}{\tau_{\rm f2}}},\\ \qquad L_{\rm s}<x\leqslant L.\end{cases} \tag{7}$$

$V_{\rm LS}$ can be calculated using the surface electrical field continuity at the end of shield ring.

3. Results and discussion

According to the analytical model above, the SEFD along the drift region can be calculated. Figure 2 shows the analytical results of the SEFD of a shielded LDMOSFET obtained from Eq. (7). The squared line is calculated using the ISE TCAD simulator with the LDMOS structure shown in Fig. 1. From

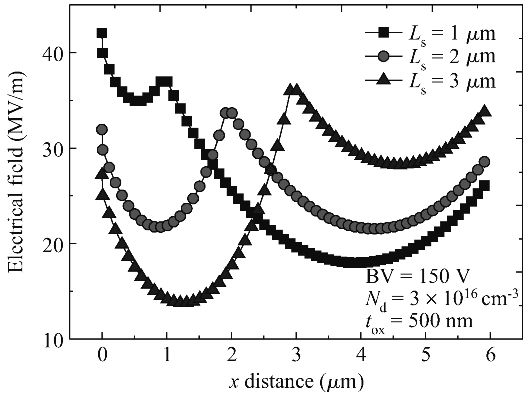

Fig. 4. Influence of shield length on the electrical field distribution.

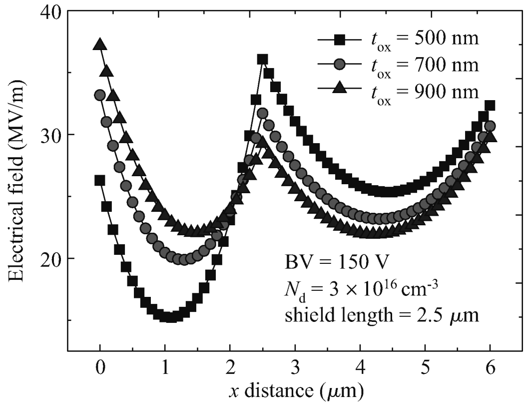

Fig. 5. Influence of shield oxide thickness on the electrical field distribution.

Fig. 2 it can be seen that the electrical field distribution computed from this model is in good agreement with the simulated result.

The effect on the SEFD of LDMOSFET with a shield ring is shown in Fig. 3, where the squared line is shown for contrast. The doping concentration of the drift region is 3×10^{16} cm^{-3} and the drain bias voltage is 150 V. Compared to a LDMOSFET without a shield ring, the SEFD in the drift region with a shield is flattened. The peak electrical field reduces drastically and its position moves from the end of gate to the end of shield. The reason for this is that the presentation of a shield ring causes depletion of the underlying drift region. According to the RESURF principle, the LDMOSFET with a shield ring will get a much higher breakdown voltage at the same condition.

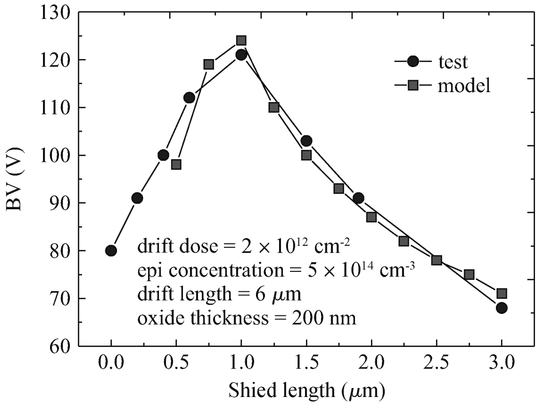

Fig. 6. Experimental and modeled results of breakdown voltage against shield length of the LDMOSFET.

Figures 4 and 5 show the influence of shield length and oxide thickness on the electrical field, respectively. We can see from Fig. 4 that as the length of the shield increases, the electrical field at the end of drain increases while at the end of gate the peak electrical field decreases. This is because as the shield length gets longer the depletion region under it is enlarged, which has the same effect of reducing the doping concentration of the drift region. The oxide thickness under the shield ring has much less effect on the electrical field at the end of drain. It can be seen from Fig. 5 that as the oxide thickens, the electrical field at the end of gate increases while at the end of the shield it decreases. It can be explained that the effect of the shield ring is strongly dependent on oxide thickness. When it is close to the drift region, there will be more space charge depleted, which can drastically reduce the electrical field peak of the PN junction at the gate end. According to the analysis above, it can be seen that as long as the shield length and oxide thickness are selected appropriately, the electrical field at the end of the gate and the drain can be made equal. Therefore, the maximum breakdown voltage can be reached.

With regard to the validation of this analytical model, Figure 6 shows the tested and modeled breakdown voltage against shield length. The LDMOS device tested has a diffused drift region with an implantation dose of 2×10^{12} cm^{-2}. The concentration of the p-type epitaxial layer is 5×10^{14} cm^{-3} and the thickness is 11 μm. The drift region length is 6 μm and the oxide thickness is 200 nm. It is known that breakdown voltage depends on the critical electrical field E_c and breakdown will occur when the peak electrical field exceeds E_c[10]. In this paper we take E_c equal to 3.2×10^5 V/cm. The circled line in Fig. 6 is the breakdown voltage tested using the above device and the squared line is the breakdown voltage calculated through the analytical model. The result is that this model is in good agreement with the experimental data and can provide accurate and fast optimization of the breakdown voltage of a shielded LDMOSFET.

4. Conclusion

In this paper, an analytical model for a shielded LDMOSFET is established and the SEFD along the drift region is calculated. According to the computation, it is evident that the shield ring can decrease the electrical field at the gate end while increasing the electrical field at the end of the drain. The influence of shield length and oxide thickness on the electrical field distribution is also studied. For the verification of this model, the electrical field is simulated using ISE TCAD simulation tools and an experimental test of the breakdown voltage also carried out. The result is that this model is in perfect accordance with both the simulation and the test.

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