Design of a total-dose radiation hardened monolithic CMOS DC–DC boost converter*

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Abstract: This paper presents the design and implementation of a monolithic CMOS DC–DC boost converter that is hardened for total dose radiation. In order to improve its radiation tolerant abilities, circuit-level and device-level RHBD (radiation-hardening by design) techniques were employed. Adaptive slope compensation was used to improve the inherent instability. The H-gate MOS transistors, annular gate MOS transistors and guard rings were applied to reduce the impact of total ionizing dose. A boost converter was fabricated by a standard commercial 0.35 μm CMOS process. The hardened design converter can work properly in a wide range of total dose radiation environments, with increasing total dose radiation. The efficiency is not as strongly affected by the total dose radiation and so does the leakage performance.

Key words: DC–DC power converter; boost converter; radiation-hardening by design; radiation hardened; total dose

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1. Introduction

In space applications, the continuous quest for weight reduction drives the research activities for migration towards the optimization of power converters. For a small size-to-weight ratio and high efficiency, the switching converters are usually chosen for space converter applications. As it provides low-cost, high-performance solutions, CMOS technology has been a popular choice for designs requiring general hardness to the natural space radiation environments. Due to the dramatically increasing processing costs and greater availability of state-of-the-art commercial foundry capacity, providing radiation hardness solely through design techniques rather than a specialized fabrication process has become more and more important[1, 2]. Radiation hardening by design (RHBD) relies solely on circuit design techniques to mitigate the damage, functional upsets, and data loss caused by space radiation.

While there are different types of converters used for power conversion, the boost converter falls in the category of "switch mode DC–DC converters". The boost converter, in general, converts input energy from one level to another level with an output DC voltage higher than the input DC voltage. The effects of total ionizing dose on the boost converter were reported previously[3, 4]. However, only total-dose effects on the discrete and hybrid switching DC–DC boost converter were considered. The total-dose effects in the monolithic DC–DC boost converter, which was fabricated by a deep submicron CMOS process, were not considered. This paper presents RHBD techniques applied to the monolithic DC–DC boost converter that can work properly in a wide range of radiation environments, with increasing total dose radiation.

2. Design issues of the radiation hardened DC–DC boost converter

Considering the issue of radiation, the design of power converters becomes a real challenge. Two basic effects occur when CMOS DC–DC converters are exposed to space radiation: (1) total dose as result of ionization damage and (2) single event effects as a result of an energetic partial strike. In this paper, we concentrate on the design techniques to mitigate total ionizing dose (TID) effects.

2.1. Boost DC–DC converter topology

The circuit of the PWM boost DC–DC converter is shown in Fig. 1, and its output voltage V_{out} is always higher than the input voltage V_{in} for steady-state operation. It 'boosts' the voltage to a higher level. The converter consists of an inductor L, a power MOSFET switch, a diode D, a filter capacitor C, a load resistor R_L, and a pulse width modulation (PWM) circuit. The PWM output voltage switches the power MOSFET between

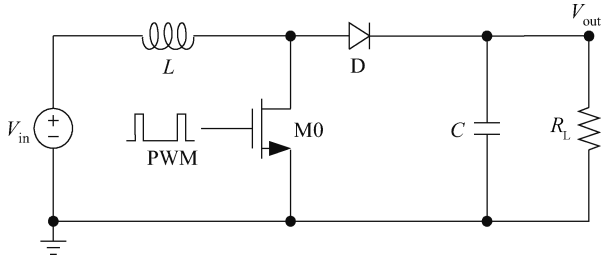

Fig. 1. Structure of a DC–DC boost converter.

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the conducting (on) and nonconducting (off) states. In each period of the PWM output waveform, the PWM output is high for a time (where is the variable duty cycle and is the period).

To first order, the output voltage is described by

$$V_{\text{out}} = \frac{T}{T - T_{\text{on}}} V_{\text{in}}, \tag{1}$$

where T is the repeating period and T_{on} is the switch-on time.

2.2. TID effects in MOS

It has been shown that the dominant radiation effects in MOS devices are due to TID effects, and not due to displacement damage[2]. It is well known that positive charge buildup in the oxide layer and interface state production, due to ionizing radiation effects, lead to threshold voltage shifts and channel mobility degradation. The amount of threshold shift in MOS devices caused by ionizing radiation is strongly dependant on the bias voltage applied to the gate, both during and after radiation. Conceptually, the radiation induced oxide charge buildup problems are a simple principle. It is only when one tries to quantify the details of the radiation response that one realizes the complexities involved in the radiation response of the MOS transistor[1, 2]. In any TID conditions, the R_{on} of MOS increases and the G_{m} of MOS decreases. As transistors degrade, the loss of device quality shows up in higher-level performance shifts.

The continued scaling of CMOS technologies has led to significant increases in the electric field in the MOSFET channel and oxides with each succeeding generation. Increased electric fields in the channel and in the oxides can lead to hot-carriers. When these carriers lose energy through impact ionization or elastic scattering events, this can lead to photon generation, substrate current, or electron/hole injection into the oxide. In a recent paper by Mayer *et al.*[5], the hot-carrier reliability of an annular transistor was shown to be better than the reliability of a standard two-edge fabricated by the same 0.25 μm technology.

2.3. The boost converter failure induced by TID

Although the effects of total-dose ionizing radiation on hybrid power converters have been studied in detail, less information is available about the effects of total-dose ionizing radiation on a monolithic DC–DC boost converter. The power converters may be very sensitive to radiation (total-dose, single event effects) and their radiation response is dependent on temperature, input bias conditions and load conditions. Reference [4] shows that the hybrid converter failures that were observed were caused by irradiation of the error amplifier, but the SG1525A PWM integrated circuit exhibited excellent total-dose tolerance, with proper circuit operation maintained up to a 1 Mrad(SiO_2) total dose. These results provide an interesting insight into the role of feedback mechanisms in the total-dose degradation of the converter. The feedback loop maintained the error amplifier bias operating point as long as the converter operated, but once the error amplifier had degraded sufficiently, the converter stopped working when the power was cycled off and on.

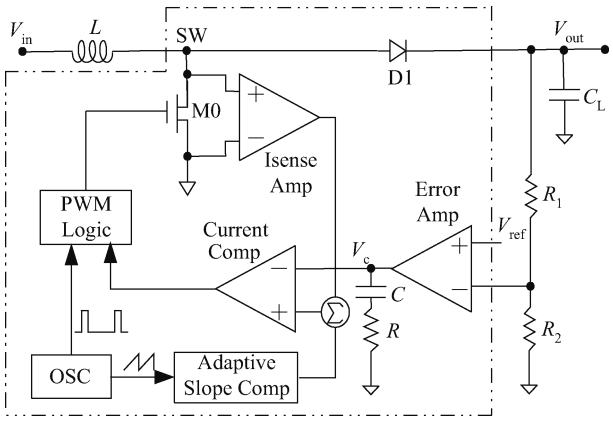

Fig. 2. Diagram of the RH DC–DC boost converter.

In fact, the boost converter is a mixed-signal system that is made of analog circuits and digital circuits. So its failure induced by total dose may be thought of as the failures of analog circuits and digital circuits. Amplifiers are sensitive to changes in gain, bandwidth, and noise, so that effects on transconductance and noise parameters are important. Comparators used for threshold determination and timing rely critically on threshold shifts. Digital circuitry is affected by threshold shifts that affect propagation delays and device transconductance, which determines switching speed.

3. Design of the radiation hardened DC–DC boost converter

The goal of radiation-hardening design is not so much to obtain a system whose characteristics do not change under irradiation as to maintain the required performance characteristics over the lifetime of the system. The RHBD techniques should maintain the speed, area penalty, power penalty and other performance characteristics compatible with radiation hardened devices by processing technology. Hardening must be considered in device, circuit, and architecture design. Changes at any one of these levels that influence circuit hardness may also influence other aspects of circuit performance. Tradeoffs between hardness, performance, reliability, manufacturability and cost further limit the range of techniques appropriate to a particular design.

3.1. General design specifications

A diagram of the radiation hardened monolithic current mode DC–DC boost converter with integrated power switches and adaptive slope compensation is shown in Fig. 2. In the DC–DC converter, M0 is the main switch and M1 is the synchronous switch; the modulator is formed by PWM logic. The specifications for this design are: input voltage from 1.2 to 5.5 V with loading current below 2 A and 2.6 to 5.5 V adjustable output voltage, the output ripple voltage is about 20 mV with a off-chip capacitor and off-chip inductor, and the power efficiency of PWM is over 80% for load current from 100 to 800 mA[6].

The radiation hardened boost converter must be designed for optimum performance and reliability in both non radiation

and radiation environments encountered during the mission. Parameters such as efficiency, output voltage, step response, loop gain frequency response and phase margin may be affected by radiation, depending on the converter topology. By considering the DC–DC converters as a unified power delivery system, a hierarchical design strategy may be employed. The ultra thin gate oxide of deep submicron technologies is inherently more tolerant to total dose effects than the thicker oxides encountered in less advanced technologies. So the radiation hardened boost converter has been fabricated by a standard commercial 0.35 μm CMOS process.

3.1.1. Loop stability

A series capacitor–resistor combination sets a pole-zero combination to govern the characteristics of the control system. The DC gain of the voltage feedback loop A_{LOOP} is given by

$$A_{\mathrm{LOOP}} = \frac{V_{\mathrm{FB}}}{V_{\mathrm{OUT}}} A_{\mathrm{EA}} G_{\mathrm{M}} R_{\mathrm{LOAD}}, \tag{2}$$

where V_{FB} is the feedback voltage, A_{EA} is the error amplifier voltage gain and G_{M} is the current sense transconductance. The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Low crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good standard is to set the crossover frequency below one-tenth of the switching frequency.

3.1.2. Adaptive slope compensation

It is a well-known problem that subharmonic oscillation appears when the current-mode switching converters' duty ratio D is larger than 0.5. Subharmonic oscillation is normally characterized by observing an alternating wide and narrow pulse at the switch node. Adding an extra ramp (slop compensation) to the current-sense signal prevents this oscillation. The linear slope compensation will result in more slope surplus, especially in low duty cycle, and affect the peak current limit of the DC–DC converter. Then the piecewise linear slope compensation is widely used in a certain application field. But because of serious jitter in the turning of the piecewise linear slope compensation, this method is difficult to operate at a continuous duty cycle range. In order to improve the above considerations, the adaptive slope compensation has been designed for boost converter. Based on the analysis of the current loop, by detecting the input and output voltage, converting the adaptive slope compensation current, the compensation of the current loop is optimized[7]. The adaptive slope compensation can not only improve the compensation accuracy but also eliminate the over compensation, the turning jitter and the poor loading capability.

3.2. Circuit level RHBD techniques

The major challenge in designing radiation-hardened integrated circuits is optimizing the actual circuit design for reliable performance in an ionizing-radiation environment. The design principles should reflect an understanding of the detailed response of the characterized technology to the types and levels of radiation anticipated for the operating device.

3.2.1. Analogue circuits

The analogue circuits of a monolithic DC–DC boost converter may include amplifiers (i.e. error amplifier), comparators and oscillators, etc. In practice, the circuit level RHBD techniques of analogue circuits trade with each other, making the design a multi-dimensional optimization problem.

Damage from radiation results in changes in devices' operating mechanisms and the circuit DC operating point. In general, the use of fully differential circuitry and current mirrors yields circuitry whose operating point relies primarily on relative device matching. Changes in threshold voltages or current gain in adjacent devices tend to track after radiation damage, so the circuit will maintain its operating point. Circuitry should also be designed to minimize single-point failure modes. Failure of common bias networks will cause all associated circuitry to fail. Local biasing with highly parallel architectures could reduce these problems.

(1) Current mirrors

Current mirrors can perform useful functions on analog signals, which may be as both bias elements and signal processing components. The speed is not a problem for these circuits, which are designed to provide a static current bias. Current mirrors are necessarily operated in saturated mode. If the total dose effects move the DC bias outside the saturated mode, the current mirror loses its precision. In order to increase the precision of current mirrors, we may use large transistors and increase V_{dd} to maintain the transistor in the saturated mode.

(2) Error amplifier

In the boost converter, the error amplifier is a transconductance amplifier. The parameters of transconductance g_{m} and the output resistance R_{O} are important for frequency compensation, as they determine the gain and phase margin of the current-mode boost DC–DC converter. As long as the converter operated, the error amplifier bias operating point is maintained by the feedback loop. But once the error amplifier had degraded sufficiently, the converter stopped working when the power was cycled off and on. It is important that the amplifier design is robust against the variation in the electrical parameters within specified limits. For example, we may rise I_{bias} overcome the DC point shift of amplifier and foresee a comfortable initial phase margin (PM > 80°) increasing the stability of amplifier. The use of current mirrors reduces further radiation induced drift caused by changes in the threshold voltage. This mitigation by mirrored drift is limited by the statistical matching of the mirror devices and by the limited difference in drain voltage of the devices. Note that the input differential pair was implemented with PMOS transistors as is the current source transistor. The threshold voltage of this PMOS transistor can only decrease in response to radiation. This observation allows optimization of the feedback mechanism, which aims to keep the value of this current constant.

(3) Comparator

The comparator is an important component in the feedback control loop modulator for the PWM control and the hysteretic comparator in the oscillator and ramp generator circuit. A crit-

ical design aspect for comparators is a good trade-off between sensitivity, speed, and power consumption. The precision depends on the input offset, which is controlled by V_t and by g_m. The speed depends on the g_m of the transistors, controlled by dose. We may increase g_m by increasing I_{dc}, which is detrimental to the power consumption. Power dissipation is a critical issue when designing DC–DC switching power converters. The comparator in the oscillator is a standard two-stage comparator with hysteresis. Hysteresis was used to avoid oscillation when the comparator switches from a high state to a low state. The comparator in the feedback control loop is implemented by a source-coupled differential pair with positive feedback to provide a high gain.

3.2.2. Digital circuits

As the threshold shifts of NMOS and PMOS are not complementary, circuit switching thresholds may change with radiation. At high damage levels, the device transconductance also suffers due to buildup of interface charge and increased scattering of charge carriers in the channel. Both effects change propagation delays, which can lead to race conditions (mismatches in propagation delays of streams whose results are combined) that cause circuit failure. One way to accommodate threshold voltage shifts after irradiation is to change the relative area of the p- and n-channel devices. Normally, a CMOS inverter will be scaled with a 2 : 1 ratio between p- and n-channel devices. This scaling compensates for the difference in hole and electron mobility in silicon and thereby provides comparable drive under normal conditions. Changing this ratio can increase the tolerance of a circuit to post-radiation changes in threshold voltage.

The logic gates are basic building blocks for digital circuit design. The method of implementing logic gates can affect total dose hardness. Since negative threshold voltage shifts due to radiation reduce postradiation PMOS drive current, NAND gates should be used instead of NOR gates, in which PMOS transistors are connected in series. There is high noise immunity, high packing density and high speed superiority of NAND gates to NOR gates in radiation hardened digital integrated circuits. If NOR gates must be used in designed circuits, then the number of inputs (fan-in) should be minimized.

Both the maximum frequency decrease due to threshold voltage shift and the minimum frequency increase due to radiation induced leakage determine the useful radiation level in dynamic circuits. Since the worst radiation bias for clocked gate CMOS circuits is half of that for transfer gate CMOS circuits, the maximum threshold voltage shift in clocked gate circuits is smaller than that in transfer gate circuits. Therefore, actual degradation in clocked gate CMOS circuits can be considered to be smaller than that in transfer gate CMOS circuits for the same total dose.

3.3. Device-level RHBD techniques

The effects of radiation have not only been counteracted on the circuit level but have also been handled on the layout level. Special layout considerations are needed for boost converter hardening. Such concerns extend from the basic device and layout as far as the details of chip architecture for various macro cells.

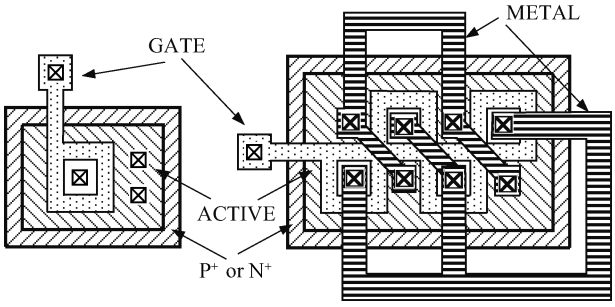

Fig. 3. Structure of annular MOSFET.

Previous studies have shown that the dominant leakage path in modern bulk CMOS technologies is indeed the parasitic edge leakage path. For a conventional NMOS transistor, a parasitic channel could be formed beneath the field oxide between the source and drain. As MOS channel edge leakage can add current error to sensitive nodes, it is necessary to restrict device geometries to closed ("edgeless") transistors, or implement explicit channel stop layout features. The H-gate transistors can prevent the kink or bipolar effect since the body contacts are present at both ends of the channels. There is no direct edge leakage path that between the source and the drain (the edges run only from N^+ to P^+ diffusions) of the H-gate structure[6, 8, 9]. The annular MOSFET can improve the hot-carrier reliability of CMOS circuits by reducing the drain electric field compared to conventional MOSFETs, which has demonstrated total-dose radiation immunity in CMOS circuits[5]. In an annular layout, the only path from source to drain is underneath the gate. As shown in Fig. 3, the specific square layout allows the easy formation of a closed matrix of cells to form a larger transistor. One of the problems in using RHBD techniques to improve the radiation tolerance of I_{CS} is that there is a significant area penalty associated with H-gate and annular gate resistors. We design the power MOSFETs as switching devices with a square annular MOSFET and a control block with an H-gate MOSFET.

The multi-finger layout increases the leakage current and the threshold voltage shift due to radiation in NMOS transistors. No significant variations have been observed between the PMOS transistors with different layouts. So we use a single stripe device instead of multi-fingered devices as far as possible in the layout.

During the switching period, large voltage spikes are generated on the power buses by parasitic inductance of the bonding wires. If these spikes are not well suppressed, the voltage stress on power switches might be high enough to break the power switches. There is not too much margin for the devices because most MOSFETs in the standard CMOS processes have only 5 to 10 V breakdown voltage. Moreover, the voltage spikes can be transferred into control core through substrate or interconnection coupling and deteriorate the function of the sensitive circuits. A proper floor plan and shielding should minimize this effect in the layout. The devices are shielded from each other by grounded guard rings, which help to prevent leakage currents and latch up between separate devices.

A micrograph of the radiation hardened monolithic DC–DC boost converter is shown in Fig. 4.

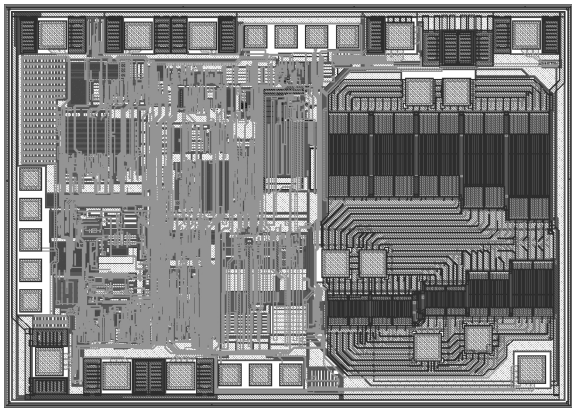

Fig. 4. Micrograph of the RH DC–DC boost converter.

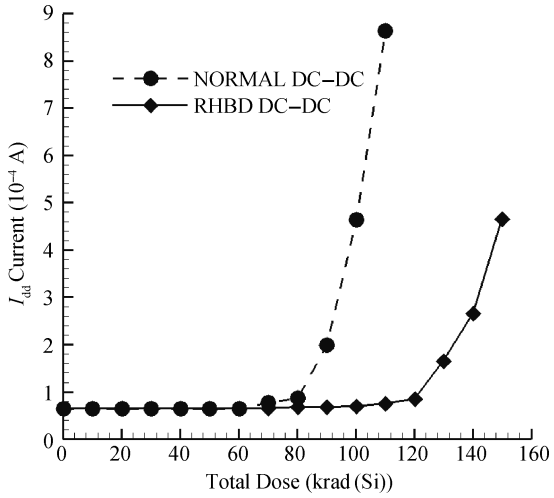

Fig. 5. Converter static leakage current degradation versus total dose.

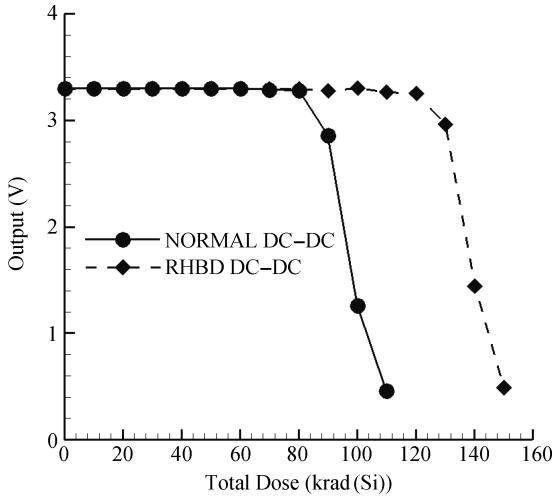

Fig. 6. Converter output voltage degradation versus total dose.

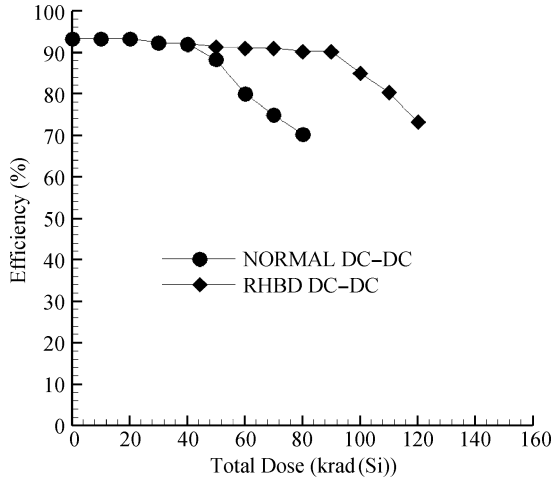

Fig. 7. Converter efficiency degradation versus total dose.

4. Experimental results

It is particularly difficult to relate accelerated laboratory tests to the total dose effects that will be encountered in space. Although basic total dose testing can be done relatively inexpensively, characterizing a process for space applications requires a much more thorough evaluation of total dose effects. This includes annealing devices after irradiation at elevated temperatures (with bias applied) to accelerate the annealing of holes, and, therefore, to simulate low dose rate effects in space. Radiation testing was performed using a Co-60 gamma ray source at a dose rate of 50 rad(Si)/s. The Co-60 source has a dose rate that falls within the standard range specified by US MIL-STD 883D, Test Method 1019.4 (50–300 rad(Si)/s). Two designs are presented to evaluate radiation tolerance in the radiation hardened and the normal monolithic DC–DC boost converters, which have been fabricated by a standard commercial 0.35 μm CMOS process. All devices were irradiated and tested at room temperature. Devices were tested under typical application conditions: in the external inductor 2.2 μH, capacitor 44 μF, input 1.2 V, output 3.3 V.

Figure 5 illustrates the measured static leakage current degradation versus total dose for the radiation hardened and the normal monolithic DC–DC boost converters. The leakage current increases with increasing TID. The results, as expected, showed that the radiation-induced static leakage current of the RHBD boost converter is much less than that of the normal boost converter.

Satellite and space probes typically encounter total dose levels between 10 and 100 krad(Si), although systems exist with requirements above and below this range. As shown in Fig. 6, the experimental results show that the normal monolithic DC–DC boost converter survived an 80 krad(Si) total ionizing dose with no degradation in function, and the radiation hardened monolithic DC–DC boost converter survived a 120 krad(Si) total ionizing dose with no degradation in function.

Figure 7 compares the efficiency degradation of the hardened and normal boost converter with load resistance of 10 Ω. By contrast, the efficiency of the hardened boost converter is not as strongly affected by total dose.

5. Summary

The design and implementation of a total dose radiation hardened monolithic CMOS DC–DC boost converter is addressed in this paper. Both circuit-level and device-level

RHBD techniques are employed to improve the radiation tolerant abilities. The radiation experiment results show that the circuit survived a 120 krad(Si) total ionizing dose with no degradation in function, the radiation-induced static leakage current of the hardened boost converter is much less than that of the normal boost converter, and the efficiency of the hardened boost converter is not as strongly affected by total dose. The RHBD techniques are effective in producing a TID-robust CMOS DC–DC boost converter for space applications.

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