A dual-mode 6–9 GHz transmitter for OFDM-UWB*

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Abstract: This paper presents a fully integrated dual-mode 6 to 9 GHz transmitter for both WiMedia and China MB-OFDM UWB applications. The proposed transmitter consists of a dual-mode I/Q LPF, an up-conversion mixer, a two-stage power driver amplifier and a broadband high-speed frequency divider with LO buffers for I/Q LO carrier generation. The measurement results show that the gain ripple of the transmitter is within $\pm 1.5/\pm 2.8$ dB from 6 to 8.7/9 GHz. The output IP3 is about +13.2 dBm, the output 1dBCP is around +2.8 dBm, and the LO leakage/sideband rejection ratio is about –35/–38 dBc. The ESD protected chip is fabricated with a TSMC 0.13 μm RFCMOS process with a die size of 1.6×1.3 mm^2 and the core circuit consumes only 46 mA under a 1.2 V supply.

Key words: dual-mode; MB-OFDM; UWB; transmitter; CMOS
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1. Introduction

As one of the choices for high-speed wireless connections in the short range, OFDM-UWB technology has ignited the interests of industry as well as academia. Recently, different UWB regulations have been proposed[1]. In Europe, the frequency range with a maximum mean equivalent isotropic radiated power (EIRP) density of –41.3 dBm/MHz is from 6 to 8.5 GHz, i.e. the WiMedia bandgroup #3. In Korea and Japan, 7–9 GHz is released unrestrictedly. Meanwhile in China, the UWB standard proposal allows transmission from 6 to 9 GHz with a maximum mean EIRP density of –41.3 dBm/MHz. Therefore developing UWB systems that operate in 6–9 GHz is of the most interest. Although many transmitters under the WiMedia-standard have been reported[2−5], to design the UWB transmitters as required by China's standard while also being compatible with the WiMedia standard is a challenging task.

In this paper, a dual-mode 6 to 9 GHz OFDM-UWB transmitter is presented to offer a solution to the above problem. Since the bandwidth of the analog baseband (ABB) in China's UWB standard proposal is half of that in the WiMedia standard, the cut-off frequency f_c of the LPF needs to switch between 132 and 264 MHz. To fulfill this requirement, a dual-mode I/Q LPF with mode-switch circuits is proposed. The architecture of the proposed transmitter is described with the detailed circuit designs in the subsections.

2. Architecture and circuit design

The proposed transmitter utilizes the direct conversion architecture because of its ease of integration and low cost. As shown in Fig. 1, it consists of a dual-mode I/Q LPF with mode-switch circuits, an I/Q up-conversion mixer with high-linear voltage-to-current (V2I) units, a two-stage power driver amplifier (PA) and a broadband high-speed frequency divider with LO buffers for generating I/Q LO signals. In addition, the trans-impedance amplifiers (TIAs) are integrated to measure the AC transfer character of the LPF.

The main signal flow of this transmitter is as follows. The ABB voltage signals from the DACs are applied at the inputs of the I/Q LPF. With the correct mode-switch bit as well as the digital control capacitor array (DCCA) control word, the image signals of the DACs and the unwanted high frequency spurs are all filtered out in both 264- and 132-MHz modes. After the output voltages of the LPF are converted into ABB currents by V2I units, they are up-converted into RF voltages by the switches in the up-conversion mixer at the rate of LO. Lastly, the differential RF voltages are amplified by a PA and are converted into a single-ended one via the 6–9 GHz off-chip balun, i.e. balun-2, to drive the antenna.

In addition, with the help of the 10–20 GHz off-chip microwave balun, i.e. balun-1, the differential $2f_{Lo}$ signals are fed into the high-speed frequency divider and the desired I/Q LO signals are ready at its outputs. The design challenges as well as the detailed circuit designs of the dual-mode I/Q LPF with mode-switch circuits, the I/Q up-conversion mixer with V2I units and the PA are described in the following subsections.

2.1. Dual-mode I/Q LPF

The main requirements of this LPF are the attenuation of the out-band signals, the in-band ripple, the dual-mode operation with accurate cut-off frequency control and accommodation to the large input ABB voltages. According to the sampling rate of a common UWB DAC, the LPF should have an attenuation of about 45 dB from 264/132 MHz to 600/300 MHz at 264/132-MHz mode. Moreover, an in-band ripple of 0.5 dB

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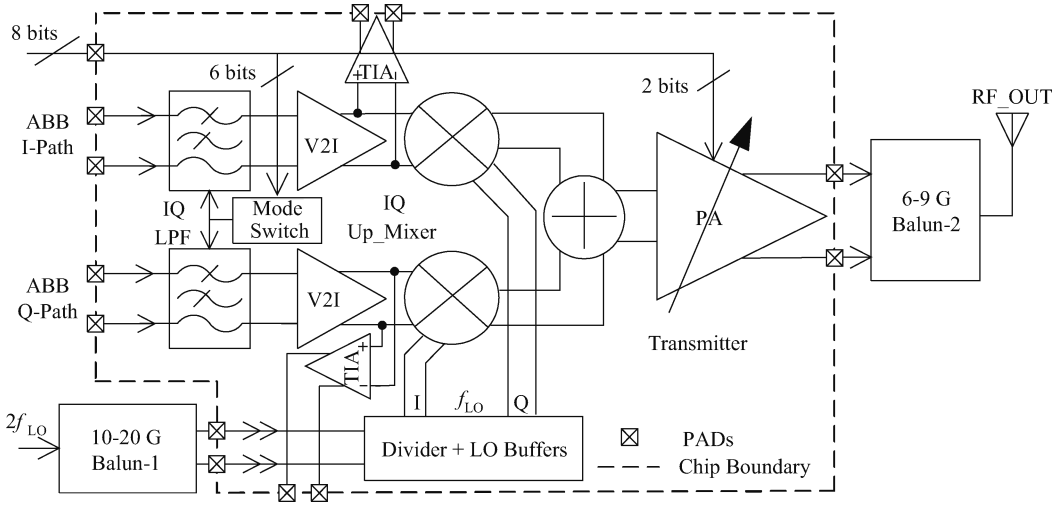


Fig. 1. Block diagram of the proposed transmitter.

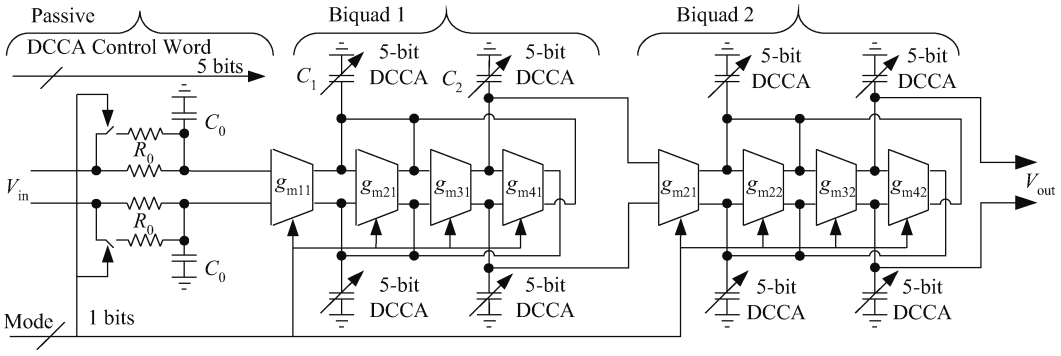


Fig. 2. Architecture of the 5th-order Chebyshev LPF with mode-switch circuits.

Table 1. Parameters of the dual-mode LPF.

Parameter	Mode	Passive	Biquad 1	Biquad 2
f_p (MHz)	264-M	94.8	–77.1±j163	–29.7±j268
	132-M	47.4	–38.6±j81	–14.8±j134
Q	264-M	0.5	1.172	4.545
	132-M	0.5	1.172	4.545
ω_0 (MHz)	264-M	94.8	182.95	270.34
	132-M	47.4	91.47	135.17

is required. To obtain comparably good phase linearity, the Chebyshev approximation is adopted. As calculation with Matlab, a 5th-order Chebyshev LPF meets the specifications of the 45-dB attenuation at $2f_c$ with less than 0.5-dB in-band ripple. The detailed calculated parameters of the LPF for 264/132-MHz mode are summarized in Table 1. The proposed 5th-order Chebyshev g_m–c LPF is as shown in Fig. 2. The real pole is realized at the passive RC sub-filter and the complex poles are realized by biquads. The transfer function of the biquad is described in Eq. (1)[6],

$$H_i(s) = \frac{A_{\mathrm{DC}i}\omega_{0i}^2}{s^2 + s\dfrac{\omega_{0i}}{Q_i} + \omega_{0i}^2}, \tag{1}$$

where i denotes the sequence number of the biquad, $A_{\mathrm{DC}i}$, ω_{0i} and Q_i are the DC gain, cut-off frequency and quality factor of the ith biquad, respectively. To simplify the design of the LPF core as well as the mode-switch circuits, let $g_{\mathrm{m}3i} = g_{\mathrm{m}4i} = g_{\mathrm{m}i}$ and $C_1 = C_2 = C$. Under these conditions, $A_{\mathrm{DC}i}$, ω_{0i}, Q_i can be simplified as Eqs. (2) to (4). As in Eq. (2), the DC gain equals the ratio of $g_{\mathrm{m}1}$ over $g_{\mathrm{m}4}$ of each biquad.

Because of the relatively large input ABB signal, $A_{\mathrm{DC}i} =$ 0 dB, i.e. $g_{\mathrm{m}1i} = g_{\mathrm{m}4i}$. As in Eq. (3), by properly adjusting $g_{\mathrm{m}i}$ and C, the desired value of ω_{0i} is obtained. Finally, the required Q_i is determined by the ratio of $g_{\mathrm{m}i}$ over $g_{\mathrm{m}2i}$ as in Eq. (4). Thus all of the circuit parameters for each mode are available.

$$A_{\mathrm{DC}i} = \frac{g_{\mathrm{m}1i}}{g_{\mathrm{m}4i}}, \tag{2}$$

$$\omega_{0i} = \sqrt{\frac{g_{\mathrm{m}3i}\,g_{\mathrm{m}4i}}{C_1C_2}} = \frac{g_{\mathrm{m}i}}{C}, \tag{3}$$

$$Q_i = \frac{\sqrt{g_{\mathrm{m}3i}\,g_{\mathrm{m}4i}}}{g_{\mathrm{m}2i}}\sqrt{\frac{C_1}{C_2}} = \frac{g_{\mathrm{m}i}}{g_{\mathrm{m}2i}}. \tag{4}$$

The mode-switch circuits are required to enable the LPF to operate in dual modes. As illustrated in Fig. 2, the mode-switch circuits are composed of the 5-bit DCCAs, the 1-bit digital control trans-conductors and the resistors. The scheme of switching between the 264- and 132-MHz modes is as follows. Originally, Mode = '0' and the LPF operates at the 264-MHz mode. All of the circuit parameters for 264-MHz mode are as in Table 1. When Mode = '1', the LPF turns to the 132-MHz

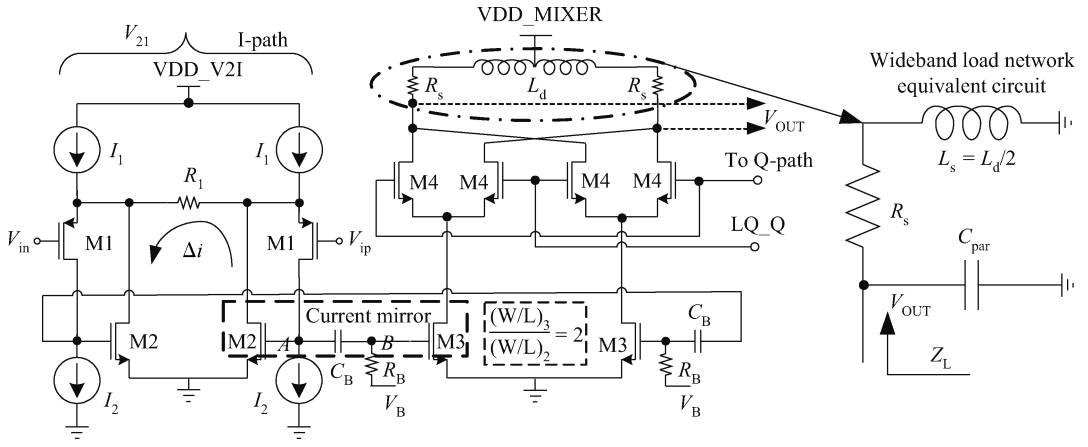


Fig. 3. Simplified I-path schematic of the up-mixer and its wideband load network.

mode. As shown in Fig. 2, the switches are off, the resistance $R = R_0$ while C_0 is unchanged, thus f_p of the passive sub-filter is halved, as required in Table 1. At the same time, g_{mi} and g_{m2i} are halved too, according to Eq. (3). ω_{0i} is also halved while Q_i is unchanged, as in Eq. (4). After the above transformations, all of the circuit parameters of the LPF are switched from 264-MHz to132-MHz mode. When the Mode switches from '1' to '0', the opposite happens.

Moreover, owing to the variations in the fabrication process and mismatches between the trans-conductors, the accuracy of ω_{0i} is limited, therefore the capacitance C in Eq. (3) is replaced by a 5-bit DCCA. By properly setting the control word of the DCCA according to the desired value of C, the required cut-off frequency of the LPF could be reached. In this way, the dual-mode LPF with precise cut-off frequency control is realized.

In addition, to deal with ABB voltages as large as 300 mVpp, the passive sub-filter is placed as the 1st stage and the high-Q biquad as the last stage. Also, to improve the linearity of the LPF under a low supply voltage with low power, the trans-conductors are built with Nauta's structure[7].

2.2. Up-conversion mixer

The simplified I-path schematic of the up-mixer is shown in Fig. 3. It utilizes two double balanced Gilbert cells with their outputs summed to realize single-sideband (SSB) up-mixing. Since the I/Q up-mixer acts as an I/Q modulator and up-conversion mixer in a direct conversion transmitter, the performances of the transmitter are mainly determined by this circuit.

Low spurs, high linearity and wide bandwidth are the main challenges for the design of this up-conversion mixer. The main spurs in the output spectrum of the transmitter are the LO leakage and the sideband signal. In order to analyze the relationship between the spurs and the errors, a SSB up-mixer model is developed, as shown in Fig. 4. In this model, $G_{i/q}$ denotes the gain of the I/Q ABB path, $A_{i/q}$ is the gain of the I/Q LO path, I/Q_{os} is the offset of the I/Q ABB path and θ is the phase error of the I/Q LO path. Because the frequency of the ABB signal is relatively low, the phase error of the I/Q ABB path is of less importance. Thus it is not included. And the offset of the I/Q LO path is excluded because it is eliminated by the AC coupling capacitors.

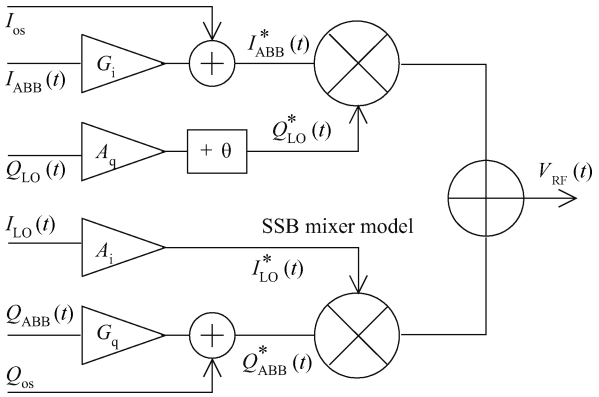


Fig. 4. SSB up-mixer model.

Assuming the input I/Q ABB and I/Q LO signals are described as Eq. (5), mathematically, the output of the up-mixer is as Eq. (6).

$$\begin{cases} I_{\mathrm{ABB}}(t) = \cos(\omega_{\mathrm{ABB}}t) \\ Q_{\mathrm{ABB}}(t) = \cos(\omega_{\mathrm{ABB}}t + 90°) = -\sin(\omega_{\mathrm{ABB}}t) \\ I_{\mathrm{LO}}(t) = \cos(\omega_{\mathrm{LO}}t) \\ Q_{\mathrm{LO}}(t) = \cos(\omega_{\mathrm{LO}}t + 90°) = -\sin(\omega_{\mathrm{LO}}t), \end{cases} \tag{5}$$

$$\begin{aligned} V_{\mathrm{RF}}(t) &= I^*_{\mathrm{ABB}}(t) \times Q^*_{\mathrm{LO}}(t) + Q^*_{\mathrm{ABB}}(t) \times I^*_{\mathrm{LO}}(t) \\ &= [G_{\mathrm{i}}\cos(\omega_{\mathrm{ABB}}t) + I_{\mathrm{os}}] \times [-A_{\mathrm{q}}\sin(\omega_{\mathrm{LO}}t + \theta)] \\ &\quad + [-G_{\mathrm{q}}\sin(\omega_{\mathrm{ABB}}t) + Q_{\mathrm{os}}] \times A_{\mathrm{i}}\cos(\omega_{\mathrm{LO}}t). \end{aligned} \tag{6}$$

After simplification and re-arrangement of Eq. (6), we find that the amplitude of the desired up-converted RF signal V_{SIG}, the sideband signal V_{SB} as well as the LO leakage V_{LOL} are depicted as in Eqs. (7)–(9), respectively.

$$\begin{aligned} V_{\mathrm{SIG}} &= \frac{1}{2}G_{\mathrm{i}}A_{\mathrm{q}}\sin\theta\cos(\omega_{\mathrm{LO}} + \omega_{\mathrm{ABB}}) \\ &\quad + \frac{1}{2}(G_{\mathrm{q}}A_{\mathrm{i}} + G_{\mathrm{i}}A_{\mathrm{q}}\cos\theta)\sin(\omega_{\mathrm{LO}} + \omega_{\mathrm{ABB}})t. \end{aligned} \tag{7}$$

$$V_{\mathrm{SB}} = \frac{1}{2}G_{\mathrm{i}}A_{\mathrm{q}}\sin\theta\cos(\omega_{\mathrm{LO}}-\omega_{\mathrm{ABB}})t + \frac{1}{2}(G_{\mathrm{i}}A_{\mathrm{q}}\cos\theta - G_{\mathrm{q}}A_{\mathrm{i}})\sin(\omega_{\mathrm{LO}}-\omega_{\mathrm{ABB}})t. \quad (8)$$

$$V_{\mathrm{LOL}} = (A_{\mathrm{q}}I_{\mathrm{os}}\sin\theta + A_{\mathrm{i}}Q_{\mathrm{os}})\cos\omega_{\mathrm{LO}}t + A_{\mathrm{q}}I_{\mathrm{os}}\cos\theta\sin\omega_{\mathrm{LO}}t. \quad (9)$$

Defining the sideband rejection ratio (SBRR) as the power ratio of the sideband and that of the RF signal, it is depicted in Eq. (10).

$$\begin{aligned}\mathrm{SBRR} &= 20\lg\left|\frac{V_{\mathrm{SB}}}{V_{\mathrm{SIG}}}\right| \\ &= 20\lg\sqrt{\frac{(G_{\mathrm{i}}A_{\mathrm{q}})^2 - 2G_{\mathrm{i}}A_{\mathrm{q}}G_{\mathrm{q}}A_{\mathrm{i}}\cos\theta + (G_{\mathrm{q}}A_{\mathrm{i}})^2}{(G_{\mathrm{i}}A_{\mathrm{q}})^2 + 2G_{\mathrm{i}}A_{\mathrm{q}}G_{\mathrm{q}}A_{\mathrm{i}}\cos\theta + (G_{\mathrm{q}}A_{\mathrm{i}})^2}} \\ &= 10\lg\frac{\left(\dfrac{G_{\mathrm{i}}A_{\mathrm{q}}}{G_{\mathrm{q}}A_{\mathrm{i}}}\right)^2 - 2\dfrac{G_{\mathrm{i}}A_{\mathrm{q}}}{G_{\mathrm{q}}A_{\mathrm{i}}}\cos\theta + 1}{\left(\dfrac{G_{\mathrm{i}}A_{\mathrm{q}}}{G_{\mathrm{q}}A_{\mathrm{i}}}\right)^2 + 2\dfrac{G_{\mathrm{i}}A_{\mathrm{q}}}{G_{\mathrm{q}}A_{\mathrm{i}}}\cos\theta + 1}.\end{aligned} \quad (10)$$

Similarly, the LO leakage rejection ratio (LOLRR) is defined in Eq. (11).

$$\begin{aligned}\mathrm{LOLRR} &= 20\lg\left|\frac{V_{\mathrm{LOL}}}{V_{\mathrm{SIG}}}\right| \\ &= 20\lg\sqrt{\frac{(A_{\mathrm{q}}I_{\mathrm{os}})^2 - 2A_{\mathrm{q}}A_{\mathrm{i}}I_{\mathrm{os}}Q_{\mathrm{os}}\sin\theta + (A_{\mathrm{i}}Q_{\mathrm{os}})^2}{(G_{\mathrm{i}}A_{\mathrm{q}})^2 + 2G_{\mathrm{i}}A_{\mathrm{q}}G_{\mathrm{q}}A_{\mathrm{i}}\cos\theta + (G_{\mathrm{q}}A_{\mathrm{i}})^2}} \\ &= 10\lg\frac{(A_{\mathrm{q}}I_{\mathrm{os}})^2 - 2A_{\mathrm{q}}A_{\mathrm{i}}I_{\mathrm{os}}Q_{\mathrm{os}}\sin\theta + (A_{\mathrm{i}}Q_{\mathrm{os}})^2}{(G_{\mathrm{i}}A_{\mathrm{q}})^2 + 2G_{\mathrm{i}}A_{\mathrm{q}}G_{\mathrm{q}}A_{\mathrm{i}}\cos\theta + (G_{q}A_{i})^2}.\end{aligned} \quad (11)$$

As shown in Eqs. (10) and (11), ideally there are no gain/phase errors of the I/Q path and it is free of offsets, i.e. $G_{\mathrm{i}} = G_{\mathrm{q}}$, $A_{\mathrm{i}} = A_{\mathrm{q}}$, $I/Q_{\mathrm{os}} = 0$, $\theta = 0$, SBRR and LOLRR are infinite. However, in real circuit design, the mismatches are always the nightmare of engineers. Fortunately, Equations (10) and (11) reveal the relations of the spurs and the mismatches; the way to reduce them is also highlighted. According to Eq. (10), SBRR is closely related to the gain mismatches of the I/Q ABB and LO paths. Also, the phase error of the I/Q LO path plays an important role. Therefore, the off-chip microwave balun-1 is chosen to possess a well-balanced output and the differential inputs of the divider are placed near the PAD. As the LO path carries the 6–9 GHz signals, the divider with LO buffers is located as close as possible to the up-mixer to reduce the gain/phase error on the I/Q LO path. In the layout design, the parasitic of the signal path is minimized and the I/Q paths are kept as symmetric as possible.

As indicated in Eq. (9), the power of the LO leakage is determined by the offset of the I/Q ABB path. In order to reduce the power of the LO leakage, an AC coupling is utilized between the V2I unit and the switches of the up-mixer, as shown in Fig. 3. The bias voltage V_{B} is a replica of the DC voltage at node A in the current mirror. With all of the above techniques, SBRR and LOLRR can be reduced to less than –35 dBc.

In addition, the linearity of the up-mixer is mainly affected by the V2I unit while the impact of the switch stage is of less importance[5]. Many techniques[8] have been proposed to improve the linearity of the V2I unit. Although the complete OPAMP-assisted V2I possesses better linearity, its application is restricted by the power consumption to achieve sufficient GBW of the OPAMP for UWB ABB as well as the limited voltage swing because of the low supply voltage. Instead, the simple OPAMP-assisted V2I unit is preferred. As shown in Fig. 3, the V2I unit consists of the input PMOS transistor M1, the source degeneration resistor R_1, the current-mirror transistors M2 and M3, the AC coupling capacitor C_{B} as well as the bias resistor for eliminating the DC-offset in V2I. The feedback loop is composed of M1, R_1, M2, I_1 and I_2, where M2 acts as the simple single-transistor OPAMP. When applied at the gate of M1, the input ABB voltage is directly transferred to the terminals of R_1 because any voltage changes at the gate will be transferred to the source of M1 to maintain a fixed V_{GS}, as required by the current sources I_1 and I_2. Thus the input voltage is converted linearly into its current counterpart with a gain of $1/R_1$. The converted current Δi circulates in M2. Then it is mirrored into the up-mixer by M3. A 400-Ω R_1 is used to improve the linearity at the cost of the gain loss in V2I. To compensate it, a 6-dB gain is set at the current mirror.

Furthermore, a broadband operation of the mixer is achieved by employing a differential inductor L_{d} to peak with the parasitic capacitance C_{par} and two series resistors R_{s} to reduce the Q of the overall load network. The equivalent circuit of the wideband load network is shown in Fig. 3. Its impedance Z_{L} is as Eq. (12), where $L_{\mathrm{s}} = L_{\mathrm{d}}/2$.

$$Z_{\mathrm{L}} = \frac{R_{\mathrm{s}} + SL_{\mathrm{s}}}{1 + SR_{\mathrm{s}}C_{\mathrm{par}} + S^2L_{\mathrm{s}}C_{\mathrm{par}}}. \quad (12)$$

Including the parasitic capacitors at the drain of M4 and the input capacitors of the next stage, $C_{\mathrm{par}} \approx 400$ fF. According to C_{par}, L_{d} is chosen around 2 nH to let the gain peak around the middle of 6–9 GHz. Using these parameters, Z_{L} versus frequency at different R_{s} is plotted in Fig. 5. Larger R_{s} leads to a flatter response but lower gain of the up-mixer. To balance the gain and ripple, a 40-Ω R_{s} is selected.

2.3. Power driver amplifier

Since the PA is the last stage of the transmitting chain, its linearity determines the output IP3 of the transmitter according to Friis' formula. Moreover, the PA should possess sufficient gain to boost the output power of the up-mixer as well as to reduce the impact of former stages on the linearity of the transmitter. A flat gain of the PA is desired, too. In addition, considerations of the rejection to common-mode interferences should be taken because the tail current sources are eliminated to fit the low supply voltage.

As shown in Fig. 6, the 1st stage of the PA is a combination of source follower (M1) and common source (M2) amplifier[9]. The phase shift of the signal passing through the two

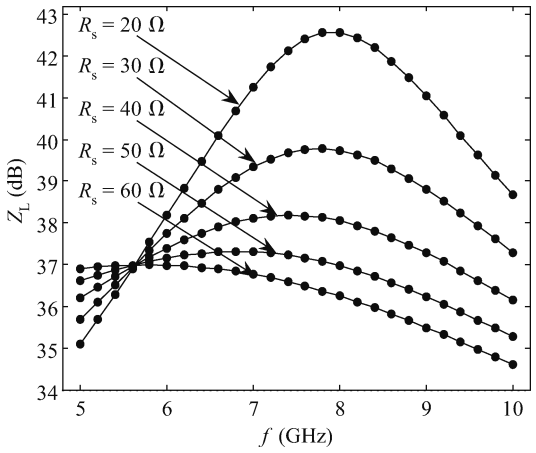


Fig. 5. Z_L versus frequency at different R_S.

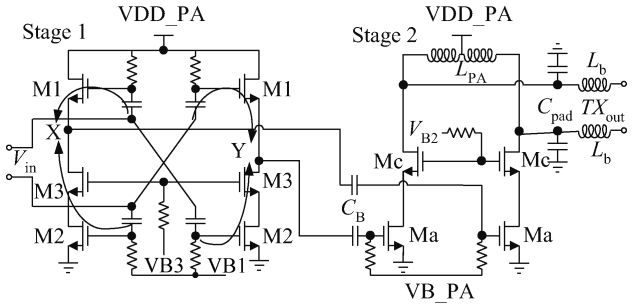


Fig. 6. Simplified schematic of a two-stage PA.

amplifiers is 0° and 180°, respectively. When the input signal V_{in} is applied at the two amplifiers, the common-mode signals in V_{in} become out-of-phase and their amplitudes are subtracted at node X/Y, while the differential-mode signals in V_{in} become in-phase and their amplitudes are added at node X/Y. In this configuration, the input differential signals are amplified with the common-mode signals being rejected. Therefore, the 1st stage increases the common-mode rejection ratio (CMRR) of the transmitter. In order to obtain a high CMRR, the gain of the two appliers, i.e. the source follower and the common source amplifier, should be equal. The transistors M1 and M2 are identical in size. Under this condition, the ideal CMRR is infinite and the differential voltage gain is 6 dB. However, the post simulation of this circuit indicates that the CMRR is improved by 12 dB, and the differential voltage gain is about +2 dB because of the inherent imbalances between the two amplifiers. Moreover, with the impact of the parasitic capacitors, the gain drops at high frequency.

The 2nd stage of the PA amplifies the RF signals to drive the off-chip balun. As the main amplification stage in this PA, its gain and linearity are important. Thus a class-A common source amplifier (Ma) is employed.

A differential inductor (L_{PA}) with a center tap is used as the load of this stage to resonate with the capacitance, including the parasitic capacitance of Mc as well as the PAD. Because the effective 50-Ω input resistors of balun-2 are part of the load network, its Q value is low and the gain is relatively flat. The value of the L_{PA} is optimized according to the PAD capacitance C_{pad} and the bonding inductance L_b to ensure that the peak of the gain is around 9 GHz instead of the middle of

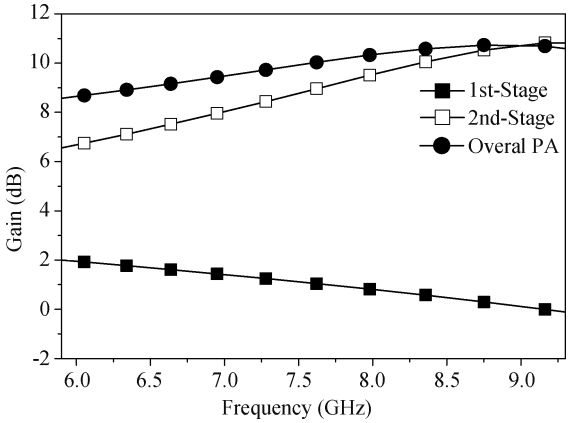


Fig. 7. Post-simulated gain of the PA.

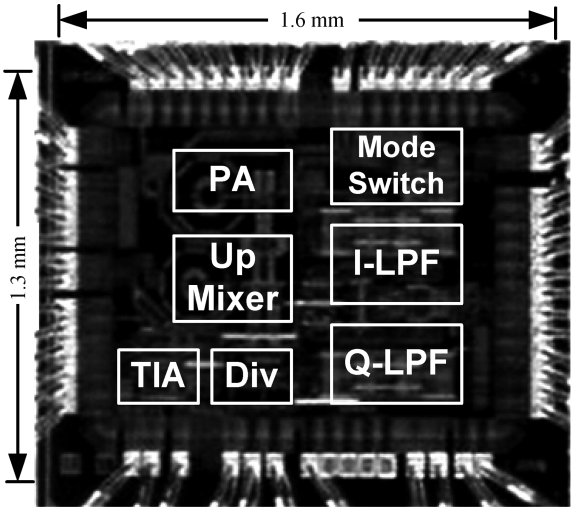


Fig. 8. Photo of a bonded transmitter chip.

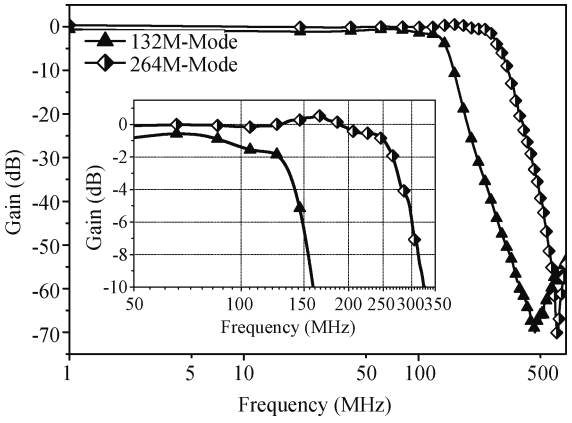


Fig. 9. AC transfer character of the dual-mode LPF.

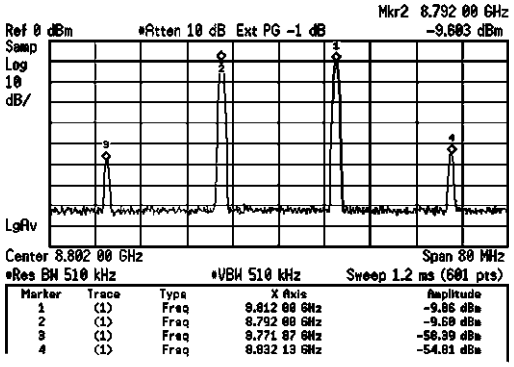
6–9 GHz. Thus it compensates the gain drop of the 1st stage at high frequency, as illustrated in Fig. 7.

In addition, in this PA, the cascode transistors, i.e. M3 and Mc, ease the Miller effect to reduce the effective loading capacitance to the former stage and avoid the breakdown of the transistors during the large signal period. 2-bit digital signals are used to select the required bias voltage for Ma; an 8-dB variable gain is realized.

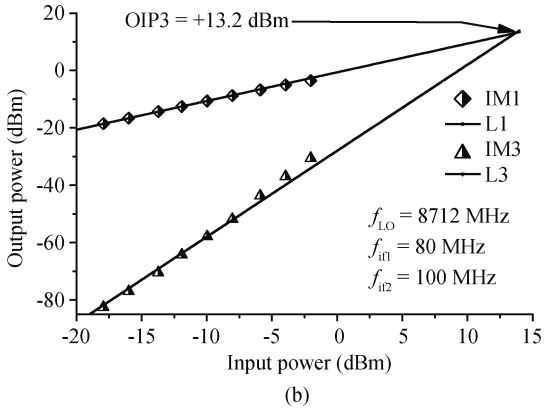
Table 2. Summery and comparison of measurement results.

Parameter	This work	JSSC09[2]	RFIC08[3]	ETRI08[4]	JSemi09[5]
Frequency (GHz)	6–9 (dual-mode)	3–8 (WiMedia)	6–9 (WiMedia)	3–5 (WiMedia)	3–5 (WiMedia)
Tech. CMOS	0.13 μm	0.18 μm	90 nm	0.13 μm	0.18 μm
With LPF (Type)	Yes (g_m–c)	Yes (passive)	No	Yes (active-RC)	No
Output power (dBm)	–6.2	–10	–5.7	0	–7
Gain flatness (dB)	< 3*	n/a.	< 3	< 1.5	< 5
SBRR (dBc)	–38	–42.2	–33.8	–28	–35.6
LOLRR Wi/o Cali (dBc)	n/a./-35	n/a./ –46.5	–47/–35	n/a./ –40	–30.1
OIP3/O1dBCP (dBm)	+13.2/+2.8	n/a./ > –8.2	–1.41/n/a.	+9.3/0	+12/>–1
Power ($I \times V$/(mW))	$46 \times 1.2/55.2^{(a)}$	$20 \times 1.8/36$	$60 \times 1.2/72^{(b)}$	$33.7 \times 1.5/50.55^{(c)}$	$17 \times 1.8/30.6^{(d)}$

*: gain flatness < 3 dB from 6–8.7 GHz, < 5.6 dB from 6–9 GHz; (a): 46 mA = 7.3 mA (LPF) + 4.7 mA (V2I) + 12 mA (up-mixer) + 22 mA (PA) excluding 20 mA (divider + LO buffers); (b): Including current consumption of divider; (c): 33.7 mA = 7.2 mA (LPF) + 13 mA (up-mixer) + 13.5 mA(d2s + PA); (d): Excluding the 15-mA current consumption of divider with LO buffers.



(a)



(b)

Fig. 10. OIP3 of the transmitter at 8712-MHz LO.

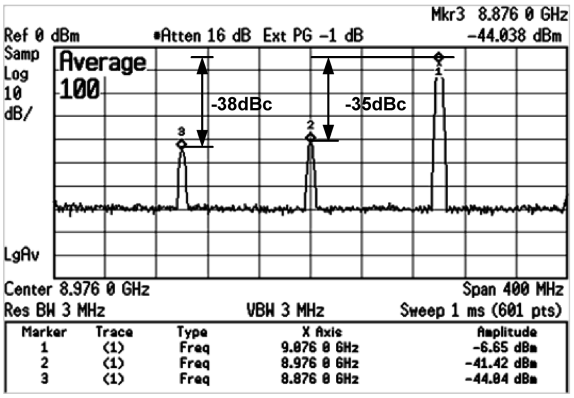


Fig. 11. SB/LOL RR at 8976-MHz LO.

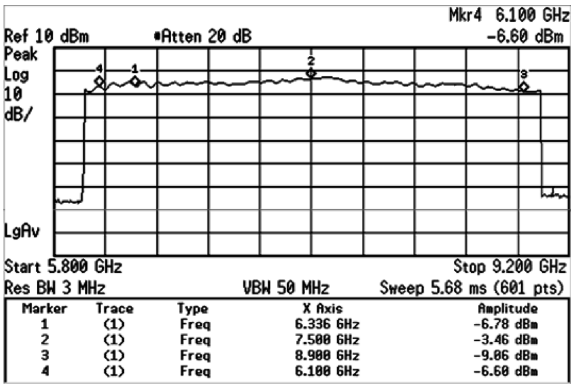


Fig. 12. Gain flatness in 6–9 GHz.

3. Measurement results

The fabricated transmitter chip with dimensions of 1.6 × 1.3 mm^2 is bonded on a PCB via a COB package for measurement, as shown in Fig. 8. The measurements are carried out with the help of both on-chip and off-chip test-assisted circuits and components including the integrated high-speed frequency divider with LO buffers, the TIAs and the off-chip microwave baluns, i.e. the balun-1/2 in Fig. 1.

As shown in Fig. 9, the measured cut-off frequency f_c of the LPF is 272/136 MHz at 264-/132-MHz mode under the proper DCCA control word. The error is less than 3%. Also, by changing the DCCA control word, f_c varies from 200 MHz to 350 MHz at 264-MHz mode and 80 MHz to 180 MHz at 132-MHz mode. Thus accurate control of f_c against the process variations and the mismatches is achieved. In addition, the attenuation of the LPF is –58/–48 dB at $2f_c$ under 264-/132-MHz mode, which is better than is required. The measurement result reveals that the robust LPF works well in both modes.

As depicted in Fig. 10, the output IP3 (OIP3) is measured by a two-tone ABB signal (80 MHz with 100 MHz). The LO frequency is at 8712 MHz, which is a typical LO frequency at high band of UWB. The output spectrum in Fig. 10(a) indicates that the OIP3 = –9.6 + (–9.6 + 54.8)/2 = +13 dBm, which is consistent with the result of Fig. 10(b). Therefore this transmitter possesses high linearity. Also, from Fig. 10(b), we find that the output 1-dB compression point (O1dBCP) is about +2.8 dBm and the conversion gain of the entire transmitting

chain is about +2 dB.

From the output spectrum of the transmitter at the highest LO (8976 MHz), as illustrated in Fig. 11, the SBRR/LOLRR is –38/–35 dBc. This indicates that a low-spur transmitter is obtained. And as in Fig. 12, the gain flatness in 6–8.7 GHz is within 3 dB. However, the gain drops at high frequency because the parasitic capacitor reduces the amplitude of the divider output quickly; the gain flatness in 6–9 GHz increases to 5.6 dB.

Finally, the measurement results are summarized and compared with recent works in Table 2. This indicates that the proposed dual-mode transmitter achieves excellent performance in terms of high linearity and low spurs.

4. Conclusion

With the mode-switch circuits in the LPF, a dual-mode 6 to 9 GHz transmitter for both WiMedia and China MB-OFDM UWB is presented. The measurement results show that this transmitter possesses high linearity (OIP3 = +13.2 dBm and O1dBCP = +2.8 dBm) and low spurs (SB/LOLRR = –38/–35 dBc). The fabricated chip occupies a die area of 2.08 mm^2 and consumes a core current of 46 mA under a 1.2 V supply. This unique transmitter offers a solution to develop compatible OFDM-UWB transmitters under different standards.

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