A highly linear fully integrated CMOS power amplifier with an analog predistortion technique

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Abstract: A transformer-based CMOS power amplifier (PA) is linearized using an analog predistortion technique for a 2.5-GHz m-WiMAX transmitter. The third harmonic of the power stage and driver stage can be cancelled out in a specific power region. The two-stage PA fabricated in a standard 0.18-μm CMOS process delivers 27.5 dBm with 27% PAE at the 1-dB compression point (P_{1dB}) and offers 21 dB gain. The PA achieves 5.5 % EVM and meets the spectrum mask at 20.5 dBm average power. Another conventional PA with a zero-cross-point of g_{m3} bias is also fabricated and compared to prove its good linearity and efficiency.

Key words: linear; CMOS; power amplifier; m-WiMAX; transformer; analog predistortion
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1. Introduction

The ever-growing high speed data transmission of emerging 4 G standards requires PA with both high linearity and efficiency[1−5]. Many techniques have been applied to enhance the poor linearity of CMOS PA, such as gate capacitance compensation and bias control techniques. However, these methods are often at the cost of efficiency or complexity[6−8]. Traditionally, to enhance linearity, the driver stage is preferred to bias at Class A to obtain good AM–AM/AM–PM performance. However, it will result in low efficiency at the back-off power region due to the high quiescent current. In this work, an analog predistortion technique is introduced mainly to enhance both the linearity and the efficiency without any extra components. The power stage is given a low bias (deep Class AB bias) to reduce the quiescent current, and its third harmonics can be canceled out by the predistorted harmonic generated by the driver stage (light Class AB bias). Therefore, both the linearity and the efficiency are improved.

In section 2, the analog predistortion technique employed for CMOS PA is described. In section 3, the fully integrated linear CMOS PA combined with an 8-shape transformer is implemented in a 0.18 μm CMOS process. In section 4, the PA is measured with a 2.5-GHz continuous wave (CW) and a specific m-WiMAX modulation signal. The measurement results are compared with the one with zero-cross-point of g_{m3} bias and prove that the proposed method has good linearity and efficiency.

2. Analog predistortion technique analysis employed for CMOS PA

In CMOS PA operation, the nonlinear harmonics mainly are generated by the nonlinearity of g_m[1, 3]. The behavior can be described as a third-order Taylor expansion in Eq. (1), which neglects some high-order and cross modulation items for simplicity.

$$g_m = g_{m1} + g_{m2}v_{gs} + g_{m3}v_{gs}^2. \quad (1)$$

The second harmonic generated by g_{m2} can be canceled by the differential configuration of CMOS PA. Thus, g_{m3} is the main nonlinear item concerned in this work. g_{m3} variation with gate bias V_{gs} is plotted in Fig. 1. Usually, there is a zero-cross-point at a deep Class AB bias region and the third harmonic can be canceled well at the bias with a small signal operation. However, at a large signal operation, the third harmonic cannot be canceled properly any more because of the

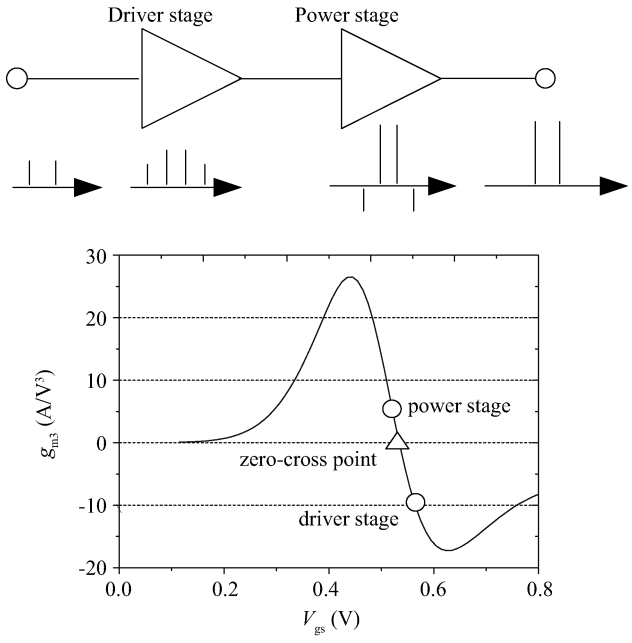

Fig. 1. Illustration of the analog predistortion technique.

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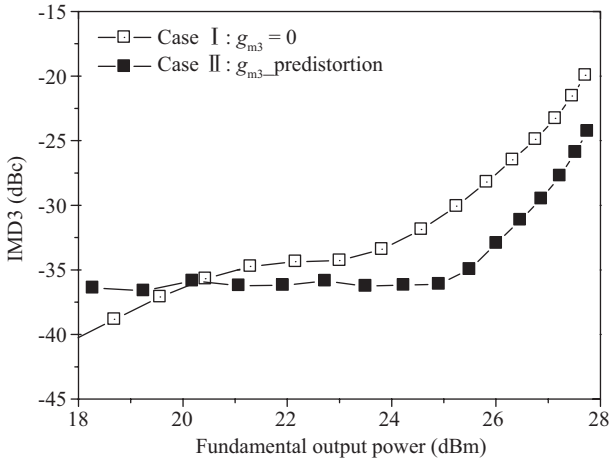
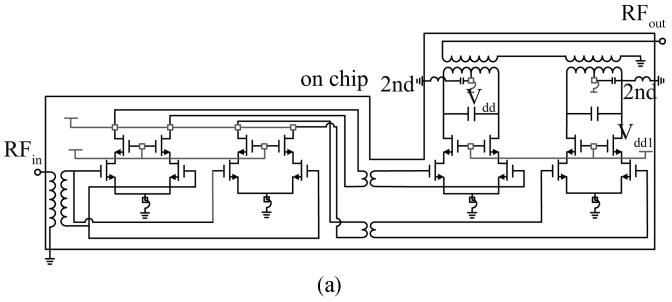
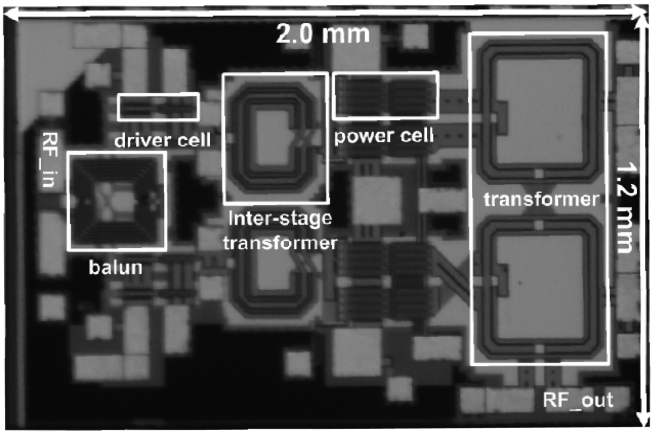


Fig. 2. Comparison of simulated IMD3.



(a)



(b)

Fig. 3. Analog predistorted CMOS PA. (a) Schematic. (b) Chip photograph.

asymmetrical profile. The gate voltage swing is very close to the pinch-off region and the nonlinearity due to C_{gs} can be very large. To improve linearity, the analog predistortion method is proposed, as depicted in Fig. 1. The bias of the power stage and the driver stage is lower and higher than the zero-cross-point of g_{m3}, respectively, and its generated harmonics can be canceled by each other properly, therefore, the net harmonic is minimized.

The simulated IMD3 are compared between the zero-cross-point of the g_{m3} technique (Case I) and the analog predistortion technique (Case II), and are compared in Fig. 2. In a low power region, case I has lower IMD3 due to the good

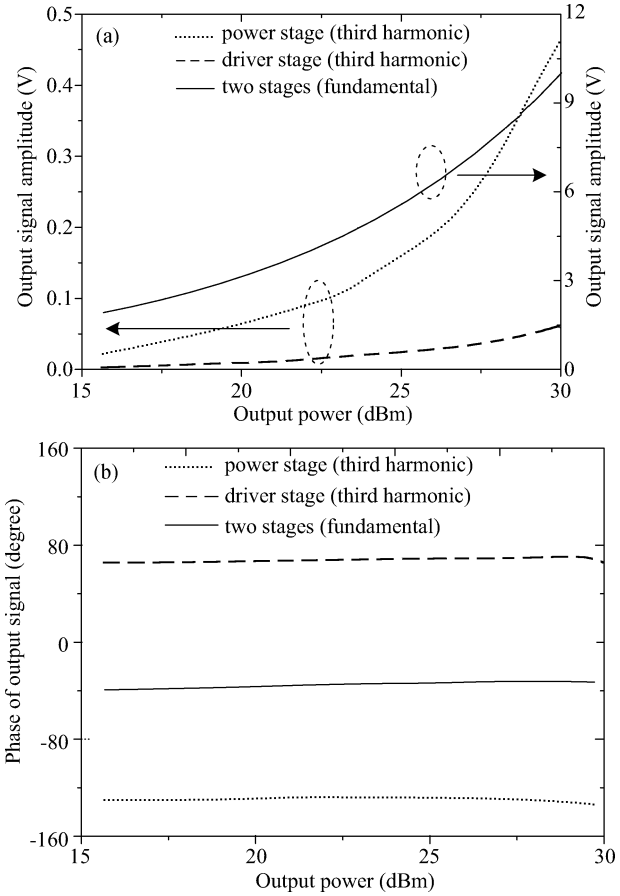


Fig. 4. Simulated amplitude and phase distortion of the driver stage, the power stage and two stages. (a) Amplitude distortion. (b) Phase distortion.

cancellation of the third harmonic. As the power increases, the third harmonic cannot be suppressed accurately because the gate voltage swing reaches the pinch-off region and Case II has lower IMD3 due to the optimized third harmonic cancellation, and it can be improved by about 5 dB between 24 dBm and 27 dBm.

3. Implementation of highly linear CMOS PA

To verify the above analysis, a highly linear CMOS PA is implemented in a standard 0.18-μm CMOS process for a 2.5-GHz m-WiMAX system. A schematic and a chip photograph of the PA are shown in Figs. 3(a) and 3(b), respectively. The single-ended signal is converted to four-way differential signals by an input balun which has about 1.8 dB loss in the simulation, and a 3 : 2 transformer is designed to offer the inter-stage matching between the driver stage and the power stage. Finally, the power is combined with an 8-shape transformer at the output. An ADS2008 MOM simulator is employed for post simulation, and the simulated loss of the transformer is less than 1 dB. Each power cell at the power stage employs the cascode configuration, and the common gate (CG) transistor is selected with a 0.35 μm gate length to enhance reliability and the common source (CS) one is selected with 0.18 μm to achieve high gain. Both stages are supplied with 3.3 V. The gate bias of CS and CG at the power stage are biased at 0.52 V and 2.2 V, and

Table 1. Comparisons among the state-of-the-art linear CMOS PAs.

Parameter	Linearity @ Power	Gain	PAE @ Power	Frequency/Process
Ref. [2]	EVM = 3.5% @ 19 dBm	27 dB	23% @ 27 dBm	2.4 GHz/90 nm
Ref. [6]	ACP1< −35 dBc @ 24 dBm	23.9 dB	29% @ 24 dBm	1.75 GHz/0.5 μm
Ref. [9]	EVM = 5.7% @ 19 dBm	19.8 dB	31% @ 24.5 dBm	2.4 GHz /0.18 μm
Ref. [10]	IM3 < −20 dB @ 19 dBm	8 dB	27% @ 24.3 dBm	5.8 GHz/90 nm
This work	EVM = 5.5% @ 20.5 dBm	21 dB	27% @ 27.5 dBm	2.5 GHz/0.18 μm

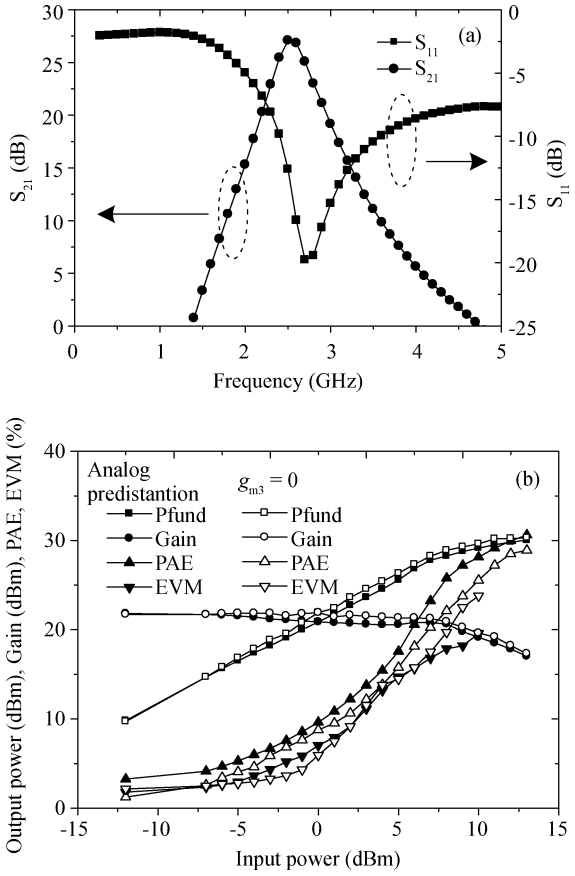


Fig. 5. (a) Small signal performance. (b) Output power, gain, PAE and EVM.

the counterparts of the driver stage are 0.56 V and 2.4 V, which make the net third harmonic suppressed properly at the desired power regions. The total quiescent current of the power stage and driver stage is only 130 mA and is 20% lower than the zero-cross-point of the g_{m3} bias design. The simulated amplitude and phase distortion of the driver stage, then power stage and the two stages are shown in Figs. 4(a) and 4(b). Assuming that the power stage has 10 dB gain, the magnitude of the third harmonic predistorted signal generated by the driver stage is designed as about one tenth of the counterpart at the power stage and out of phase in high power regions (the output power is from 25–28 dBm). Therefore, the distortion of the amplitude and phase for the two stages is minimized and the linearity can be enhanced.

4. Measurement results

The measured small signal performance is shown in Fig. 5(a). The returning loss is lower than −15 dB at the center

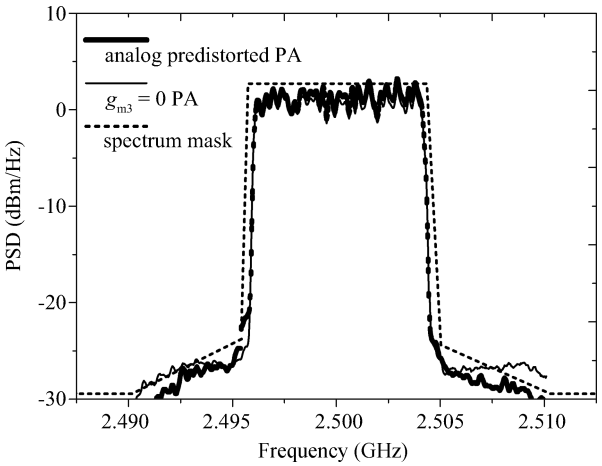


Fig. 6. Spectra at a 20.5 dBm average power level with a m-WiMAX modulation signal.

frequency, presenting good input matching and the small signal gain achieves 28 dB. The CW measurement results at 2.5 GHz are described in Fig. 5(b). The PA delivers 30 dBm with 30% PAE at the saturated point, 27.5 dBm with 27% PAE at the P_{1dB} point and offers 21 dB gain. The counterpart of the measurement results of the PA with the zero-cross-point of g_{m3} bias are also shown with hollowed curves for comparison. We can find that the analog predistorted PA has 4% higher efficiency in the 7 dB back-off region due to the low quiescent current. The gain and output power are only 0.2 dB lower than the compared one. The reliable operation of the PA is also validated in the experiment and the PA can even operate safely at 4.5 V.

The linearity of the PA is measured with a 2.5-GHz 16 QAM m-WiMAX signal which has a 8.75 MHz modulation signal bandwidth and a 9.6 dB PAPR. The EVM and spectrum at 20.5 dBm average power are shown in Figs. 5(b) and 6, respectively. The EVM presents similar results with our analysis, as depicted in Fig. 2, and the analog predistorted PA has 5.5% EVM and meets the m-WiMAX spectrum mask at 20.5 dBm average power. The measured spectrum of the PA with a zero-cross-point of g_{m3} is also shown in Fig. 6, and its spectrum is about 3 dB worse than the analog predistorted one and follows our prediction. In Table 1, the state-of-the-art performance of linear CMOS PAs are summarized and compared with this work. These comparisons reveal that this PA offers competitive performance.

5. Conclusion

A highly linear transformer-based CMOS PA employing the analog predistortion technique is designed in this paper.

The two-stage PA delivers 30 dBm saturated power with 30% PAE, 27.5 dBm with 27% PAE at the P_{1dB} point and has 21 dB gain. Its EVM is lower than 5.5% and the spectrum can meet the WiMAX specification at 20.5 dBm average power. This work proves that the analog predistortion can improve both the linearity and the efficiency of the CMOS PA without compromising the cost and complexity.

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