Analysis and design of a 1.8–2.7 GHz tunable 8-band TDD LTE receiver front-end*

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Abstract: This paper describes the analysis and design of a 0.13 μm CMOS tunable receiver front-end that supports 8 TDD LTE bands, covering the 1.8–2.7 GHz frequency band and supporting the 5/10/15/20 MHz bandwidth and QPSK/16QAM/64QAM modulation schemes. The novel zero-IF receiver core consists of a tunable narrowband variable gain low-noise amplifier (LNA), a current commutating passive down-conversion mixer with a 2nd order low pass trans-impedance amplifier, an LO divider, a rough gain step variable gain pre-amplifier, a tunable 4th order Chebyshev channel select active-RC low pass filter with cutoff frequency calibration circuit and a fine gain step variable gain amplifier. The LNA can be tuned by reconfiguring the output parallel LC tank to the responding frequency band, eliminating the fixed center frequency multiple LNA array for a multi-mode receiver. The large various gain range and bandwidth of the analog baseband can also be tuned by digital configuration to satisfy the specification requirement of various bandwidth and modulation schemes. The test chip is implemented in an SMIC 0.13 μm 1P8M CMOS process. The full receiver achieves 4.6 dB NF, –14.5 dBm out of band IIP3, 30–94 dB gain range and consumes 54 mA with a 1.2 V power supply.

Key words: long-term evolution; receiver; tunable; CMOS
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1. Introduction

Third-generation (3G) wireless systems, such as TD-SCDMA/WCDMA, are now being deployed on a broad scale all over the world. However, user and operator requirements and expectations are continuously evolving, and competing radio access technologies are emerging. The overall target of this long-term evolution (LTE) of 3G[1], sometimes also referred to as beyond 3G or super-3G, is to arrive at an evolved radio access technology that can provide service performance on a par with, or even exceeding, that of current fixed line accesses. LTE is divided into both FDD and TDD mode in the down to date protocol. As TDD mode provides a higher spectrum efficiency and supports smart antenna, which satisfies the MIMO characteristic required by LTE, TDD LTE is preferred in the industry and academic research area. Furthermore, TDD LTE can co-exist and be compatible with the TD-SCDMA system.

Conventional multi-mode receivers use an LNA array[3] or wideband LNA[4] to receive the various bands. As conventional narrowband LNA uses on-chip coils as the input impedance matching and output load, which are bulky devices that occupy a large area, the chip area consumption of the LNA array is quite a challenging issue for SOC. There are also sources of problems that are difficult to predict and control, such as magnetic mutual coupling to nearby inductors, substrate noise coupling, etc. Furthermore, an additional level of switching is required as an interface to the external TDD switch/FDD duplexer. These switches introduce additional losses in front of the LNA and hence degrade the noise figure of the receiver. Moreover, if implemented off-chip, they are costly in terms of added complexity (number of pins), number of external components, and PCB area. It can be argued that the switches may be implemented on-chip but their design is not trivial, even in nanometer CMOS technologies. Such switches require large devices in order to reduce the losses. The result is parasitic non-linear capacitances that require careful co-design with the LNAs. A wideband LNA might be the best choice for a software-defined radio (SDR) or cognitive radio application. However, the voltage gain, NF and linearity are much worse than narrowband LNA, especially in the deep sub-micrometer CMOS process with low power supply and high thermal noise coefficient for deep sub-micrometer device. Furthermore, the power consumption of wideband LNA is at the tens of milliwatts level, which is also a challenging issue for wideband LNA design. Therefore, multi-band tunable narrowband LNA with low power and excellent NF becomes a feasible solution for a multi-mode receiver with a low power supply voltage. Multi-band tunable LNAs are commonly designed using narrow-band LNAs, which have either additional resonators or some sort of reconfigurability by switching passive and active devices. These topologies have been the subject of intense research lately.

This paper proposes a tunable 8-band TDD LTE direct-conversion receiver (DCR), including a tunable narrowband LNA covering 8-band TDD LTE frequency band with a large gain control range, a current commutating passive mixer with 2nd order low pass TIA, an LO divider, a rough gain step variable gain pre-amplifier, a tunable 4th order Chebyshev channel select active–RC LPF with cutoff frequency calibration and a fine gain step VGA and buffer for ADC.

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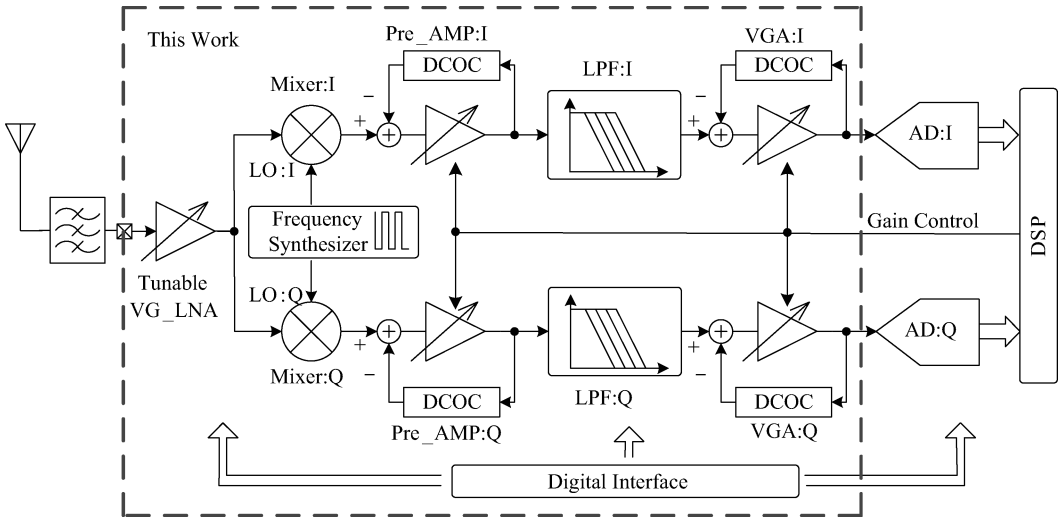

Fig. 1. TDD LTE receiver front-end system architecture.

Table 1. Sensitivity and NF requirement (1/3 QPSK).

Parameter	Channel bandwidth (MHz)			
	5	10	15	20
Sensitivity (dBm)	–100	–97	–95.2	–94
Noise floor (dBm)	–98.5	–95.5	–93.7	–92.5
NF (dB)	9	9	9	9
SNR (dB)	–1	–1	–1	–1
Diversity gain (dB)	3	3	3	3
Margin (dB)	2.5	2.5	2.5	2.5

2. System architecture

TDD LTE covers 8-band in the frequency range 1.88–2.62 GHz and supports multiple bandwidths up to 20 MHz. The system specification requires 9 dB NF and –18 dBm IIP3 to meet the sensitivity and linearity requirement. Taking the 3 dB insertion loss of an off-chip SAW filter, the NF and IIP3 requirements changes to 6 dB and –21 dBm, respectively. The sensitivity and NF requirements with 1/3 code rate QPSK modulation are listed in Table 1.

As the maximum bandwidth reaches 20 MHz and the strict power limitation for the handset device, a direct-conversion receiver (DCR) is chosen to minimize the power consumption. It is strongly desired to have a highly integrated monolithic solution for mobile terminals, which is particularly important since MIMO technology uses several transceiver chains working in parallel, and therefore, the required number of external components increases proportionally with the number of chains. As the zero-IF architecture uses fewer components than other architectures, it is the best candidate for 4G front-ends. Although the disadvantages of DCR, such as $1/f$ noise and I/Q mismatch, restrict the application of DCR, the flexible reconfiguration characteristics (compared with low-IF and high-IF architecture) make it the best choice for software-defined radio (SDR) or reconfigurable receiver to simplify the reconfiguration scheme and the channel select LPF and ADC design[6].

The system architecture with an I/Q path is shown in Fig. 1. In this design, a novel tunable narrowband LNA with a convenient reconfiguration scheme is realized to cover the 1.8–2.7 GHz band. A current commutating passive mixer with a 2nd order low pass TIA is designed to meet the strict linearity requirement of the mixer in a low power voltage design, and the 2nd order low pass TIA also filters part of the out-of-band interference to mitigate the linearity requirement of the following stages by 10 dB. A rough gain step pre-amplifier is applied to amplify the IF signal from the mixer and decrease the noise contribution of the following active-RC LPF. A tunable bandwidth 4th order Chebyshev active-RC LPF is applied to implement the channel selection and anti-alias filtering and a RC constant calibration circuit is used to calibrate the on chip resistance and capacitance variation. A fine gain step variable gain amplifier is used to reduce the dynamic range requirement of the ADC. The digital reconfiguration is given by a digital SPI or scan chain interface. The design of the frequency synthesizer and ADC is not included in this paper.

3. Circuit analysis and design

3.1. Tunable narrowband LNA

Due to the perfect noise performance, a conventional source inductor degenerated LNA is widely used in commercial products. But as the input impedance matching network and output LC tank are two irrelevant networks and the input impedance matching uses off-chip passive device, tuning the center frequency to realize a reconfigurable receiver is quite sophisticated. Several works try to use mutual inductance to relate the input matching network and output LC tank[7]. However, the tuning performance still cannot meet the requirement, and noise and reverse isolation deteriorate[8]. This uses two order network for input matching and output impedance, but it loses the intrinsic perfect noise performance and can only be used for two relative far frequency band.

For a tunable narrowband LNA design, one of the best choices is wideband input matching or a narrowband output load, and the other choice is narrowband input matching and an output load with the same center frequency while tuning. A common gate transconductor with a parallel LC tank load has the characteristic of wideband input matching and a nar-

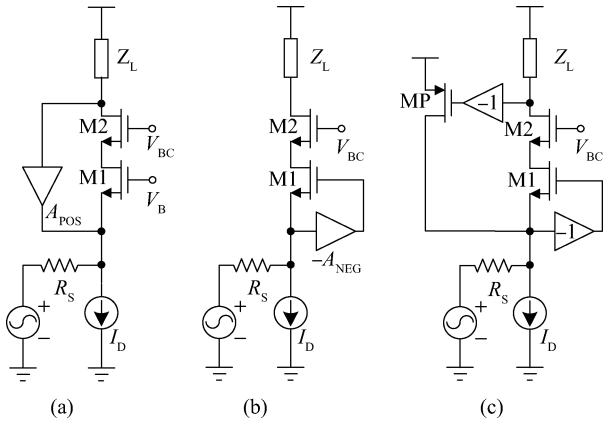

Fig. 2. TDD LTE receiver front-end system architecture.

rowband load, therefore tuning the output LC tank makes the prototype tunable LNA. However, limited by the input matching, the transconductor is fixed as $g_m = 1/R_s$, but the NF is in reverse proportion to the g_m, therefore extra NF optimization schemes, such as noise cancellation and feedback, are introduced to break the limitation of input matching and NF. Noise cancellation uses proportional output loads, which are not suitable for tunable LNA, so in this design, feedback, including positive and negative feedback, are applied to improve the NF.

As shown in Fig. 2(a), the output voltage is fedback by a positive amplifier to the input node, therefore the input impedance is increased by the loop gain and larger g_m can be used to improve the NF and voltage gain[9]. Negative feedback (Fig. 2(b))[10] is also used to boost the transconductor by $1+A_{NEG}$, therefore the noise contribution of M1, which is the main noise contribution of the overall NF, is reduced by $1+A_{NEG}$, and the power consumption is also reduced by $1+A_{NEG}$ if the power consumed by A_{NEG} can be neglected. In Fig. 2(c), positive and negative feedback are combined to improve the NF and voltage gain. A_{POS} can be realized by coupling from the reverse side of the differential LNA, then using a transconductor (MP) to consist of the shunt-shunt feedback. A_{NEG} can be easily realized by a cross-coupled capacitor (CCC) technique. Therefore, the input impedance is

$$Z_{in} = \frac{1}{2g_{mM1}(1 - g_{mMP}Z_L)}, \tag{1}$$

where g_{mM1} and g_{mMP} are the transconductor of M1 and MP, respectively, and Z_L is the load impedance. Therefore, the input impedance matching is directly related to the load Z_L. If a pure resistor is used as the wideband load, the input matching is also wideband, and if a parallel LC tank is used as the narrowband load, the input impedance matches the source impedance at the same center frequency as the LC resonate frequency, which is exactly suitable to realize a tunable LNA with narrowband input matching and output load. And the voltage gain is

$$A_V = 2g_{mM1}Z_L, \tag{2}$$

the overall noise factor is

$$F = 1 + \frac{\gamma(1 - g_{mMP}Z_L)}{2} + g_{mMP}R_S\gamma + \frac{R_S(2 - g_{mMP}Z_L)^2}{Z_L}. \tag{3}$$

In comparison with the conventional common gate LNA, of which the noise factor is approximately $1+\gamma$, the noise contribution of M1 is reduce to $(1 - g_{mMP}Z_L)/2$ times of the conventional common gate LNA. Taking the loop stability into account, $g_{mMP}Z_L$ is set to 1/3–1/2, thus the noise contribution of M1 is reduced to 1/3–1/4 times of the conventional common gate LNA.

Figure 3 presents the tunable narrowband LNA based on the prototype of Fig. 2(c). The input signal is converted to differential by an off-chip wideband balun, and the transconductor transistor M1 is divided to 4 parts (M11A, M12A, M13A, M14A) to realize the variable gain by switching the cascode transistor M2. If G_0 is off, the M22A, M22B, I_{D2} and positive feedback transistor MPA and MPB are off, therefore the structure is degenerated back to the CCC common gate LNA, as shown in Fig. 2(b), and the voltage gain and power consumption are decreased. Lower gain can be realized by controlling G_1 and G_2 to switch off M23A, M24A, M23B and M24B, and the signal current is bypassed to the current source I_{D1} to keep input impedance matching. The bias voltage of the transconductor transistor M1 is generated by common mode feedback loop. The output load is a parallel differential inductor with center tap and capacitor array. Therefore the frequency tuning can be easily realized by reconfiguring the capacitor array switches.

3.2. Current commutating passive mixer with 2nd order TIA

Due to the scaling down power supply voltage, a current commutating passive mode mixer becomes the best choice for a wireless receiver. It also benefits from the superior $1/f$ noise performance and high linearity as there is no internal high impedance node. As shown in Fig. 4, a transconductor converts the signal voltage to signal currents and feeds to the double balanced mixing switches. The switches are driven by LO buffers and biased in such a way that the mixer works only in the ON overlap region to improve the linearity performance[11].

A conventional current commutating mixer applies a simple integrator to realize the current output to voltage output. In this design, a Tow–Thomas biquad is applied to realize the tunable bandwidth TIA and filters the out-of-band interference in current mode, thus alleviating the linearity requirement of the following stages. And the cutoff frequency f_p and Q factor are given by

$$\begin{cases} f_p = \dfrac{1}{2\pi\sqrt{R_1R_3C_1C_2}}, \\ Q = \dfrac{R_2}{\sqrt{R_1R_3}}\sqrt{\dfrac{C_1}{C_2}}. \end{cases} \tag{4}$$

As R_1 is the output load of the current commutating mixer, R_1 and R_3 are fixed to relax the design complexity, and capacitors C_1 and C_2 can be tuned by trans-gates switches to choose the responding bandwidth and an automatic f_p calibration circuit is added to calibrate the on-chip resistor and capacitor vari-

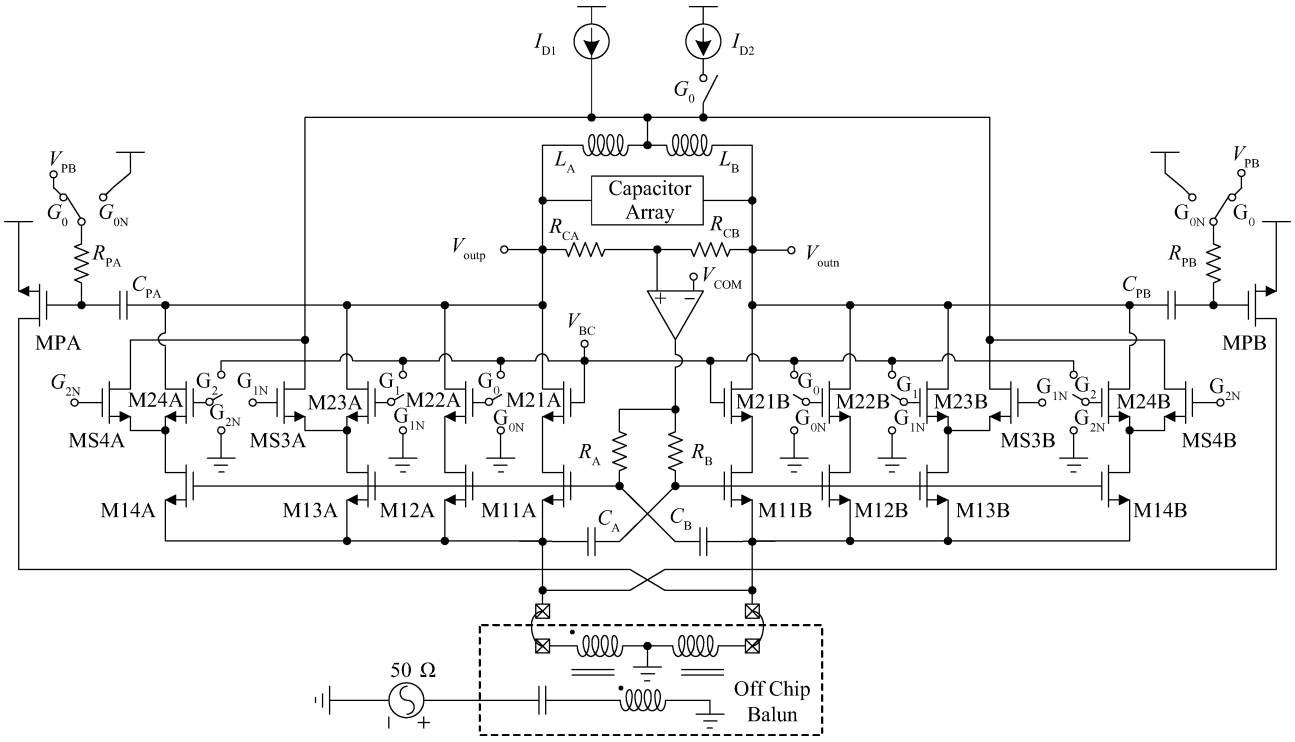

Fig. 3. Proposed tunable narrowband variable gain LNA.

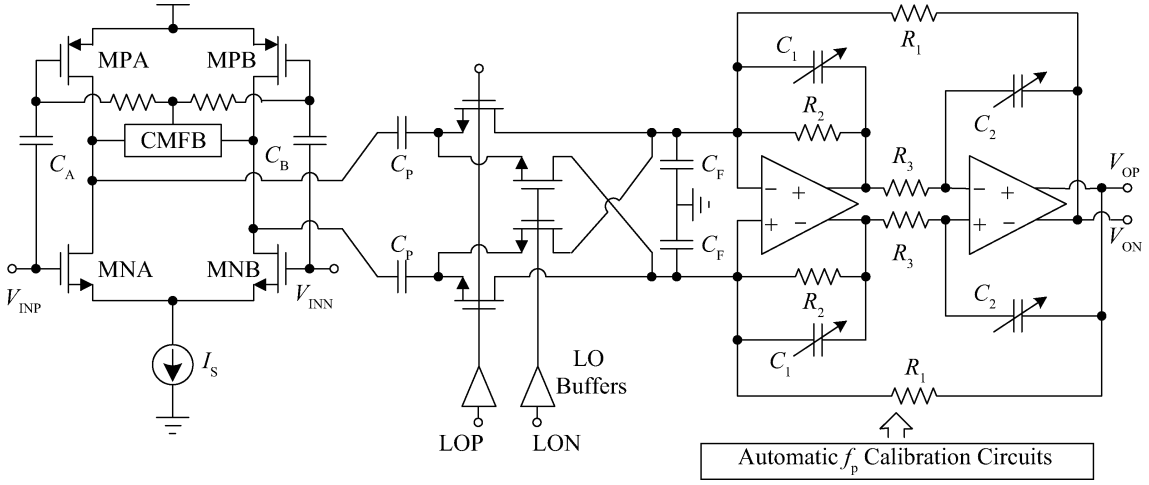

Fig. 4. Current commutating passive mixer with 2nd order TIA.

ation. The classic current mode two-stage OTA with 450 MHz GBW is used in this biquad.

As R_1 is the load resistor and R_3 is one of the main noise contributors and the resistance is limited to one or several kΩ level, a large area capacitor must be used to filter the out-of-band interference, especially for a low bandwidth design. In this design, capacitors are tuned and calibrated to cover the f_p = 2.5/5/7.5/10 MHz bandwidth, and it provides approximate 10 dB attenuation at $2f_p$, thus relaxing the out-of-band linearity requirement of the following stages. As the out-of-band input impedance of this biquad is much higher than the in-band input impedance, an extra capacitor C_F is added to filter RF currents and decrease out-of-band impedance to improve the out-of-band linearity.

3.3. Variable gain pre-amplifier

As the channel select active-RC LPF is one of the main noise contributors to the overall NF of the receiver chain, the voltage gain of previous stages must be high enough to reduce the noise contribution of the LPF. However, limited by the low power supply voltage and the high PAPR in OFDM modulation, the voltage conversion gain of the RF front-end is limited by the out-of-band interference. Due to the out-of-band filtering in the previous 2nd order TIA, a low noise high linearity variable gain pre-amplifier can be added between the mixer and the LPF to reduce the noise contribution of the LPF and increase the overall dynamic range.

A resistor feedback amplifier (Fig. 5) is applied to provide

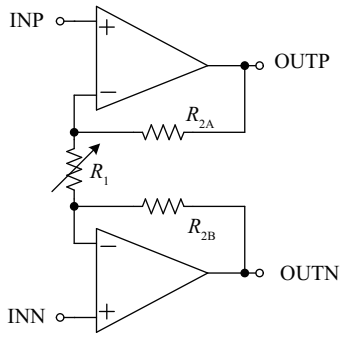

Fig. 5. Variable gain pre-amplifier.

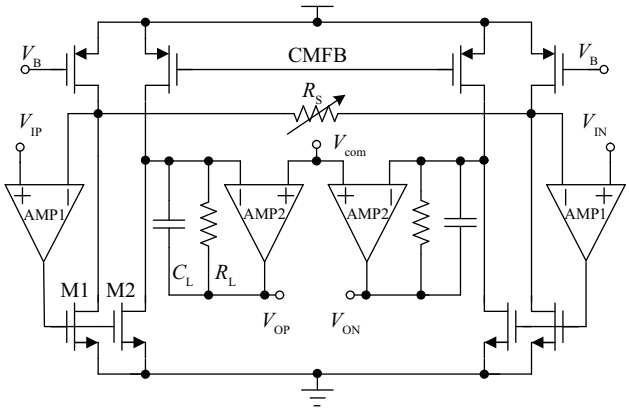

Fig. 6. Schematic of VGA.

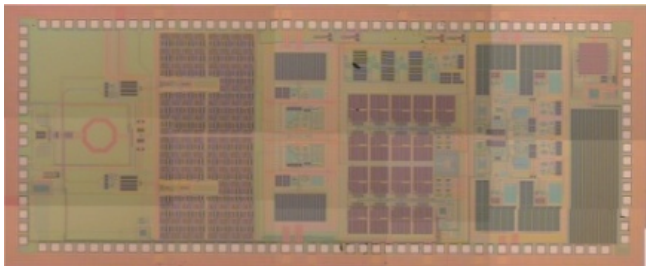

Fig. 7. Micrograph of the testchip.

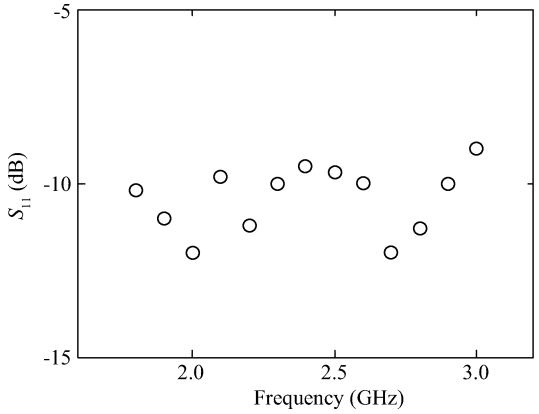

Fig. 8. Input impedance matching.

voltage gain $1 + 2R_2/R_1$, and R_1 can be tuned by switches to realize variable gain from 2 to 20 dB with a 6 dB gain step. An extra low pass feedback loop with a 30 kHz cutoff frequency is added to cancel the dc offset from the intrinsic offset, self-mixing and even order inlinearity.

3.4. Channel select active-RC LPF

A classic 4th order Two–Thomas active-RC LPF is applied to realize the channel selection (each of the stages is similar to the TIA in Fig. 4; the pole and Q factor of each stage is also given by Eq. (4)). As the relative gap adjacent to 20 MHz is just 6.25% required by the protocol, a Chebyshev filter is chosen in this design to provide a steeper roll-off characteristic in comparison with the Butterworth filter. In-band ripple and group-delay are also taken into account as the design tradeoff with a roll-off characteristic. As the noise performance of this LPF is determined by the OTA and capacitor C_1 and C_2, C_1 and C_2 are fixed while the resistors are tuned inversely proportional to bandwidth, therefore channel selection is flexibly reconfigured by a digital interface to configure the switches on/off in the resistor array. An automatic f_p calibration circuit is added to calibrate the on-chip resistor and capacitor variation. The calibration accuracy keeps the RC time constant below 5% variation.

3.5. VGA

A variable gain amplifier and output buffer for the SH circuit of the following ADC is presented in Fig. 6. 9–40 dB gain range and 1 dB gain step are achieved to reduce the dynamic range requirement of the ADC, and the output buffer achieves the setup precision requirement of 10-bits, 100-MHz ADC. The VGA consists of a gm constant transconductor, which is inversely proportional to R_S, and a transimpedance output buffer. The input signal is followed by buffers (made of AMP1 and M1) to R_S, and the signal current flowing through M1 is amplified by M2, then flows through the transimpedance and changes to output voltage. The voltage gain is given by

$$A_V = \frac{(W/L)_{M2}}{(W/L)_{M1}} \frac{2R_L}{R_S}, \tag{5}$$

thus the gain accuracy is determined by the relative match of transistors and resistors. The AMP2 in the transimpedance is a two stage class AB OTA with 600 V/μS slew rate, 450 MHz GBW to satisfy the setup precision requirement of 10-bits, 100 MHz ADC, which uses 4–5 pF sampling capacitor in the SH circuits. Capacitor C_L is used to compensate the pole in the transfer function, which is introduced by the input capacitor at the input port of transimpedance. An extra low-pass feedback loop is used to realize the DCOC with 30 kHz cutoff frequency to cancel the dc offset, which would degrade the DC offset from mismatch and self-mixing.

4. Chip implementation and measurement results

This tunable 8-band TDD LTE receiver front-end is implemented in a SMIC 0.13 μm 1P8M CMOS process. The micrograph of this test chip is presented in Fig. 7. The test chip occupies 1.8×3.5 mm^2 active chip area. To achieve better per-

Table 2. Performance summary.

Parameter		Measured results	Design target
Frequency band (GHz)		1.8–2.7	1.88–2.62
IF bandwidth (MHz)		2.5/5/7.5/10	2.5/5/7.5/10
DCOC cutoff frequency (kHz)		30	–
S_{11} (dB)		< –10	< –10
Conversion gain (dB)		94	90
Channel selection @ $2f_p$ (dB)		38	30
Noise	DSB NF (dB)	4.6	6
	$1/f$ corner (kHz)	150	< 200
Linearity	Out-of-band IIP3 (dBm)	–14.5	–21
	In-band OIP3 (dBm)	27	22
I/Q mismatch	Gain (dB)	0.3	< 1
	Phase (°)	0.5	< 2
Power @ 1.2 V (mA)		54	< 60

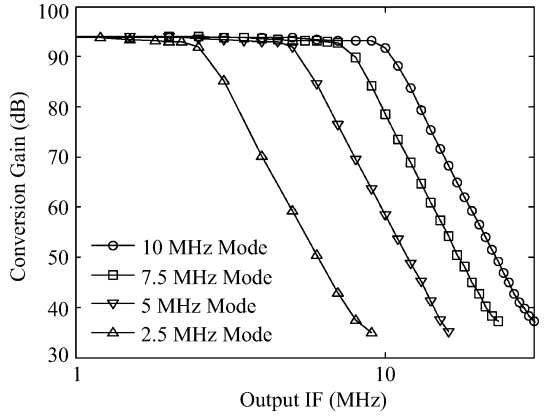

Fig. 9. Maximum voltage conversion gain and channel selection.

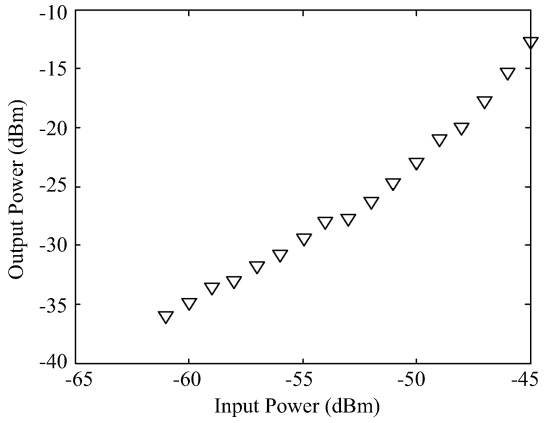

Fig. 10. Out-of-band linearity.

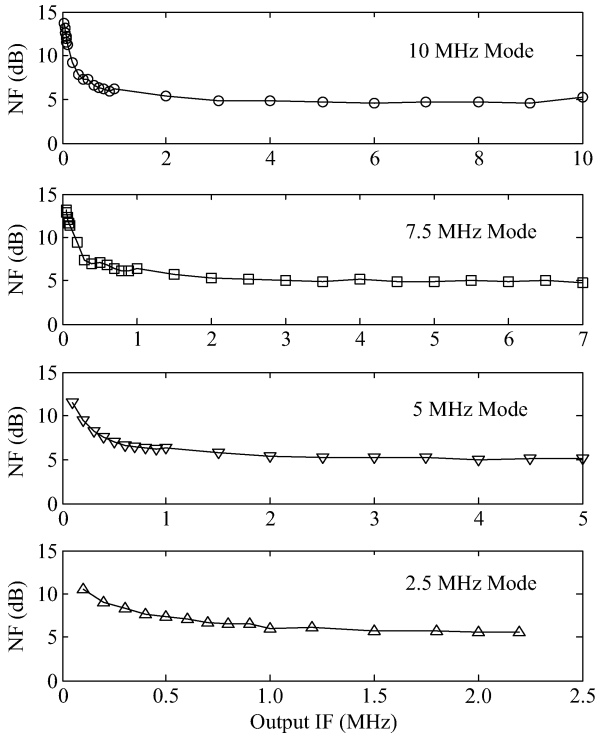

Fig. 11. Measured double sideband NF.

formance, the layout must be given special consideration. An extra isolation guard ring and deep-nwell protection are added to prevent the noise coupled from the substrate. Power supplies for the RF circuits, analog circuit, frequency divider and digital circuits are separated to prevent noise coupling. Bonding pads for RF signals are also optimized to increase electrostatic discharge (ESD) voltage and reduce parasitic capacitor to ground, which results in signal power loss. The test chip is assembled in chip-on-board technology with an external wideband 1 : 1 impedance ratio balun for measurement.

The measurement results show that the chip works well and satisfies the design target. It covers the 1.8–2.7 GHz frequency band and shows –10 dB S_{11} (Fig. 8), and the impedance matching is limited by the wideband characteristic of the off-chip balun. Figure 9 shows that the maximum overall voltage conversion gain reaches 94 dB and 0.4 dB in-band ripple. The RF part (LNA+Mixer) provides 34 dB voltage conversion gain and ABB provides 60 dB IF voltage gain. As the characteristic of the on-chip inductor varies over the wideband frequency band, the maximum gain decreases by 4 dB at the lowest 1.8 GHz frequency point. It supports a 2.5/5/7.5/10 MHz bandwidth and provides the same steep roll-off characteristics in the adjacent channel, about 38 dB @ $2f_p$. As shown in Fig. 10, two tone measurement shows that with –46 dBm out-of-band input power, the 3rd order inter-modulation (IM3) component under maximum gain setup is –15.3 dBm, thus shows –14.5 dBm out-of-band input intercept point (IIP3). The measured double side-band (DSB) NF (Fig. 11) is about 4.6 dB with 150 kHz

$1/f$ noise corner under various bandwidth setups. Table 2 summaries the measurement result in detail. The power consumption is as low as 54 mA with a 1.2 V low power supply voltage (excluding the power consumption of the LO divider).

5. Conclusion

A tunable 8-band TDD LTE zero-IF receiver, which covers the 1.8–2.7 GHz frequency band, is implemented in a SMIC 0.13 μm 1P8M CMOS process. It supports the 5/10/15/20 MHz bandwidth and QPSK/16QAM/64QAM modulation schemes. A tunable narrowband LNA with a flexible tuning scheme and low NF is realized to receive multiband in this design. The measurement results show that the receiver achieves 30–94 dB conversion gain, 4.6 dB DSB NF, –14.5 dBm out-of-band IIP3and 27 dBm in-band OIP3. The receiver satisfies the design target, agrees with the theoretical analysis, and meets the demands of the protocol.

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