A physical-based pMOSFETs threshold voltage model including the STI stress effect*

Wu Wei(吴畏), Du Gang(杜刚), Liu Xiaoyan(刘晓彦)†, Sun Lei(孙雷), Kang Jinfeng(康晋峰), and Han Ruqi(韩汝琦)

Institute of Microelectronics, Peking University, Beijing 100871, China

Abstract: The physical threshold voltage model of pMOSFETs under shallow trench isolation (STI) stress has been developed. The model is verified by 130 nm technology layout dependent measurement data. The comparison between pMOSFET and nMOSFET model simulations due to STI stress was conducted to show that STI stress induced less threshold voltage shift and more mobility shift for the pMOSFET. The circuit simulations of a nine stage ring oscillator with and without STI stress proved about 11% improvement of average delay time. This indicates the importance of STI stress consideration in circuit design.

Key words: STI stress; threshold voltage; mobility; strain
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1. Introduction

While the MOSFET scales down to the nano-scale, the performance improvement of the device is more and more driven by the stress technique[1]. As one of the important intrinsic stress sources, STI induced mechanical stress is non-negligible in nano MOSFET devices. The effect of STI stress on the device characteristics has been discussed from a few years ago to now[2−7]. The well-known BSIM4 phenomenon STI stress model was used to capture the mechanical STI stress effect in the direction of channel length[8]. However, such a model has less physical meaning and more parameters. To accurately and effectively describe the characteristics of MOSFET, it is necessary to develop a more physical threshold voltage and mobility model under STI stress. A physically-based nMOSFET threshold and mobility model of STI stress was described recently[9].

Compared with the nMOSFET, the pMOSFET is more affected by STI stress. This STI stress improves hole mobility in pMOSFETs, which could be one of the approaches to realize high speed CMOS devices as well as reducing the imbalance between n- and p-channel current drive[10]. This paper proposes the physical-based threshold voltage models for the pMOSFET including STI mechanical stress effects. The parameter Δs, meaning the physical strained size under STI stress, $\Delta E_{\rm th}$ and $\Delta E_{\rm m}$, reflects the activation energy per strain due to stress. We use the 130 nm technology pMOSFET layout dependent experimental data including various gate lengths, active areas, and gate locations to verify this model. The comparison between pMOSFET and nMOSFET drive capability under STI stress is also discussed. The new developed threshold model can increase the accuracy of the compact model.

2. STI stress induced models

2.1. Threshold voltage model

In general, the valence band of the pMOSFET is quantized and holes occupy the heavy-hole subband. The strain from stress makes the light-hole and heavy-hole band energy spitted, and the hole band structure of the hole, whatever heavy-hole or light-hole offsets the original quantification and pushes the light-hole band up of heavy-hole band structure, which makes light-hole in predominance[11, 12]. By simplification, the shift in threshold voltage of the pMOSFET due to STI stress can still be described by three items as electron affinity, band gap narrowing, and density of states[12−15], as follows,

$$q\Delta V_{\rm th(SS)} = -\Delta E_{\rm c(SS)} + m\Delta E_{\rm g(SS)} - (m-1)\,kT \times \ln\frac{N_{\rm c(Si)}}{N_{\rm c(SS)}} - mkT\ln\frac{m_{\rm dp(Si)}}{m_{\rm dp(SS)}}, \quad (1)$$

where SS means strained Si under STI stress. m is body effect factor, which is defined in Ref. [15]. $\Delta E_{\rm c(SS)}$ means Si conduction band change under STI stress, and $\Delta E_{\rm g(SS)}$ is band gap change due to STI stress. $N_{\rm c(Si)}$ and $N_{\rm c(SS)}$ in the third item of Eq. (1) are density-of-states of n type bulk Si without and with STI stress, reflecting the density-of-states changes. $m_{\rm dp(Si)}$ and $m_{\rm dp(SS)}$ are effective mass of the confined hole in the inversion layer with and without STI stress. One could assume that the forth item is relatively small[15]. Equation (1) could be

$$q\Delta V_{\rm th(SS)} = -\Delta E_{\rm c(SS)} + m\Delta E_{\rm g(SS)} - (m-1)\,kT\ln\left(\frac{m_{\rm n(Si)}}{m_{\rm n(SS)}}\right)^{3/2}, \quad (2)$$

where $m_{\rm n}$, $m_{\rm n(SS)}$, are bulk electron effective mass without and with STI stress. Like the hole effective mass[9], the third item of the reflecting density-of-states could be[16]

$$\frac{m_{\rm n(Si)}}{m_{\rm n(SS)}} = \exp\frac{\Delta E_{\rm s}}{kT}, \quad (3)$$

where $\Delta E_{\rm s}$ is the activation energy to change the bulk electron effective mass of pMOSFET under STI stress. With Eq. (3), Equation (2) will be

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† Corresponding author. Email: xyliu@ime.pku.edu.cn
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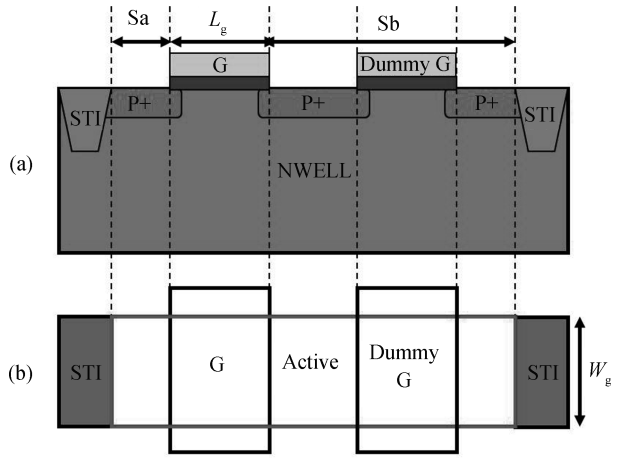

Fig. 1. Illustration of Sa and Sb of the pMOSFET STI stress model. (a) Cross section. (b) Top view.

$$\begin{aligned} q\Delta V_{\text{th(SS)}} &= A\frac{\Delta s}{\text{Sab\_eff}} - \frac{3}{2}(m-1)\Delta E_{\text{s}} \\ &= \left(A - \frac{3}{2}(m-1)B\right)\frac{\Delta s}{\text{Sab\_eff}} \\ &= \Delta E_{\text{th}}\frac{\Delta s}{\text{Sab\_eff}}. \end{aligned} \tag{4}$$

Here, we assumed that ΔE_{s} is linearly dependent on the strain. A includes the activation energy of the electron affinity, the band gap narrowing effect, and B includes the activation energy of the changes in density of states. Thus the parameter ΔE_{th} combines A and B of the activation energy of affinity, band gap narrowing, and density of states together. Δs is the change along the MOSFET channel length under STI stress. Sab_eff is the effective distance between the STI edge and the middle of the gate, as described in Eq. (5) and Fig. 1. Thus Δs/Sab_eff means the strain along the MOSFET channel length under STI stress.

We calculate the Sa and Sb to describe STI stress layout dependence, based on the method in Ref. [6]. The values of ΔE_{th} and Δs are achieved by fitting

$$\text{Sab\_eff} = \frac{1}{\dfrac{1}{L_{\text{g}} + 2\text{Sa}} + \dfrac{1}{L_{\text{g}} + 2\text{Sb}}}. \tag{5}$$

The mobility of the pMOSFET devices is more affected by STI stress than the nMOSFET. But we may still use the similar mobility model as the nMOSFET in our previous study of the nMOSFET under STI stress to describe it[9]. ΔE_{m} and Δs are the key parameters in this mobility model. Our comparison results of mobility between the pMOSFET and the nMOSFET under STI stress imply that using this mobility is acceptable.

2.2. Model parameter extraction method

As in the above analysis, the model parameters of the pMOSFET STI stress include threshold and mobility parameters: Δs, ΔE_{th} and ΔE_{m}. These parameters need to be extracted. The extraction steps and final extracted values are as follows:

Table 1. pMOSFET V_{th} comparisons between the model with and without STI stress consideration.

Parameter	Calculated V_{th} without STI stress model (V)	Calculated V_{th} with STI stress model (V)
Sa = 0.9, Sb = 0.9	−0.682	−0.682
Sa = 0.9, Sb = 14.2	−0.682	−0.676
Sa = 12.6, Sb = 2.8	−0.682	−0.672

(1) ΔE_{th} and ΔE_{m} unit is eV, and Δs unit is μm.

(2) A BSIM3 pMOSFET original model is extracted from Sa = Sb = 0.9 device to have good fitting.

(3) For wide x short device I–V data with different Sa and Sb, ΔE_{th} and ΔE_{m} and Δs are tuned interactively in order to have a balance fitting results among all of the I–V data.

(4) In our modeling, ΔE_{th} is –110 eV. ΔE_{m} is –61 eV, and Δs is $-7.8 \times 10^{-5}\,\mu$m.

3. Results and discussion

In this part, we used 130 nm technology wide x short pMOSFET experiment data to verify the model first. Since the pMOSFET and the nMOSFET are both affected by STI stress, we made comparisons between the pMOSFET and the nMOSFET performance under STI stress secondly. Finally, to verify the effect of STI stress on the circuit, a nine stage ring oscillator with and without STI stress was simulated.

3.1. Model verification

The WxS devices are most sensitive to the STI induced stress. Therefore, we made a BSIM3 original model of the WxS pMOSFET device based on the experimental data with the minimum and equal Sa and Sb. (All of the geometries are normalized by the minimum gate length.) The STI stress should be maximum at this case. Secondly, we integrate our STI stress model into the above model to simulate the experimental data with a different active area. Figure 2 shows that the measurement data fit well after our STI stress dependent model was integrated into the original model.

In our verification, the original model from the device with minimum Sa and Sb will over-predict the threshold if the Sa and Sb are increased. Table 1 shows that the pMOSFET threshold voltage was modeled by our STI stress model. Figure 2 also shows that the over-prediction of the simulated I–V values was corrected by the integrated STI stress model.

3.2. Model discussion

The STI stress influences on the pMOSFET and nMOSFET device characteristics were compared. First, we compared the pMOSFET and nMOSFET mobility shift due to STI stress, as shown in Fig. 3, in order to show that our mobility model of the pMOSFET is acceptable and the threshold voltage model will not be affected by the existing mobility model. It can be seen that the mobility shifts by STI stress of the nMOSFET and the pMOSFET are different. The STI stress increases the pMOSFET channel mobility and decreases the nMOSFET channel mobility, which is consistent with conclusions of previous studies[17]. This indicates the possibility of improving

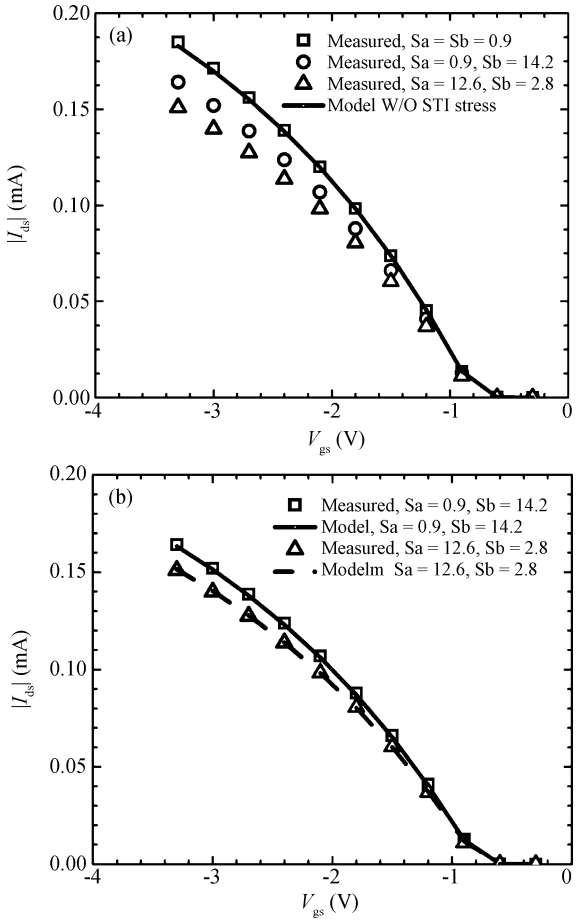

Fig. 2. Comparison between the pMOSFET I_{ds}–V_{gs} model and measured data. (a) The original model without STI stress consideration cannot fit the measurement data with a different active area. (b) With the STI stress model included, the measurement data are fitting well.

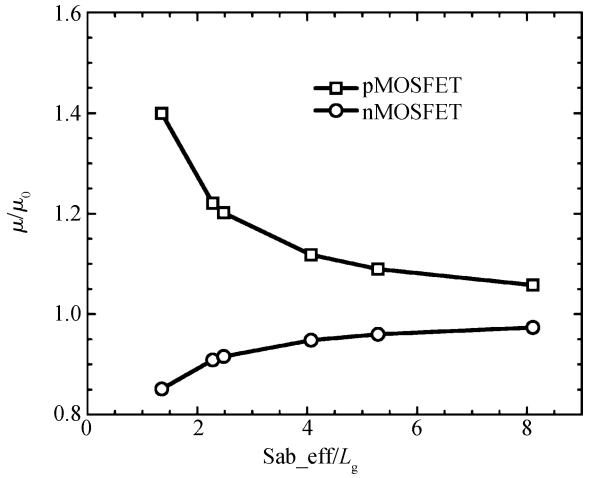

Fig. 3. Comparison between the pMOSFET and nMOSFET mobility changes by STI layout dependence.

the pMOSFET performance by the appropriate layout placement of the STI.

Figure 4 shows the threshold voltage shift due to STI stress of the nMOSFET and the pMOSFET. It can be seen that the absolute threshold voltage of the pMOSFET is less affected by

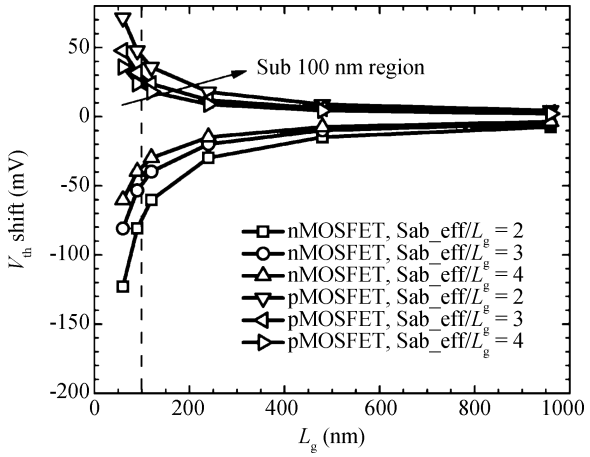

Fig. 4. Comparison between the pMOSFET and nMOSFET threshold voltage shift prediction by the STI stress induced model when the gate length scales down to the sub 100 nm region.

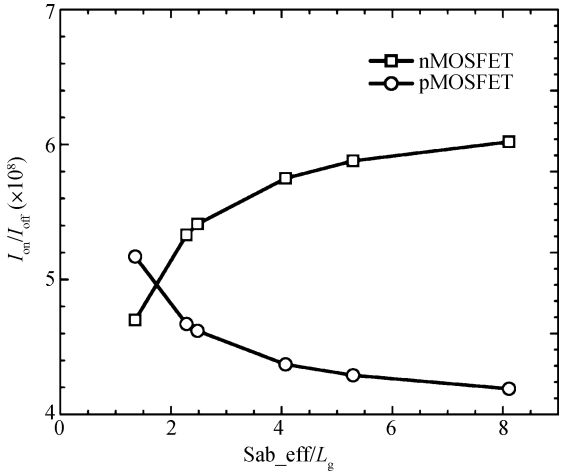

Fig. 5. I_{on}/I_{off} ratio comparison between the pMOSFET and the nMOSFET under STI stress.

STI stress than that of the nMOSFET, although they are both shifted by tens of milli-volts by STI stress.

The drive capability of the nMOSFET and the pMOSFET with STI stress are compared, as shown in Fig. 5. The I_{on} and I_{off} ratio comparison shows that STI stress is helpful to improve the drive capability of the pMOSFET, while the nMOSFET drive capability is decreased by STI stress.

As a validation of our STI stress model, a nine stage ring oscillator circuit was simulated to evaluate the impact of STI stress in the performance of a practical circuit. The transient simulation of the oscillator with or without the STI stress model is shown in Fig. 6. Because of the improvement of the driven capability, the average delay time of the oscillator was improved from 0.105 to 0.0938 ns, by almost 11%, due to STI stress. This indicates the importance for a designer to be able to use STI layout dependent location to improve the performance of the circuit.

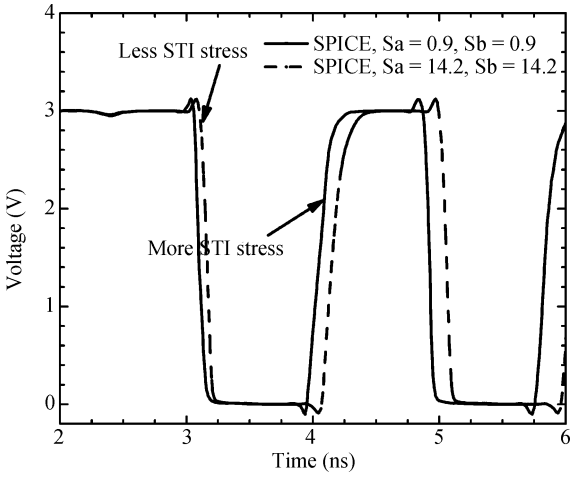

Fig. 6. Time delay comparison of the ring oscillator between two STI layout locations corresponding to more and less STI stress.

4. Conclusions

Physical-based STI stress depended pMOSFET models were developed to describe the threshold voltage and mobility changes under STI. The strain Δs/Sab_eff and respective activation energy parameters were included in these models. The parameter extraction method was described. The model was verified by a 130 nm technology pMOSFET experiment with a different active area. The STI stress effects on the nMOSFET and the pMOSFET were discussed and compared. Simulation for the impact of STI stress on circuit performance was investigated by a nine stage ring oscillator circuit. It was verified that the pMOSFET characteristics were oppositely affected by STI stress to that of the nMOSFET. STI induced stress changed the pMOSFET key characteristics, whatever channel mobility or threshold voltage, more than which nMOSFET was changed. Using a pMOSFET and a nMOSFET under STI induced stress, we can intentionally improve the circuit performance of the design.

Appendix A

The detail deduction from Eq. (1) to Eq. (4) is as follows.

The shift of threshold voltage of the pMOSFET due to STI stress can be described by three items—electron affinity, band gap narrowing, and density of states[12−15]—as follows,

$$q\Delta V_{\mathrm{th(SS)}} = -\Delta E_{\mathrm{c(SS)}} + m\Delta E_{\mathrm{g(SS)}} - (m-1)\,kT \times \ln\frac{N_{\mathrm{c(Si)}}}{N_{\mathrm{c(SS)}}} - mkT\ln\frac{m_{\mathrm{dp(Si)}}}{m_{\mathrm{dp(SS)}}}. \tag{A1}$$

$m_{\mathrm{dp(Si)}}/m_{\mathrm{dp(SS)}}$ could be 1–2[15], which makes the fourth item of Eq. (A1) very small. Equation (1) will be

$$q\Delta V_{\mathrm{th(SS)}} = -\Delta E_{\mathrm{c(SS)}} + m\Delta E_{\mathrm{g(SS)}} - (m-1)\,kT\ln\frac{N_{\mathrm{c(Si)}}}{N_{\mathrm{c(SS)}}}. \tag{A2}$$

From the definition of electron current density, $N_{\mathrm{c}} = 2\left[2\pi kTm_{\mathrm{n}}/h^2\right]^{3/2}$,

$$\frac{N_{\mathrm{c(Si)}}}{N_{\mathrm{c(SS)}}} = \left(\frac{m_{\mathrm{n(Si)}}}{m_{\mathrm{n(SS)}}}\right)^{3/2}. \tag{A3}$$

Under STI stress, it could be assumed that $m_{\mathrm{n(SS)}} = m_{\mathrm{n(Si)}}\exp\left(-\frac{\Delta E_{\mathrm{s}}}{kT}\right)$[16]. With Eq. (A3), Equation (A2) will be

$$q\Delta V_{\mathrm{th(SS)}} = -\Delta E_{\mathrm{c(SS)}} + m\Delta E_{\mathrm{g(SS)}} + \frac{3}{2}(m-1)(-\Delta E_{\mathrm{s}}). \tag{A4}$$

We assumed that the activation energies, $\Delta E_{\mathrm{c(SS)}}$ meaning Si conduction band change under STI stress, $\Delta E_{\mathrm{g(SS)}}$ meaning band gap change due to STI stress, and ΔE_{s} meaning the activation energy of effective mass change, are linearly dependent on the channel strain. Then Equation (A4) will be

$$q\Delta V_{\mathrm{th(SS)}} = -A'\frac{\Delta s}{\mathrm{Sab\_eff}} + mB'\frac{\Delta s}{\mathrm{Sab\_eff}} - \frac{3}{2} \times (m-1)\left(C'\frac{\Delta s}{\mathrm{Sab\_eff}}\right). \tag{A5}$$

There must be one parameter ΔE_{th}

$$\Delta E_{\mathrm{th}} = -A' + mB' - \frac{3}{2}(m-1)\,C'. \tag{A6}$$

Thus Equation (A5) could be

$$q\Delta V_{\mathrm{th(SS)}} = \Delta E_{\mathrm{th}}\frac{\Delta s}{\mathrm{Sab\_eff}}. \tag{A7}$$

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