Fabrication and characteristics of a 4H-SiC junction barrier Schottky diode*

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Abstract: 4H-SiC junction barrier Schottky (JBS) diodes with four kinds of design have been fabricated and characterized using two different processes in which one is fabricated by making the P-type ohmic contact of the anode independently, and the other is processed by depositing a Schottky metal multi-layer on the whole anode. The reverse performances are compared to find the influences of these factors. The results show that JBS diodes with field guard rings have a lower reverse current density and a higher breakdown voltage, and with independent P-type ohmic contact manufacturing, the reverse performance of 4H-SiC JBS diodes can be improved effectively. Furthermore, the P-type ohmic contact is studied in this work.

Key words: 4H-SiC; junction barrier Schottky; field guard ring

1. Introduction

With increasing interest in SiC Schottky barrier diodes (SBD) in power conversion applications, much effort has been focused on improving SiC SBD performance. The junction barrier Schottky (JBS) diode offers the Schottky-like ON-state with fast switching characteristics, and the PiN-like OFF-state characteristics with low leakage current. Several SiC JBS diodes have been reported by different groups[1−4]. The conduction loss can be much lower than that of a PiN diode with a breakdown voltage of less than 3 kV due to the high (2.7 V) turn-on voltage of the SiC P–N junction[5]. The leakage current of the JBS diode is lower than that of a SBD, owing to the high electric field shielded away from the Schottky contact by a depletion layer of P–N junctions. As shown in Fig. 1(a), the anode contains a Schottky contact above the SBD regions and a P-type ohmic contact above the P^+ regions, so it is fabricated simultaneously by deposit Schottky contact metal in the customary process, as shown in Fig. 1(b). In this work, two kinds of processes to fabricate the anode were employed to study the influence on the electrical characteristics of the JBS diodes.

To design a JBS diode with a high breakdown voltage, several kinds of termination can be used, such as a junction termination extension and a mesa termination. However, these terminations require etching and extra ion implanting. To reduce the processing steps and avoid the disadvantages caused by these extra steps, the filed guarding ring (FGR) was fabricated with P^+ for the main junction simultaneously in this work. The 4H-SiC JBS diodes with and without FGRs were fabricated by the two different processes mentioned above.

2. Design and fabrication

A 10 μm N^- epilayer with doping of 1.56×10^{15} cm^{-3} was grown on the N^+ substrate purchased from CREE, with a doping concentration of more than 1×10^{18} cm^{-3}. Samples 1 and 2 were processed on the substrate with different techniques separately. First of all, the circular P^+ regions for the samples were formed at the same time. Multiple implantations were implemented at 400 ℃ in argon ambience. Al ion implantation was with energy of 30, 280, and 500 eV, while the doses of 8.6×10^{13}, 5.2×10^{14}, and 7.8×10^{14} cm^{-2} were taken, respectively.
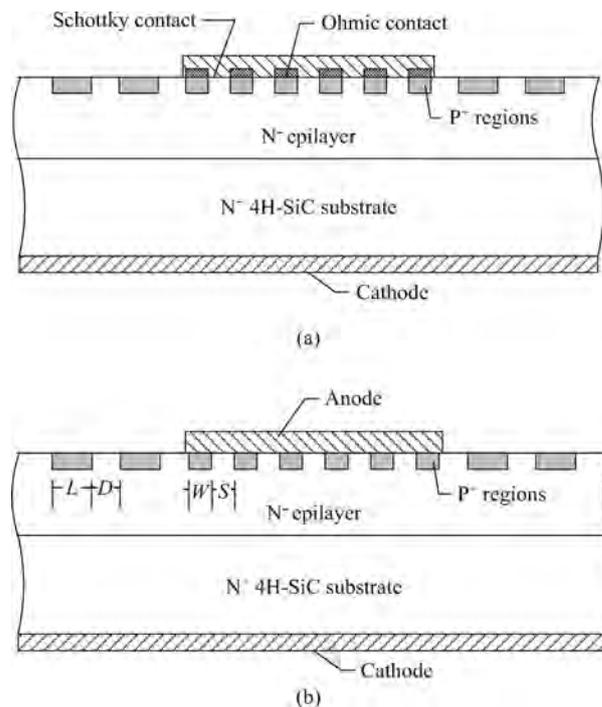
Fig. 1. Schematic cross section of the JBS diodes.

Parameters for all structures are shown in Fig. 1(a), and all of the parameters' values were chosen to be the same for both samples. The P$^+$ junctions are characterized by the width of the P$^+$ implantation window (W) and the spacing in between (S). FGRs are characterized by the width of a single ring (L) and the spacing between the two nearest rings (D). According to Ref. [6], L was chosen to be the fixed value 5 μm, and D = 2.5 μm in the experiment. For convenient description in this paper, the JBS will be marked as JBS (S, W). In this work, the four structures with different designs are (a) JBS (2.5, 4) without edge termination; (b) JBS (2.5, 4) terminated by FGRs; (c) JBS (3, 4) without edge termination; and (d) JBS (3, 4) terminated by FGRs. FGRs with $L = 5$ μm for each ring were implanted around the periphery of the forward conducting active area to reduce electric field crowding at the edge of the diode under reverse bias. All of the FGRs were formed simultaneously with the P$^+$ junction regions with ion-implantation, thus the depth and concentration are the same as the P$^+$ junction regions. The samples were annealed at 1650 ℃ for 45 min in argon ambience. Then, the profile in 0.6 μm depth was measured.

It is well known that a high temperature annealing (> 1000 ℃) is usually required for ohmic contact activation. The fact that the melting temperature of Al (660 ℃) is much lower gives rise to contact morphological problems. It was reported that Al melted during the high temperature anneal[7], spilling over the surface of the devices, potentially damaged the periphery of the devices. To improve the contact morphology, according to Ref. [8], a multi-layer of Ti/Al/Ti/Al/Ti/Al/Ag was deposited on sample 1's top of P$^+$ junction regions after P$^+$ regions done, and then an annealing at 1000 ℃ in a gas mixture of 97% N$_2$ and 3% H$_2$ for 2 min was carried out to create a P-type ohmic contact.

Both samples underwent tri-layer metallization of Ti/Ni/Ag to form a backside contact. Sample 1 was annealed for 2 min and sample 2 was annealed for 5 min at 1000 ℃ in a gas mixture of 97% N$_2$ and 3% H$_2$. Finally, bi-layer metallization of Ti/Ag was used to form the front Schottky metal contact for both samples. Figure 2 shows the scanning electron microscope (SEM) photographs of both samples. It was previously thought that sample 2 had a much better periphery than sample 1 since sample 2 was not annealed to make P-type ohmic contact. As can be seen in Fig. 2(a), the Al spilled a little over the edge of the anode area for sample 1. This can be improved if a thinner Al layer is chosen and the Ti/Al multi-layer superposition time is increased[8].

3. Results and discussion

The fabricated devices were electrically measured at room temperature using a Tektronix 370B programmable curve tracer and an Agilent B1500A semiconductor device analyzer.

Figure 3 shows a comparison of the reverse current density versus reverse voltage between JBS (2.5, 4) and JBS (3, 4) from each sample. As we know, when the JBS is reverse biased, the depletion layers of the adjacent P–N junctions will spread wider, leading to a reduction in the width of the Schottky channel. After the depletion layer is pinched off, a potential barrier for SBD is formed, then the depletion layer is extended toward the N$^+$ substrate with further increasing reversed voltage[9].
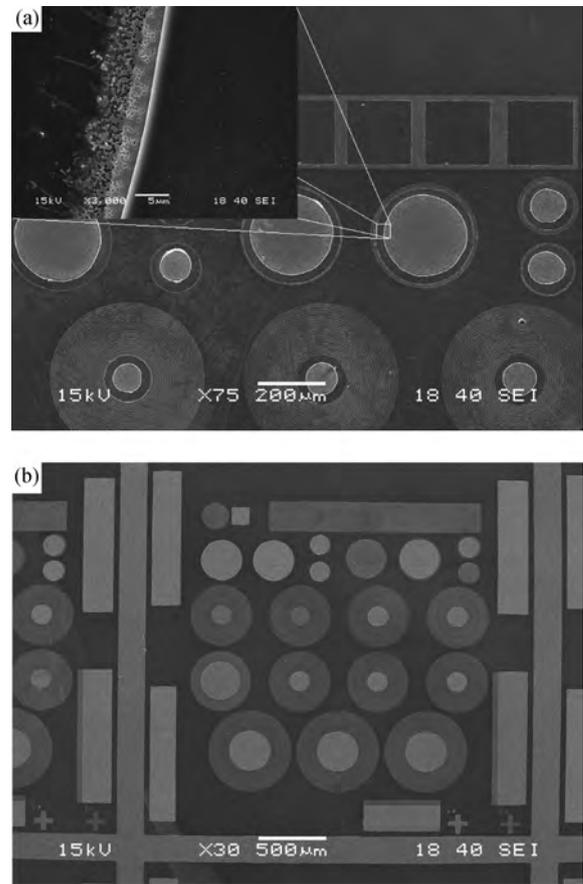
Fig. 2. SEM photos of both samples. (a) Sample 1. (b) Sample 2.
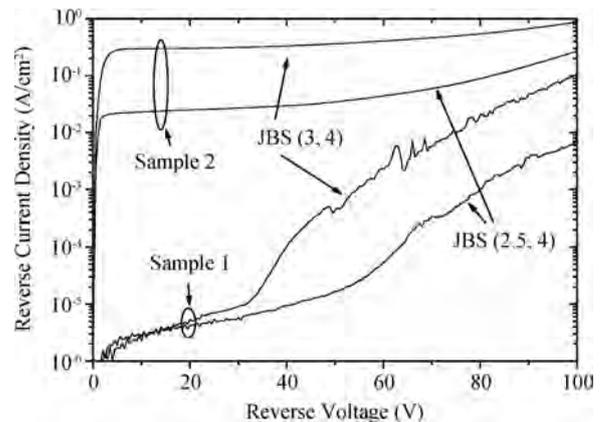
Fig. 3. Reverse V–J characteristics of JBS diodes with different values of S for samples 1 and 2.

However, as can be seen from this figure, the current densities from sample 1 have much lower reverse current densities than those of sample 2. As mentioned above, the P-type contact for sample 2 is not independently fabricated, which causes the barrier on the P$^+$ regions to be much higher then excepted, and the depletion layers between the two nearest P$^+$ regions will not pinch off effectively. Figure 3 shows a comparison between two JBS diodes with different S. Apparently, the JBS diode with $S = 2.5$ μm has a lower reverse current density than the one with $S = 3$ μm.

It can be seen from Fig. 4 that the reverse current den-
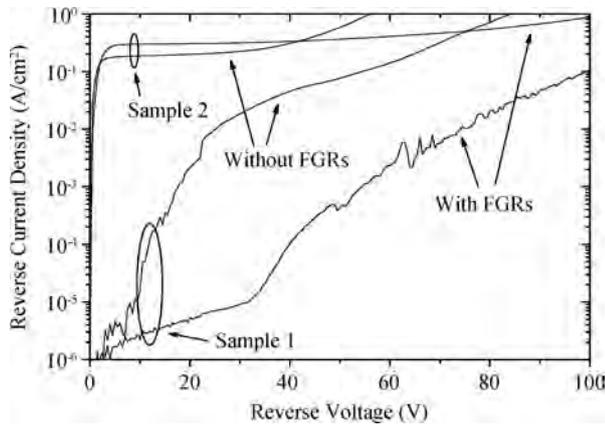
Fig. 4. Reverse $V-J$ characteristics of JBS diodes with and without edge termination for samples 1 and 2.

Fig. 5. Forward $V-J$ characteristics of SBD and JBS diodes.

sity of JBS diodes with FGRs are much lower than those without FGRs, since FGRs can effectively reduce the field crowding in the edge of devices, it has a higher breakdown voltage. In this work, JBS diodes with a breakdown voltage of up to 400 V when the current density is lower than 1 A/cm^2 is created with FGRs[10]. However, the FGR structure with different ring spacing and ring widths is difficult to optimize, and interface charges influence the breakdown voltage significantly, since we didn't apply any passivation layer on the surface of the devices, so the reverse current in this work is a little higher correspondingly.

The dominant mechanism of reverse current depends on the Schottky barrier height, temperature, applied voltage, surface status, and defects in the material. According to the techniques we employed during manufacture, the main reasons for a relatively high leakage current and low breakdown voltage are as follows:

(1) Ti is used as the metal to form the Schottky barrier.

Using the thermionic emission theory, the current through the SiC Schottky diode can be expressed by

$$I = AA^*T^2 \exp\left(-\frac{\phi_B}{kT}\right)\left[\exp\frac{qV}{nkT} - 1\right], \qquad (1)$$

where A is the diode area, A^* is the Richardson's constant, ϕ_B is the Schottky barrier height, n is the ideality factor, and other constants have their usual meanings.

The forward $V-J$ characteristics of SBD and JBS diodes are shown in Fig. 5. Calculated with Eq. (1), the barrier height formed in this work is 0.79 eV, which is smaller than that fabricated with Ni ($\phi_B = 1.26$ eV)[11].

(2) Multi-step ion implantation brought in damages in the space lattice.

(3) The epilayer material deterioration in high temperature annealing, which was stated previously. To reduce the damage during a high-temperature activation anneal, AlN can be used to prevent silicon evaporation from the 4H-SiC surface[12].

4. Summary

The process that fabricates a P-type ohmic contact independently has been employed to fabricate 4H-SiC JBS diodes.
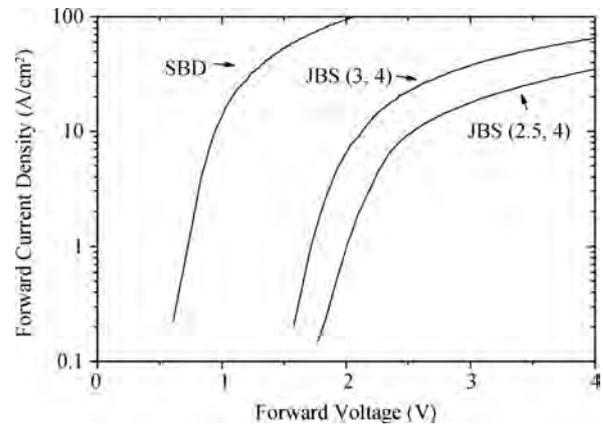
The influence of FGRs in the reverse characteristics of JBS diodes has been studied. Results show that the JBS diodes with P-type ohmic contact fabricated independently have a better performance than those by the customary process and with P+ regions doping concentration ($\sim 1 \times 10^{18}$ cm^{-3}) and window spacing (2.5 μm), 4H-SiC JBS diodes using FGRs termination have a reverse current density lower than 1×10^{-3} A/cm^2 below 100 V.

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