PDSOI DTMOS for analog and RF application*

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Abstract: Based on the platform of 0.35 μm PDSOI CMOS process technology, the partially depleted silicon-on-insulator dynamic threshold voltage (PDSOI DT) NMOS with an H-gate was implemented. The analog characteristics and RF characteristics of the gate-body contacted dynamic threshold voltage H-gate NMOS and conventional H-gate NMOS were performed and compared. Furthermore, the fundamental operation principle and physical mechanism of the PDSOI H-gate DTMOS compared with the conventional H-gate NMOS are analyzed in detail. The results indicate that the cutoff frequency can reach 40 GHz and the maximum oscillation frequency 29.43 GHz as $V_{gs} = 0.7$ V and $V_{ds} = 1$ V.

Key words: silicon-on-insulator; dynamic threshold voltage; analog and RF characteristics
DOI: 10.1088/1674-4926/32/5/054004 **EEACC:** 2560

1. Introduction

Over the past few years, SOI technology has become more and more popular for low power applications[1]. With the scaling down of the CMOS technology, the supply voltage and threshold voltage are reduced accordingly in order to meet the requirements of breakdown voltage and speed. However, the reduced threshold voltage gives rise to an increase in off-state current, which consumes more power during off-state. So as to resolve this drawback, a gate-body contacted dynamic threshold voltage (DT) MOS was proposed for lower threshold voltages during on-state and higher threshold voltages during off-state, which can be widely used for high speed and low power applications[2, 3].

Based on the above reasons, DTMOS has a great advantage in the digital integrated circuits. Additionally, as transistors always work in the saturation region for analog and RF applications, the analog and RF characteristics of DTMOS in the saturation region are also attractive. Some research has been carried out to investigate the analog and RF characteristics of DTMOS[4−7], and various kinds of special process and added circuits are proposed to improve the high frequency characteristics[8−10]. The device characteristics between gate-body contacted dynamic threshold voltage H-gate NMOS and normal H-gate NMOS in a 0.35 μm process are compared in this paper, and a small signal model is proposed to analyze the difference in the analog and RF characteristics of these two types of H-gate NMOS.

2. Device structure and fabrication

Figure 1(a) shows a schematic cross section of our PDSOI DTMOS. The body is tied to the gate via AL and silicide interconnects. The 300 μm/0.35 μm DT NMOSFETs were fabricated by a 0.35 μm process on 150 mm unibond (smart cut) wafers from Soitec Corp. The material parameters are as follows: p(100), 13.5–22.5 Ω·cm, 290-nm-thick top silicon film, and 400-nm-thick BOX (buried oxide). The micrograph of the test chip is shown in Fig. 1(b). Figure 2 shows the layouts of gate-body contacted dynamic threshold voltage H-gate NMOS and normal H-gate NMOS. Here, the H-gate structure instead of the T-gate structure is adopted in order to reduce the parasitic resistor existing along the channel.

3. Analog characteristic

After the formation of the PDSOI DT NMOS and PDSOI conventional NMOS, electrical characterizations were carried out with a Keithley 4200SCS semiconductor characteristics system. Figure 3 presents the transfer characteristics of the PDSOI DT NMOS and PDSOI H-gate NMOS. Compared with the conventional PDSOI H-gate NMOS, we could see that the drain current of the PDSOI DT NMOS is still zero at a low drain voltage as the gate–source voltage is larger than 1.2 V, and the drain current increases more rapidly along with the increase in drain voltage. The saturation drain current of the DT NMOS can even reach 96.3 mA and 21.2 mA as the gate voltage is 1.5 V and 0.9 V, while the saturation drain current of the conventional NMOS can only reach 32 mA and 3.5 mA as the gate voltage is 1.5 V and 0.9 V. As we know, the PDSOI DT NMOS has two operation regions: the first one is controlled by a gate, and the other one is viewed as a bipolar device. The approximate equation of the drain current can be derived as follows,

$$I_d = I_{dmos} + I_{dbipolar} = k_n \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right] - A_E J_s\left[\exp(qV_{gd}/kT) - 1\right], \quad V_{gs} > V_{ds} + V_{th}, \quad (1)$$

* Project supported by the State Key Development Program for Basic Research of China (No. 2006CB3027-01).
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Received 3 November 2010, revised manuscript received 9 December 2010

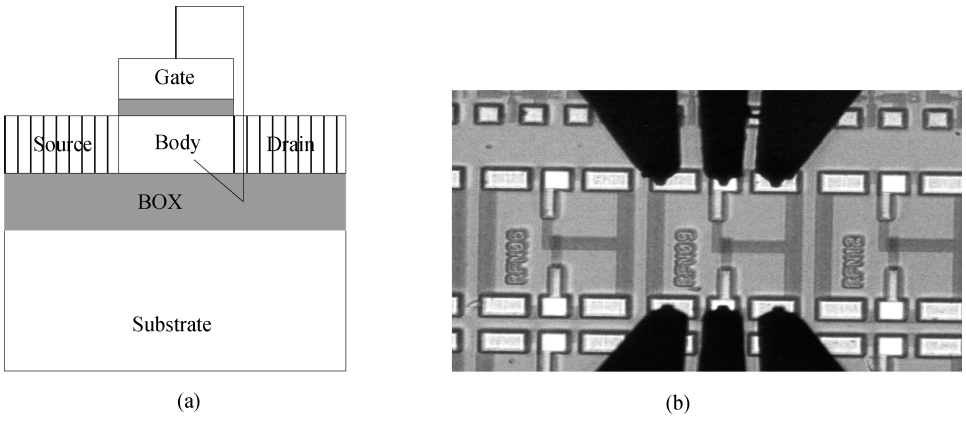

Fig. 1. (a) Schematic cross section of our PDSOI DTMOS. (b) Micrograph of the test chip.

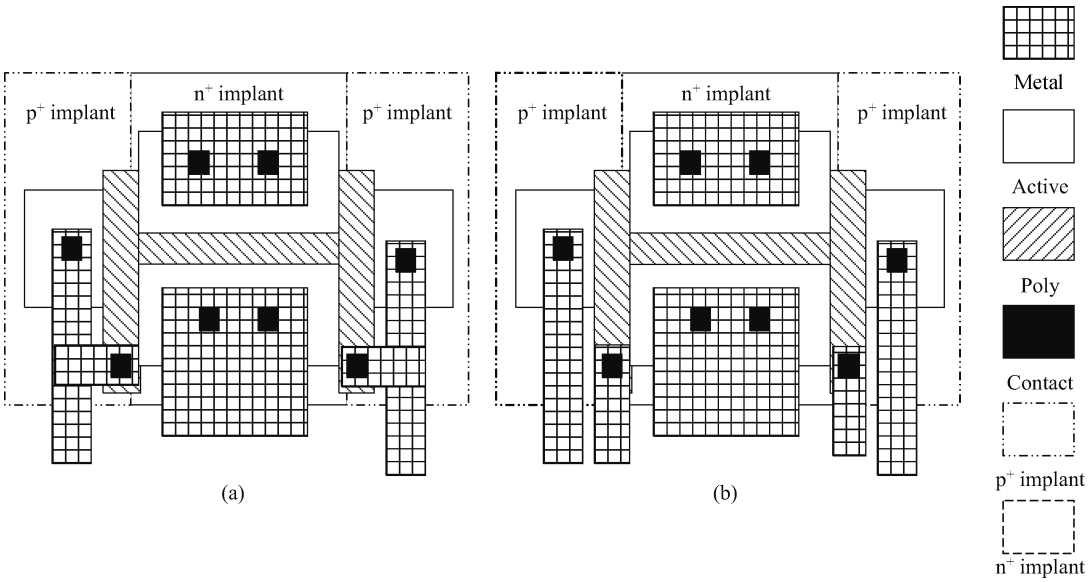

Fig. 2. Layouts of (a) a gate-body contacted dynamic threshold voltage H-gate NMOS and (b) a normal H-gate NMOS.

$$I_{\rm d} = I_{\rm dmos} + I_{\rm dbipolar} = \frac{k_{\rm n}}{2}\frac{W}{L}(V_{\rm gs} - V_{\rm th})^2 - A_{\rm E}J_{\rm s}\left[\exp(qV_{\rm gd}/kT) - 1\right], \quad V_{\rm ds} < V_{\rm gs} < V_{\rm ds} + V_{\rm th}, \tag{2}$$

$$I_{\rm d} = I_{\rm dmos} + I_{\rm dbipolar} = \frac{k_{\rm n}}{2}\frac{W}{L}(V_{\rm gs} - V_{\rm th})^2 + A_{\rm E}J_0\exp(qV_{\rm gs}/kT), \quad V_{\rm th} < V_{\rm gs} < V_{\rm ds}. \tag{3}$$

As the gate (body) voltage is higher than $V_{\rm ds} + V_{\rm th}$, the MOS part works in the linear region, and the bipolar part is only acted as two diodes (body-source diode and body-drain diode). The drain current is approximately supposed as Eq. (1), and the drain current due to MOS is compensated by the one due to the body-drain diode current, which can explain that the drain current with a higher gate voltage is marginally zero as the drain voltage is small. As the gate voltage is between $V_{\rm ds} + V_{\rm th}$ and $V_{\rm ds}$, the MOS part enters into saturation region, and the bipolar part still acts as two diodes, so the drain current is similarly considered as Eq. (2). However, as the gate voltage is lower than $V_{\rm ds}$, the bipolar part gradually comes to work as a bipolar device, and the drain current is thought of as the sum of MOS drain current and the collector current of the bipolar device. In addition, the threshold voltage is smaller because of the body effect, so the drain current shown in Fig. 3(a) is much higher than that in Fig. 3(b). We could see that the drain current of the DT NMOS can even reach to 21.3 mA as the gate voltage is 0.9 V and the drain voltage is 1 V, while the drain current of the conventional NMOS can only reach 3.4 mA as the gate voltage is 0.9 V and the drain voltage is 1 V.

Figure 4 presents the drain current and transconductance of the PDSOI DT NMOS and the PDSOI H-gate NMOS. Compared with the conventional PDSOI H-gate NMOS, the drain current increases more rapidly along with the increase in gate voltage, and the transconductance also rises and falls faster. The approximate equation of transconductance derived from Eqs. (1)–(3) is as follows,

$$g_{\rm m} \approx k_{\rm n}\frac{W}{L}V_{\rm ds} - (q/kT)A_{\rm E}J_{\rm s}\exp(qV_{\rm gd}/kT), \quad V_{\rm gs} > V_{\rm ds} + V_{\rm th}, \tag{4}$$

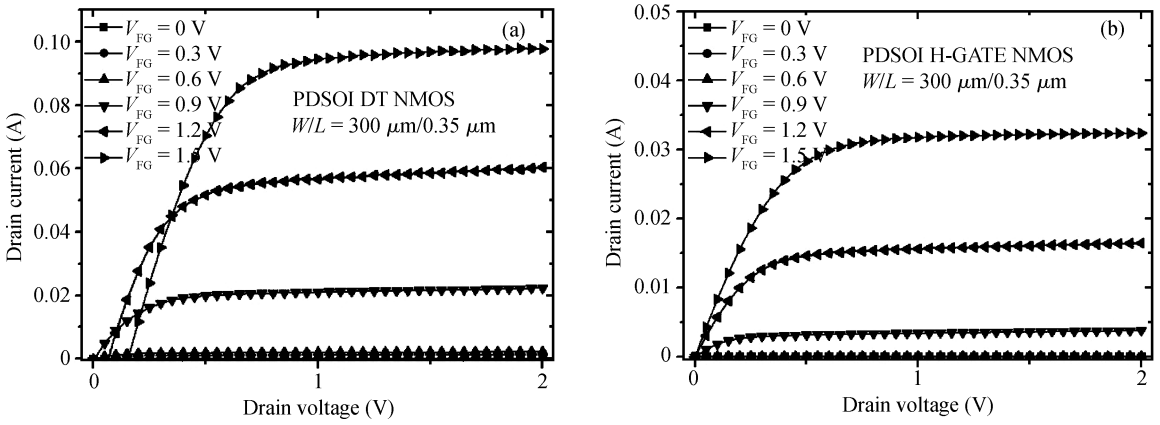

Fig. 3. I_d versus drain voltage for (a) a PDSOI DT NMOS and (b) a PDSOI H-GATE NMOS.

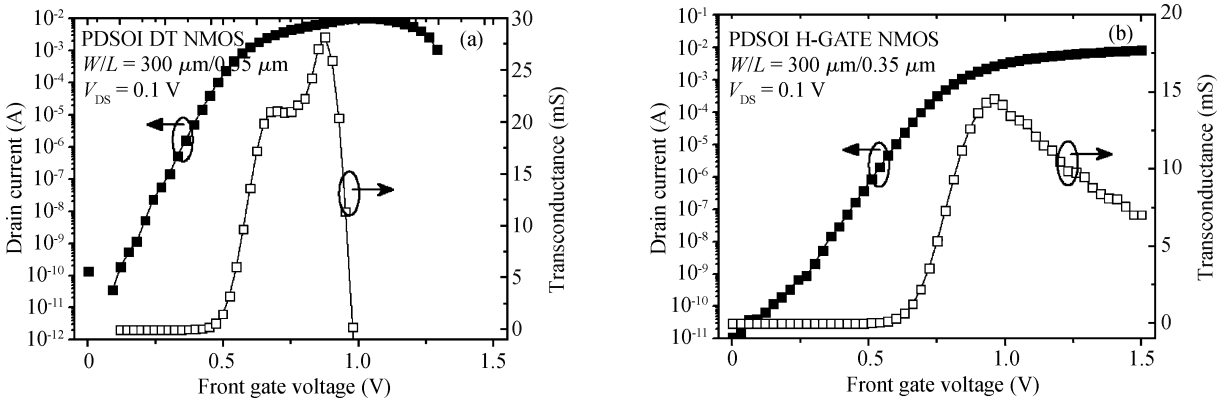

Fig. 4. Drain current and transconductance versus gate voltage of (a) the PDSOI DT NMOS and (b) the PDSOI H-gate NMOS.

$$g_m \approx k_n \frac{W}{L}\left(V_{gs} - V_{th}\right) - (q/kT)A_E J_s \exp(qV_{gd}/kT), \quad V_{ds} < V_{gs} < V_{ds} + V_{th}, \quad (5)$$

$$g_m \approx k_n \frac{W}{L}\left(V_{gs} - V_{th}\right) + (q/kT)A_E J_0 \exp(qV_{gs}/kT), \quad V_{th} < V_{gs} < V_{ds}. \quad (6)$$

We can find that before the gate voltage is lower than the threshold voltage, the MOS part and bipolar device part are in the cut off region, and the transconductance remains at zero. As the gate voltage is higher than the threshold voltage, the MOS part enters into the saturation region, and the bipolar device part starts to work, so g_m increases more rapidly, as illustrated in two terms of Eq. (6), and finally reaches 28.2 mS as the gate voltage is 0.9 V, which only reaches 14.7 mS as the gate voltage is 0.96 V in the conventional PDSOI NMOS case. As the gate voltage is between the drain voltage and the sum of the drain voltage and the threshold voltage, the MOS part is still in the saturation region, and the bipolar device part begins to work as two diodes. We can see that the first term of Eq. (5) increases and the second term of Eq. (5) is reduced, so the increase in transconductance slows down and reaches a maximal value in the end. Compared with the conventional PDSOI NMOS, as the gate voltage becomes larger than the sum

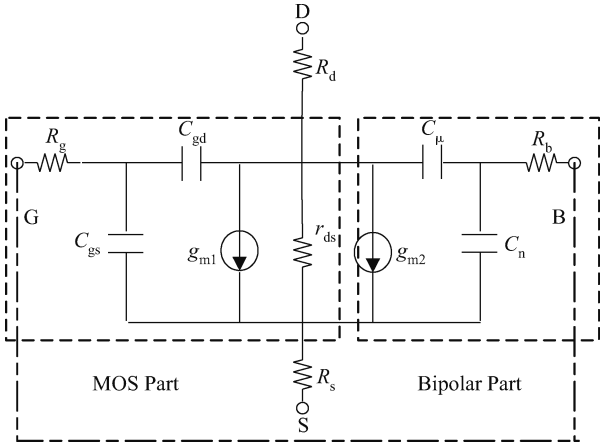

Fig. 5. Simplified small signal model of the DT NMOS.

of the drain voltage and the threshold voltage, the first term of Eq. (4) holds the line, and the second term of Eq. (5) is reduced. By the way, the first term of Eq. (4) is approximate and reduced slowly because the effect of negative differential mobility and the transconductance of DTMOS is reduced more steeply than the conventional H-gate NMOS because of the item $-(q/kT)A_E J_s \exp(qV_{gd}/kT)$ in Eq. (4). As a result, the transconductance of the DTMOS falls rapidly to zero as the gate voltage is about 1 V, while the transconductance of the

DTMOS is still 7 mS as the gate voltage reaches 1.5 V, which should be considered seriously in the analog application.

4. RF characteristic

Figure 5 shows a simplified small signal model of the DT NMOS as both the MOS part and the bipolar device part work, in which g_{m1} represents the transconductance of the MOS part and g_{m2} represents the transconductance of the bipolar device part. We can derive a simplified cutoff frequency by neglecting the parasitical resistor in Eq. (7), and the maximum oscillation frequency of the MOS part and the bipolar device part are respectively derived considering the parasitical resistor and the parasitical capacitance in Eqs. (8) and (9),

$$f_{\mathrm{T}} = \frac{i_{\mathrm{drain}}}{i_{\mathrm{gate}}} = \frac{g_{\mathrm{m1}} + g_{\mathrm{m2}}}{2\pi(C_{\mathrm{gs}} + C_{\mathrm{gd}} + C_{\mu} + C_{\pi})} \propto g_{\mathrm{m}}, \quad (7)$$

$$f_{\max} = \frac{f_{\mathrm{T}}}{2\sqrt{\dfrac{g_{\mathrm{ds}}}{g_{\mathrm{m}}}\dfrac{V_{\mathrm{ds}}}{V_{\mathrm{gs}} - V_{\mathrm{th}}}}} \propto f_{\mathrm{T}}, \quad (8)$$

$$f_{\max} = \left(\frac{f_{\mathrm{T}}}{8\pi r_{\mathrm{b}} C_{\mathrm{dBC}}}\right)^{1/2} \propto f_{\mathrm{T}}^{1/2}. \quad (9)$$

The RF characteristics were carried out with the vector network analyzer HP 8510C. As discussed in the last section, the transconductance of the DTMOS is reduced steeply as the gate voltage is larger than the sum of the drain voltage and the threshold voltage, so we make the maximal value of the gate voltage 1 V for testing. Figures 6 and 7 show the curves of the current gain H_{21} and the power gain $G_{\max}$ versus the frequency. As the gate voltage is 0.3 V, the DTMOS is cut off, and the current gain H_{21} and power gain $G_{\max}$ are even negative and almost hold the line, because the current flow into gate (body) node from the drain node via the back biased diode and the body-source diode is shut down. Before V_{gs} reaches about 0.7 V and g_{m} reaches almost the maximal value proved in Fig. 4(a), we can see that the cutoff frequency is increasing along with the increase in gate voltage, because f_{T} is directly proportional to g_{m} in Eq. (7). As V_{gs} is larger than the sum of the drain voltage and threshold voltage, the transconductance of the DTMOS is reduced steeply as proved in Eq. (4) and the curve of current gain H_{21} is moved down due to the relationship of direct proportion between the transconductance and the cutoff frequency. As shown in Fig. 7, the maximum oscillation frequency behaves similarly to the cutoff frequency because of the relationship of direct proportion between the maximum oscillation frequency and the cutoff frequency according to Eqs. (8) and (9).

As shown in Figs. 6 and 7, we can see that the cutoff frequency can reach 40 GHz and the maximum oscillation frequency can reach 29.43 GHz as the gate voltage is 0.7 V.

5. Conclusion

A partially depleted silicon-on-insulator dynamic threshold voltage NMOS with an H-gate is proposed in this paper.

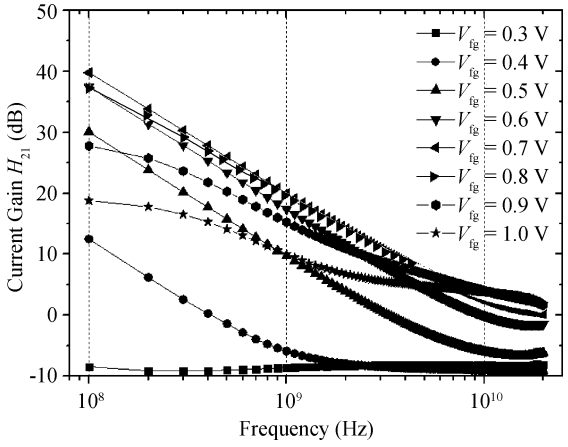

Fig. 6. Current gain versus frequency.

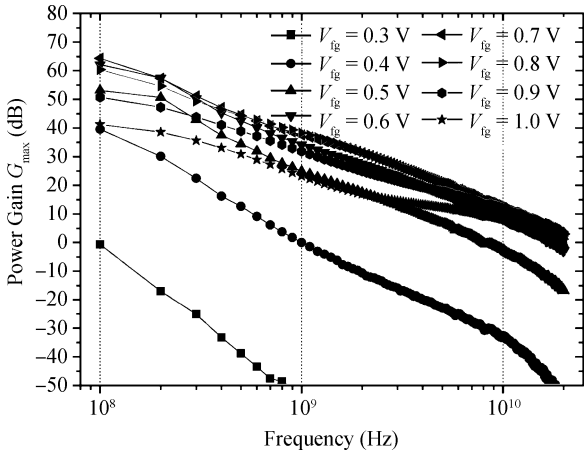

Fig. 7. Power gain versus frequency.

We make a comparative study of a gate-body contacted dynamic threshold voltage H-gate NMOS and a conventional H-gate NMOS in a 0.35 μm PDSOI process for analog and RF application. According to our experimental results, we analyze the physical generation mechanism of the difference in analog and RF characteristic of the PDSOI DTMOS and the normal H-gate NMOS, and obtain a cutoff frequency of 40 GHz and a maximum oscillation frequency of 29.43 GHz when $V_{\mathrm{gs}} = 0.7$ V and $V_{\mathrm{ds}} = 1$ V. In future work, we will try to improve the gate-body contacted method, and especially shorten the distance of the gate contact and body contact via new process technology, and try to introduce an added transistor to resolve the problem of the power supply voltage limitation.

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