Improving the quality factor of an RF spiral inductor with non-uniform metal width and non-uniform coil spacing*

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Abstract: An improved inductor layout with non-uniform metal width and non-uniform spacing is proposed to increase the quality factor (Q factor). For this inductor layout, from outer coil to inner coil, the metal width is reduced by an arithmetic-progression step, while the metal spacing is increased by a geometric-progression step. An improved layout with variable width and changed spacing is of benefit to the Q factor of RF spiral inductor improvement (approximately 42.86%), mainly due to the suppression of eddy-current loss by weakening the current crowding effect in the center of the spiral inductor. In order to increase the Q factor further, for the novel inductor, a patterned ground shield is used with optimized layout together. The results indicate that, in the range of 0.5 to 16 GHz, the Q factor of the novel inductor is at an optimum, which improves by 67% more than conventional inductors with uniform geometry dimensions (equal width and equal spacing), is enhanced by nearly 23% more than a PGS inductor with uniform geometry dimensions, and improves by almost 20% more than an inductor with an improved layout.

Key words: inductor layout optimization; variable metal width and spacing; integrated RF inductor; silicon substrate

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1. Introduction

In the development of silicon radio frequency integrated circuits (RFICs), the on-chip inductor is a key component to achieve the required circuits, such as a low noise amplifier, voltage controlled oscillator, and mixers. High quality (Q) performance of the inductor is also crucial for the phase noise performance of RFICs.

A high-Q inductor is a paramount component in RF circuit design. However, the Q factor degenerates due to integration substrate losses and strip metal losses[1,2]. In order to reduce substrate losses, the patterned ground shield (PGS) technique[3] is adopted, since it prevents capacitive coupling to the lo substrate. Metal losses include the skin effect with different wire widths[4] and eddy currents[5−7]. In order to reduce the metal losses, an optimized layout of the spiral inductor is proposed. Craninvkx and Steyaert[8] proposed that the inner turn of the spiral metal coil should be narrower than the outer turn. Hsu[6] reported that, for a broadened spiral inductor with a larger step width between two coils, the eddy-current loss is reduced more due to the inner metal width of the inner turns reducing noticeably.

However, such a stacked spiral coil structure with a gradually broadened width provides an increased chip area (for the uniform spacing between two coils). In addition, the electric field density is increased from the outside metal coil to the inside metal coil, and the density of the spiral in the center reaches the largest. The Q factor of the broadened inductor improves slightly, especially at high frequency, due to the eddy current loss caused by the current crowding effect.

Here, non-uniform spacing is adopted with a broadened metal width together for the optimized inductor layout. The result indicates that the novel spiral inductor with arithmetic-progression step widths and geometric-progression step spacing can improve the Q factor without chip area increment. In order to reach the maximum Q factor, for the novel inductor, a PGS structure is used on the substrate with an optimized layout together. Compared to the standard spiral inductor, a remarkable improvement in the Q factor is achieved for the novel inductor, which is as high as 67%.

2. Description of the layout optimization method

2.1. Coil spacing

The performance of an inductor is mainly determined by its Q factor. This is defined as the ratio of the energy stored to the total dissipation per cycle for a sinusoidal excitation[9],

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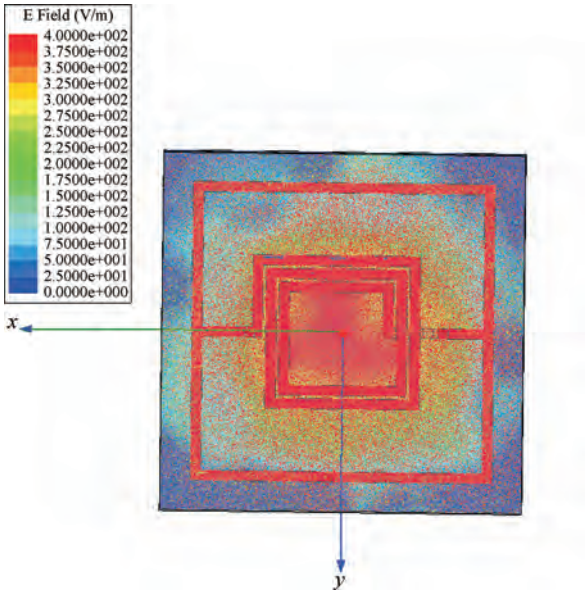

Fig. 1. Vector electric field distribution plot of the standard inductor with uniform width and uniform spacing.

$$Q = 2\pi \frac{\text{energy stored}}{\text{energy lost per cycle}} = 2\pi \frac{E_{\text{m, max}} - E_{\text{e, max}}}{E_{\text{per}}}, \quad (1)$$

where $E_{\text{m, max}}$ is the maximum value of magnetic energy, $E_{\text{e, max}}$ is the maximum value of electric energy, and E_{per} is the average power loss. From Eq. (1), the high Q factor can be directly related to $E_{\text{e,max}}$ shrinkage since $E_{\text{m, max}}$ and E_{per} keep stable.

Figure 1 is the vector electric filed distribution plot of the standard inductor with uniform width and uniform spacing, which is simulated by a high frequency structure simulator (HFSS). The density is increased from the outside metal coil to the inside metal coil, and the density of the spiral in the center is the largest. In the inner turn of the spiral, the largest electric field density causes non-uniform current distribution. This current crowding effect is due to induced eddy currents on adjacent strips in the inner turns, which results in an increment of $E_{\text{e, max}}$, thus degrading the Q factor and inductance[10].

Therefore, the electric density in the center should be reduced. Large coil spacing can be helpful to achieve a low electric density. Figure 2 shows the Q factors of the inductors versus the frequency of different coil spacings, which is simulated by using advanced design system (ADS). Other physical dimensions of these four spiral inductors are kept the same, such as the metal thickness, metal width, and dielectric thickness between the coil and the substrate. From Fig. 2, it can be seen that a concomitant increment in Q factor is from 12 to 18, when the spacing increases from 5 to 20 μm.

From Fig. 1, the density of the centre electric field is high, but the density of the border region electric field is low. Therefore, non-uniform coil spacing is adopted for the optimized layout of the spiral inductor. From the outer winding coil to the inner winding coil, the metal coil spacing gradually increases

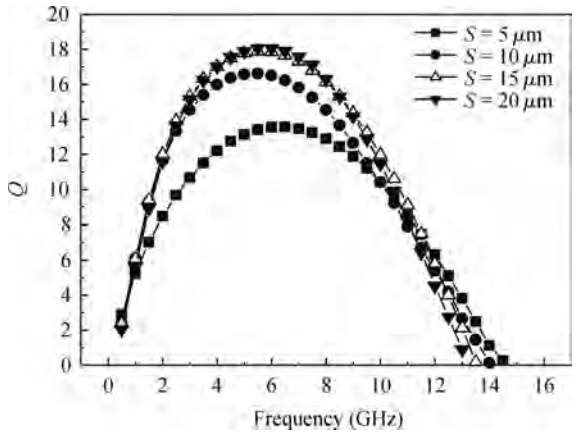

Fig. 2. Q factors of the inductors versus frequency for different coil spaces.

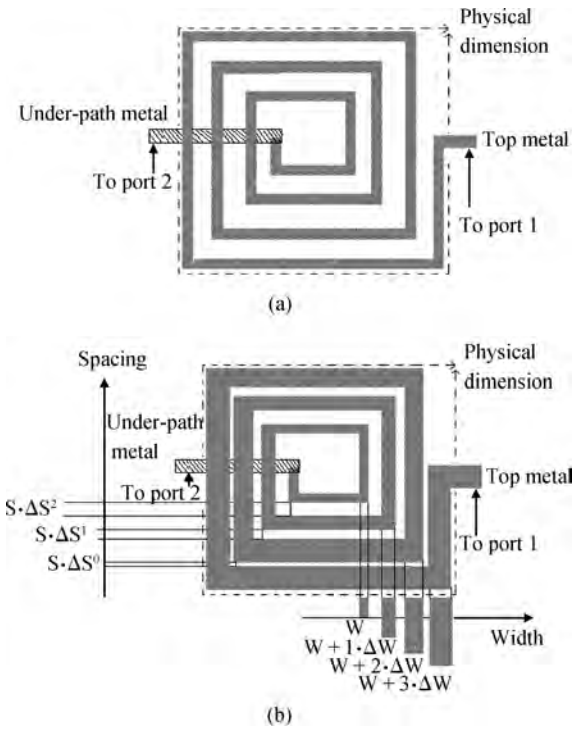

Fig. 3. Top-view schematic diagrams of (a) a 3.5-turn standard spiral inductor and (b) a 3.5-turn spiral inductor with optimized layout, which includes non-uniform metal width and non-uniform coil spacing.

by a geometric-progression step, in order to weaken the current crowding effect in the centre and the skin effect in the adjacent metal strips.

2.2. Optimized layout for spiral inductor

Figure 3 shows both the 3.5-turn standard and the spiral inductor with optimized layout. The top view of the standard inductor with equal metal width of 10 μm and equal coil spacing of 15 μm is shown in Fig. 3(a). Figure 3(b) shows the inductor with optimized layout, which includes non-uniform metal width and non-uniform coil spacing. The first inner turn of the metal is used as the reference turn, with metal width of 5 μm.

The outer turns are increased by an arithmetic-progression step width ($\triangle W$) from the reference metal. From the inner coil to the outer coil, the spacing between the third coil and fourth coil is used as reference spacing, and it equals 2.5 μm. The spacing is increased by a geometric-progression step ($\triangle S$). The metal width W_n and spacing S_n in the inner coil are described as

$$W_n = W + n\Delta W, \tag{2}$$

$$S_n = S(\Delta S)^n. \tag{3}$$

According to the equivalent method of a single π model used in Ref. [11], for this novel inductor with optimized layout, $E_{\mathrm{m,\,max}}$, $E_{\mathrm{e,\,max}}$, and E_{per} can be given by

$$E_{\mathrm{m,\,max}} = \frac{1}{2}LI^2 = \frac{V_{\mathrm{O}}^2 L_{\mathrm{S}}}{2[(wL_n)^2 + R_{\mathrm{S}}^2]}, \tag{4}$$

$$E_{\mathrm{e,\,max}} = \frac{V_{\mathrm{O}}^2(C_{\mathrm{S}} + C_{\mathrm{P}})}{2}, \tag{5}$$

$$E_{\mathrm{per}} = \frac{\pi V_{\mathrm{O}}^2}{w}\left[\frac{1}{R_{\mathrm{P}}} + \frac{R_{\mathrm{S}}}{(wL_{\mathrm{S}})^2 + R_{\mathrm{S}}^2}\right], \tag{6}$$

where w is the frequency, V_{O} is the drive voltage, L_{S} represents the series inductance of the inductor coil, C_{S} is the series capacitance of the inductor coil, C_{P} is the parallel plate capacitance, R_{P} is the parallel plate resistance, and R_{S} is the series resistance of the inductor coil mainly due to conductor losses. R_{S} is a frequency dependent element that accounts for the edge, proximity, and skin effect[12] on the current flow. Induced eddy currents are attributed to the proximately effect[13]. For this case, R_{S} can be written as

$$R_{\mathrm{S}} = \sum_{n=1}^{N}\left[\frac{r_{\mathrm{s}}(f)}{W_n} + Cg_n^2 f^2 W_n^2\right] l_n, \tag{7}$$

where $r_{\mathrm{s}}(f)$ is the sheet resistance of the metal strip, f is the frequency, and C is the constant that can be obtained by fitting the experimental or simulated results. For C in the case of a constant strip width inductor, Equation (7) has a minimum for a width W_{opt} given by

$$W_{\mathrm{opt}} = \sqrt[3]{\frac{r_{\mathrm{s}}(f)}{2kf^2}}, \tag{8}$$

with

$$k = C\frac{\sum_{n=1}^{N} g_n^2 l_n}{\sum_{n=1}^{N} l_n}, \tag{9}$$

where g_n is a function dependent only on geometrical parameters and l_n is the length of the nth turn of the coil. For a given inductor geometry and operation frequency, by comparing the experimental or simulated optima width W_{opt}, k can be obtained. Then using Eq. (9), we obtain C. Finally, once the fitting parameter C is known, then the set of optima strip-width values by minimizing R_{S} can be obtained of n variable W_n ($n = 1, \cdots, N$).

g_n depends on geometrical parameters such as (1) the number of turns N; (2) the length of the first turn of the coil l_1; (3) the metal strip width w_n; and (4) the turn to turn spacing s_n. The inductor geometry can easily be considered using the correct expression for g_n function. Actually, g_n can be written as

$$g_n = \frac{B_n}{I}, \tag{10}$$

where B_n is the magnetic field, which consists of three parts, as follows,

$$B_n = B_{n,n} + B_{n,\,\mathrm{in}} + B_{n,\,\mathrm{out}}, \tag{11}$$

where $B_{n,n}$ is the magnetic field at turn n generated by itself, $B_{n,\,\mathrm{in}}$ is the magnetic field at turn n generated by the inner turns, and $B_{n,\,\mathrm{out}}$ is the magnetic field at turn n generated by the outer turn. The detailed expressions for the magnetic fields ($B_{n,n}$, $B_{n,\,\mathrm{in}}$ and $B_{n,\,\mathrm{out}}$) are shown in Ref. [4]. There exit an important factor for magnetic fields is d_n, which can be written as

$$d_n = \frac{l_n}{8}. \tag{12}$$

In the case of a square spiral, l_n can be expressed as

$$l_n = l_{n-1} + s_{n-1} + 6s_n + s_{n+1} + \frac{7W_{n-1} + 9W_n}{2}, \tag{13}$$

where s_{n-1} is the spacing between turns n and $n-1$.

Substituting Eqs. (4)–(6) into Eq. (1), the Q factor of the spiral inductor with non-uniform width and non-uniform spacing is expressed as

$$Q = \frac{wL_{\mathrm{S}}}{R_{\mathrm{S}}}\frac{R_{\mathrm{p}}}{R_{\mathrm{p}} + [(wL_{\mathrm{S}}/R_{\mathrm{S}})^2 + 1]R_{\mathrm{S}}} \times\left[1 - (C_{\mathrm{S}} + C_{\mathrm{P}})\left(\frac{R_{\mathrm{S}}^2}{L_{\mathrm{S}}} + w^2 L_{\mathrm{S}}\right)\right]. \tag{14}$$

The inductance of the spiral inductor can be written as

$$L = \sum_{n=1}^{N}(L_n + M_n), \tag{15}$$

where L_n is the inductance of the nth unit metal strip inductor, and M_n is the coupling inductance between the nth unit metal strip inductor and the $(n+1)$th unit metal strip inductor. They can be expressed as

$$L_n = 0.002l_n\left[\ln\frac{2l_n}{a+b} + 0.025049 + \frac{a+b}{3l_n} + \frac{\sigma T}{4}\right], \tag{16}$$

$$M_n = 2l_n q, \tag{17}$$

where a and b are the width and length of the cross section of the nth unit rectangle inductor, and σ is the magnetic permeability of the vacuum. Therefore, we propose an iterative method to optimize the inductor layout to reach the maximum Q factor at a given frequency. The main calculation steps are as follows.

(1) An initial set of strip width values are defined, i.e., the same strip width values for all turns.

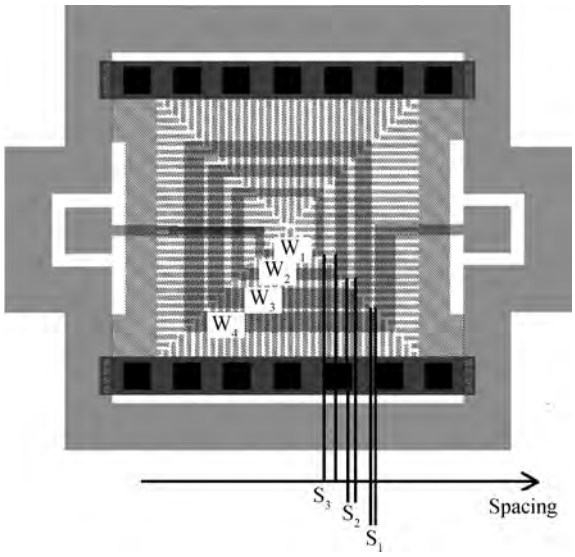

Fig. 4. Layout of the novel spiral inductor with non-uniform width and non-uniform spacing on a silicon substrate.

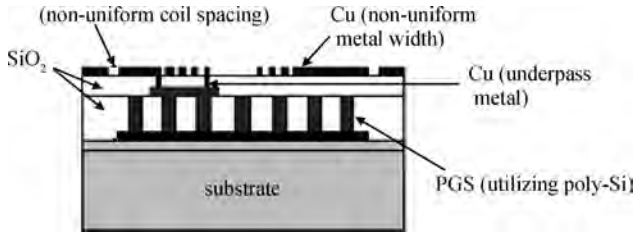

Fig. 5. Cross view of the novel spiral inductor with optimized layout on silicon substrate.

(2) Taking into account the strip width w_n, spacing value s_n and other geometric parameters defining the inductor layout, i.e., number of turns N, by using Eqs. (12) and (13).

(3) Using Eqs. (10) and (11), the values of g_n are obtained.

(4) Finally, the set of strip width w_n and spacing value s_n are updated using Eqs. (2), (3), (8) and (13).

(5) The progress stops here if the desired accuracy of w_n and s_n are reached. If not, the process is repeated from step (2).

(6) The quality factor Q and inductance L of this novel inductor can be determined by using Eqs. (14)–(17).

3. Results and discussion

By using 0.35 μm silicon CMOS technology, Figure 4 is the layout of the novel spiral inductor with non-uniform metal width and non-uniform spacing on a silicon substrate. In order to achieve the maximum Q factor, a PGS substrate is added for the novel spiral inductor, with non-uniform metal width and non-uniform coil spacing together. The first turn of the metal (M1) is used as the reference turn, and the metal width of the first turn is 5 μm. From the inner coil to the outer coil, the metal width increases by an arithmetic-progression step width ($\triangle W = 5$). Therefore, the widths of M1, M2, M3 and M4 are 5, 10, 15 and 20 μm, respectively. At the same time, the coil spacing decreases by an arithmetic-progression step width ($\triangle S = 2$). The spacing (S_1) between the M3 and M4 is the narrowest. The values of S_1, S_2 and S_3 are 2.5, 5 and 10 μm, respectively.

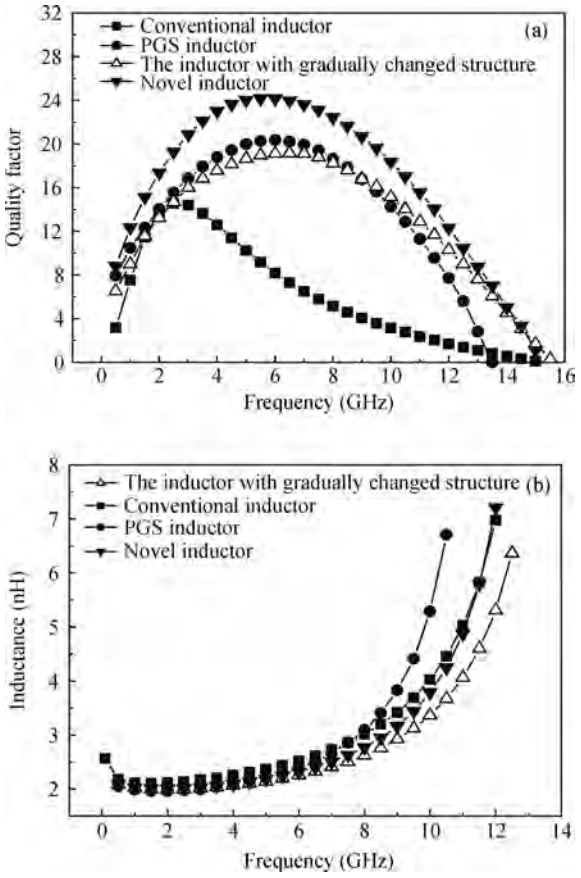

Fig. 6. Simulated results of Q factor and inductance versus frequency for the conventional inductor (uniform metal width of 15 μm and uniform coil spacing of 10 μm, without PGS), the PGS inductor (uniform metal width of 15 μm and uniform coil spacing of 10 μm, with PGS), the inductor with gradually changed structure (the widths of 5, 10, 15, 20 μm, and the spacing of 2.5, 5, 10 μm, without PGS), and novel inductor (with the gradually changed structure, with PGS).

Figure 5 depicts the cross section of the novel spiral inductor with an optimized layout. The inductor is on the high-resistivity silicon substrates with a thickness of 5.6 μm, and the substrate resistivity is 1 kΩ·cm. The underpass metal thickness is 0.5 μm, and the thickness of the metal coil is 1.9 μm. The sheet resistance is 40 mΩ. The dielectric thickness between the coil and the substrate is 0.2 μm.

Four kinds of inductors have been designed using 0.35 μm silicon CMOS technology. They include the conventional inductor (uniform metal width of 15 μm and uniform coil spacing of 10 μm, without PGS), the PGS inductor (uniform metal width of 15 μm and uniform coil spacing of 10 μm, with PGS), the inductor with gradually changed structure (the widths of 5, 10, 15, 20 μm, and the spacings of 2.5, 5, 10 μm, without PGS), and the novel inductor (with the same gradually changed structure, with PGS). The other dimensions of all of the inductors are kept the same, such as the metal thickness and substrate resistivity.

Figure 6(a) shows the Q factor versus the frequency for these four inductors. Comparing the inductor with gradually changed structure with the conventional inductor, in the range from 0 to 16 GHz, the maximum value of the Q factor can

be improved by 42.86% without PGS. The results indicate that the optimal layout with non-uniform spacing is indeed helpful for increment of the Q factor. Among these four inductors, the novel inductor achieves an optimal Q factor. The value of the novel inductor is 8 at 0.5 GHz, then increases with frequency and reaches the peak at 6 GHz, which is as high as 24. Compared with the other three inductors, the maximum value of the Q factor improves by 67% more than the conventional inductor, improves by nearly 23% more than the PGS inductor, and improves by 20% more than the inductor with gradually changed structure.

The corresponding inductances of these four inductors are shown in Fig. 6(b). The inductances are kept almost the same in the operation range. This is helpful for the design of low power consumption and high performance radio frequency integrated circuits.

4. Conclusion

An improved layout of the inductor has proposed in this paper, which includes a variable metal width based on the arithmetic-progression format and a variable coil spacing based on the geometric-progression format. For the inductor with improved layout, Q factor improvement is mainly due to the suppression of eddy current loss, by weakening the current crowding effect in the centre. In order to reach the maximum Q factor, for the novel inductor, the PGS structure is used on the substrate with optimized layout together. The novel inductor achieves the optimum Q factor among four inductors, within an inductance variation of 5%, which can eventually assist in RFIC design.

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