A low noise high efficiency buck DC–DC converter with sigma–delta modulation*

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Abstract: Some research efforts to improve the efficiency and noise performance of buck DC–DC converters are explored. A carefully designed power MOSFET driver, including a dead time controller, discontinuous current mode (DCM) controller and gate width controller, is proposed to improve efficiency. Instead of PWM modulation, sigma–delta modulation is introduced into the feedback loop of the converter to move out the clock-referred harmonic spike. The proposed converter has been designed and fabricated by a 0.35 μm CMOS process. Measured results show that the peak efficiency of the converter can reach 93% and sigma–delta modulation suppresses the harmonic spike by 30 dB over PWM modulation.

Key words: buck DC–DC converter; PWM modulation; sigma–delta modulation; DCM; dead time control; width control; current sensing

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1. Introduction

Battery-operated portable electrical equipment must be efficient, small and low cost. This cannot function without the support of a high-performance power supply. Switching-mode power supplies (SMPSs) can offer efficient power conversion and reliable voltage regulation even with widely varying input voltage and/or load. This makes SMPSs become an essential part of portable equipment. In order to maximize the battery life, it is absolutely necessary that intensive research efforts to improve the efficiency of SMPSs are explored in the design process. Another potential drawback and growing concern about conventional SMPSs is their spectral characteristics. In conventional SMPSs, pulse width modulation (PWM) is implemented to generate a control signal that has a fixed frequency and varying duty cycle. The signal contains many clock-referred harmonic spikes, which can couple into the supply and ground lines via the substrate, degrading the performance of the sensitive mixed signal and RF circuits on the same die. These harmful spikes are highly undesirable in noise-sensitive applications, such as wireless communication systems. A spectrally quiet SMPS can be obtained by using low-noise modulation techniques, instead of PWM. Sigma–delta modulation is an alternative approach[1].

This paper presents a low noise, high efficiency buck DC–DC converter with second-order sigma–delta modulation. The proposed power MOSFET driver includes a dead time controller, DCM controller and gate width controller. In a dead time controller, a novel auto-adaptive circuit based on a charge-pump is proposed. In a width controller, the current-sensing circuit is improved. A traditional current-sensing circuit samples the peak current of the power MOSFET. It requires the switching signal of the power MOSFET to have a fixed duty cycle. Because of the different modulation method, the duty cycle varies. This makes it impossible to sample the peak current. A novel current-sensing method, sampling averaging current, is proposed to resolve this problem. As to reducing noise, a second-order, continuous-time modulator is designed, and the current feedback method is improved. The improvement reduces the power consumption of the OTA and enhances the performance of the modulator.

2. Proposed buck DC–DC converter

The buck converter draws power from an external DC supply (i.e. battery) discontinuously and supplies it to the load continuously with a lower voltage level. Figure 1 shows the system level bock diagram of the proposed buck DC–DC converter. It contains two main parts: a power conversion circuit and a feedback control circuit. The power conversion circuit includes power MOSFET switches, gate drive buffers, a high-efficiency power MOSFET driver and two off-chip components (inductor, capacitor). The feedback control circuit includes a type-III frequency compensator and a second-order continuous-time sigma–delta modulator.

Although the converter is lossless theoretically, the non-idealities in practical implementation consume power when the converter works. In contrast to a feedback control circuit, a power conversion circuit caused most of the power loss. This is because the power conversion circuit has most of the gate area, in other words, most of the parasitic capacitance. And, it always works under the highest frequency, being the same with clock frequency and full swing, from supply to ground. As a result, the efficiency of the converter is determined by the power conversion circuit. Briefly, the power loss in the conversion circuit mainly includes gate-drive loss, conduction loss, switching loss, and body-diode conduction loss[2]. A high-efficiency power MOSFET driver is developed to reduce them. The dead-time controller generates an overlap of off-state for n-type and p-type power MOSFETs to prevent shoot-though current. The NMOS dead-time controller can also automatically adjust dead-time, according to the load condition. This feature makes

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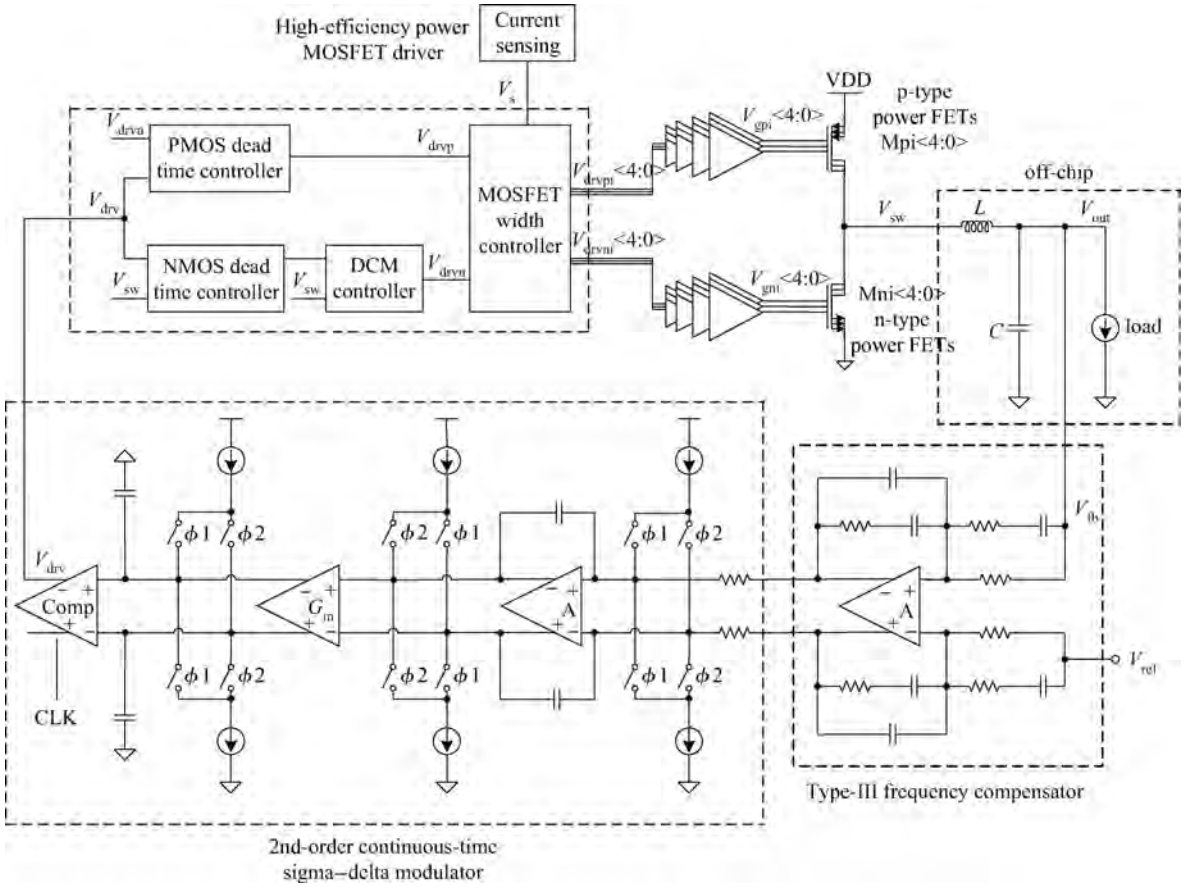

Fig. 1. Block diagram of the proposed buck DC–DC converter.

it possible to switch on an n-type MOSFET at the moment of the voltage V_{sw} falling to zero, which can avoid body-diode conduction loss, due to too long dead time or switching loss, due to too short dead time. The conduction loss is inversely proportional to the size of the power MOSFETs, while the gate-drive loss is directly proportional to it. The width controller can optimize the size of the power MOSFET, according to the load condition. When the converter supplies a light load, the inductor current may vary very much, and become negative at some point. This reverse current discharges the capacitor, and reduces the power efficiency. The DCM controller switches off the N-type MOSFET when the inductor current falls to zero, which can improve the light load efficiency of the converter.

Conventional pulse width modulation varies its duty cycle to control the ratio of the on-state and off-state of the power MOSFETs and adjust the output voltage level of the converter. Although PWM is a simple and reliable modulation scheme, it is not spectrally quiet. The noise characteristics of PWM modulation are shown in Fig. 2. The noise characteristics of the converter with PWM modulation are shown in Fig. 3.

As shown in Fig. 4(a), the sigma–delta modulator contains three blocks. They are the subtract block (delta), the integrator block (sigma) and the quantizer. The modulator uses a high gain loop to digitize the input signal x. The gain A is almost contributed by the integrator block. A is very large in the low-frequency band and attenuates as the frequency arises. This means that the output of the modulator almost equals the input signal x in the low-frequency band and differs much with

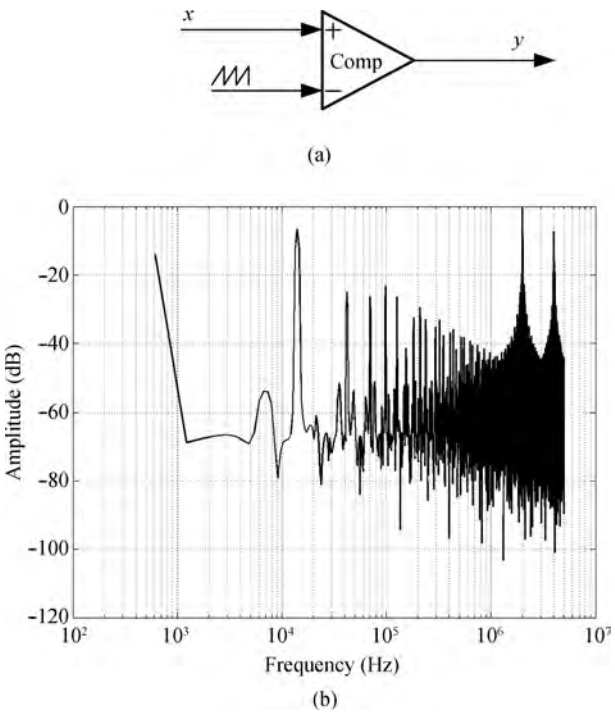

Fig. 2. PWM modulation. (a) Diagram of modulator. (b) Output spectrum for 14 kHz-sine input.

it in the high-frequency band. In the frequency domain, the un-

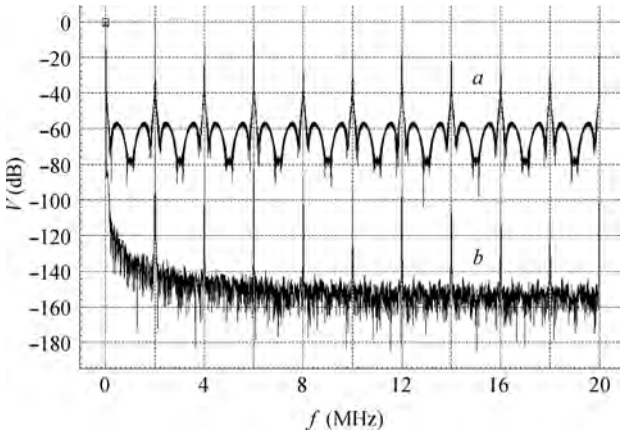

Fig. 3. Buck DC–DC with PWM modulation. (*a*) Spectrum of switch signal V_{drv} (upper). (*b*) Spectrum of output voltage of the converter.

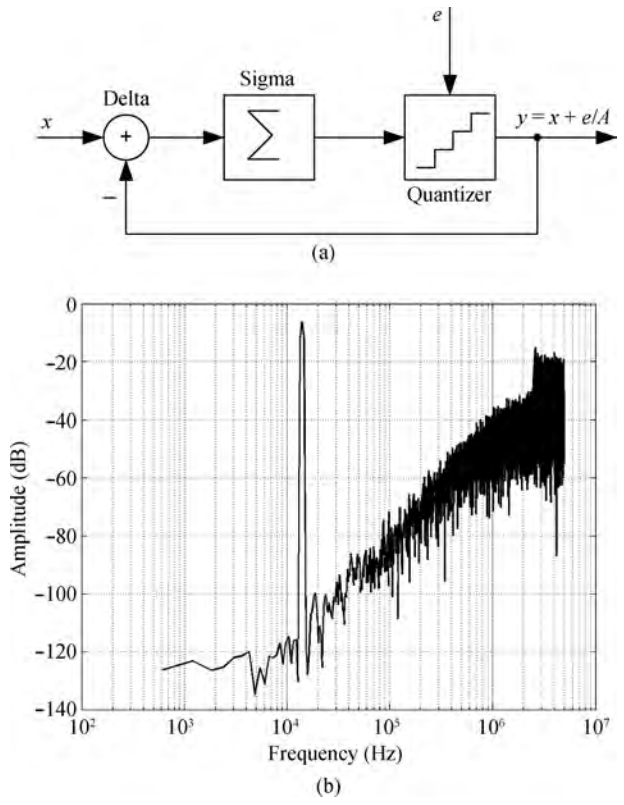

Fig. 4. Sigma–delta modulation. (a) Diagram of modulator. (b) Output spectrum for 14 kHz-sine input.

desired contents are moved out from the low-frequency band to the high-frequency band[3]. In the low-frequency band, the transfer function of the sigma–delta modulator is

$$y = \frac{A}{A+1}x + \frac{A}{A+1}e \approx x + \frac{1}{A}e, \qquad (1)$$

where e is quantization error. The noise-shaping effect can be seen from Fig. 4(b). The noise characteristics of the converter with sigma-delta modulation are shown in Fig. 5.

The feedback control circuit measures, amplifies and digitizes the difference between the output voltage of the converter and the reference voltage, to generate the control signal for the power MOSFET driver. The frequency compensator makes sure that the closed loop has enough phase margin to maintain the stability of the converter and enough DC gain to maintain the accuracy of the converter. Generally speaking, the driver contributes none to DC gain and phase shift of the loop. The power MOSFETs contribute none to DC gain and 180° phase shift of the loop. The off-chip inductor and capacitor contribute a small amount of DC gain, and a large phase shift of the loop. The output of the sigma–delta modulator almost equals the input of it in the low-frequency band, which means that the modulator contributes none to the DC gain and phase shift of the loop. Additional DC gain and phase margin are introduced into the loop of the converter by a type-III frequency compensator. A type-III frequency compensator contains high DC gain, which is up to 1000, and three poles and two zeroes, which can generate enough phase margin for the loop. The frequency characteristics of the main modules are shown in Fig. 6.

Fig. 5. Buck DC–DC with sigma–delta modulation. (*a*) Spectrum of switch signal V_{drv}. (*b*) Spectrum of output voltage of the converter.

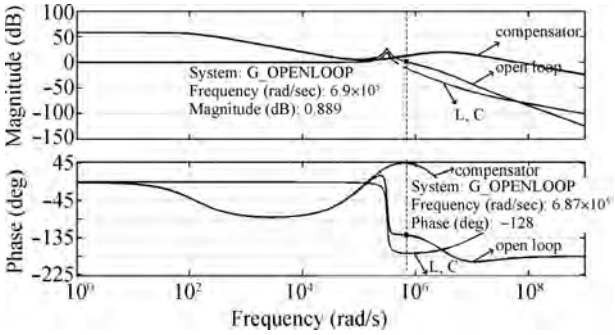

Fig. 6. Bode diagram of the converter loop.

3. Circuit design

3.1. Dead-time controller

As shown in Fig. 1, the driver consists of a dead time controller, a DCM controller and a width controller. A PMOS dead-time controller simply sets the opening time of the PMOS to the instant when the NMOS jumps off. The circuit implementation is shown in Fig. 7(a).

The dead-time controller for N-type power MOSFETs is much more complicated. As the optimal dead time varies with

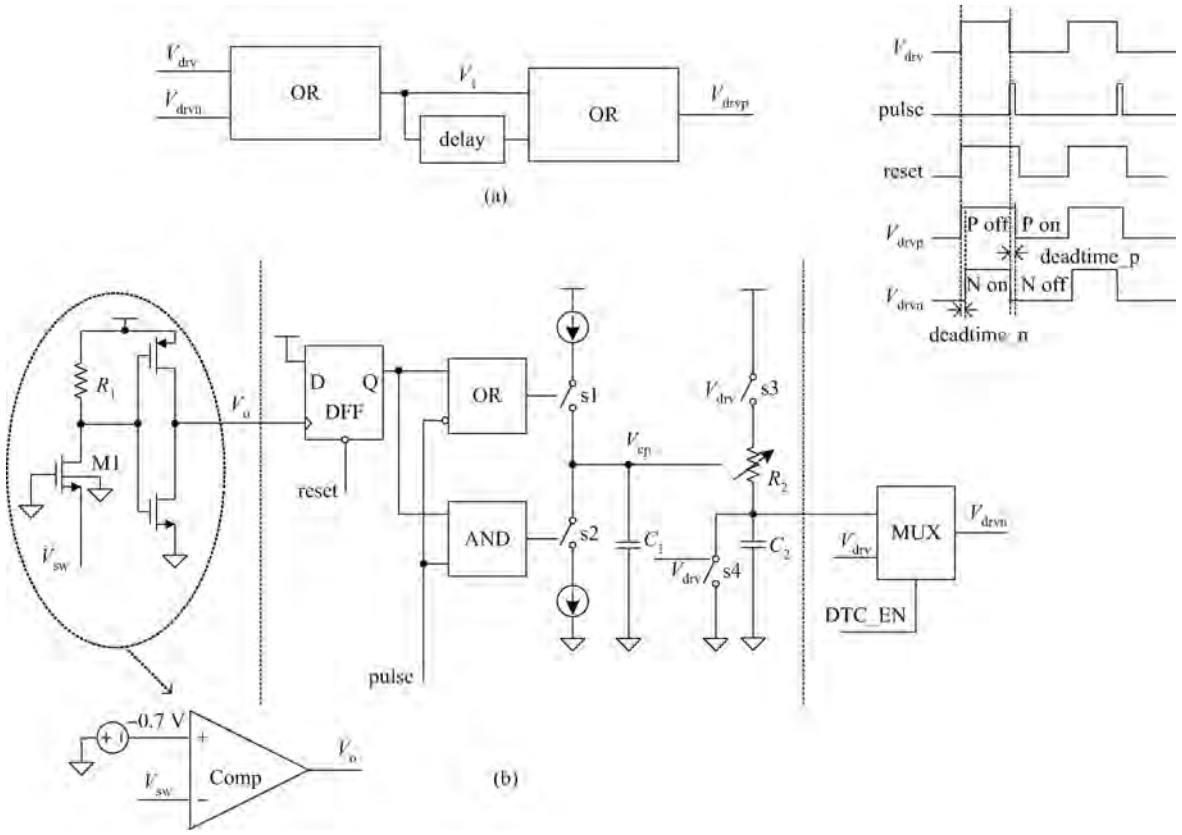

Fig. 7. (a) p-type power MOSFET dead-time controller. (b) Proposed n-type power MOSFET dead-time controller.

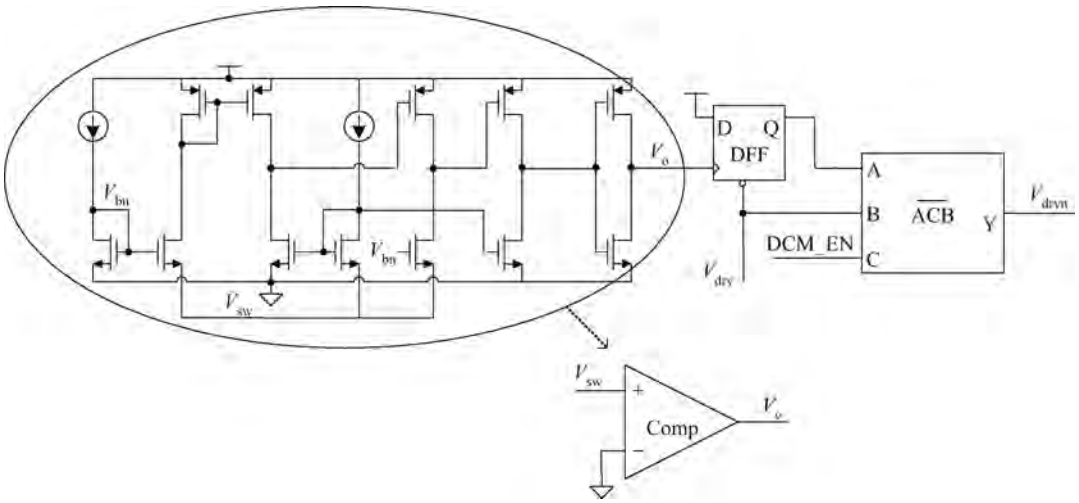

Fig. 8. DCM controller.

the load current, a novel dead time controller based on a charge-pump circuit is presented to realize auto-adaptive dead time. The circuit implementation is shown in Fig. 7(b). The controller has a –0.7 V comparator at the frontend[4]. The comparator determines that the current dead time is too long or too short. If the current dead time is too long, the voltage V_{sw} will drop below –0.7 V while switching on NMOS. If the current dead time is too short, the voltage V_{sw} will not drop below –0.7 V while switching on the NMOS. According to the comparison result, the capacitor of the charge pump will be charged or discharged. The output voltage V_{cp} of the charge pump adjusts the value of the variable resistor R_2. Then dead-time set by R_2 and C_2 is tuned again and again. Finally, the opening time for NMOS is set to the moment when the voltage V_{sw} drops to –0.7 V.

3.2. DCM controller

The DCM controller switches off NMOS when the inductor current drops to zero. Due to the parasitic resistance of the NMOS channel, the direction of the voltage V_{sw} changes as that of the inductor current changes. The circuit uses a comparator to sense the direction of the voltage V_{sw} and reset the control

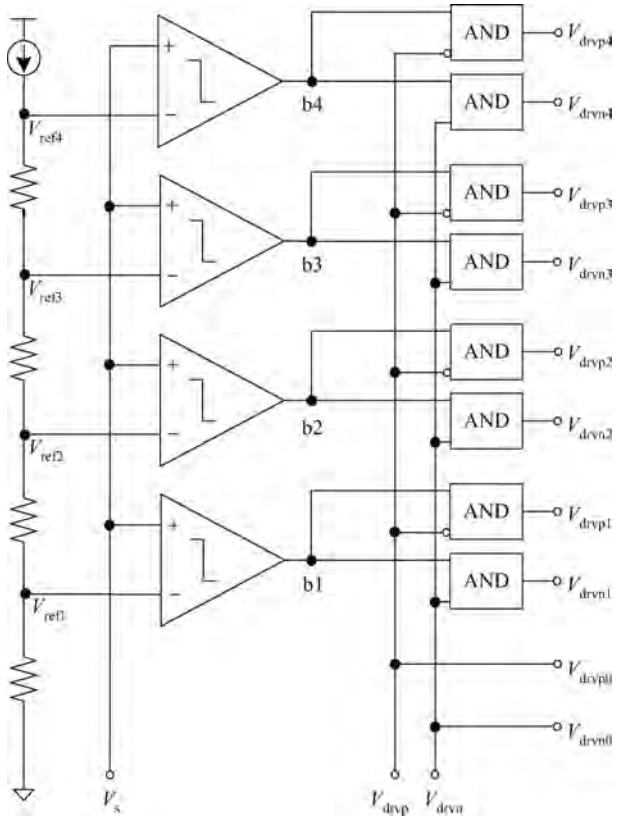

Fig. 9. Width controller circuit.

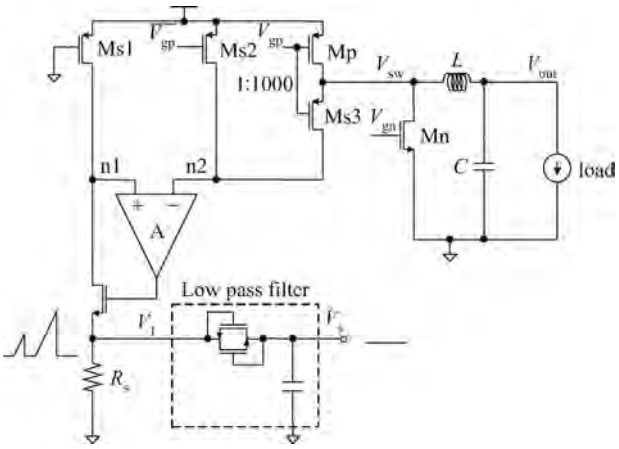

Fig. 10. Proposed current sensing circuit.

signal V_{drvn}. Figure 8 shows the circuit implementation of the DCM controller.

3.3. Power MOSFET width controller

As shown in Fig. 9, the width controller circuit generates five groups of control signal for power MOSFETs. Four of them are generated by a 2-bit flash ADC.

The current-sensing circuit measures the load current, using the method of mirroring the PMOS current. Unlike PWM modulation, the control signal generated by the sigma–delta modulator is with varying period. So, the method of sensing the peak current does not work any longer. An averaging current-sensing circuit is proposed to solve this problem. The circuit implementation is shown in Fig. 10. A low pass filter is applied

Table 1. Performance comparison between this and other work.

Source	CICC2007[6]	PEDS2009[7]	This work
Process	0.18 μm SiGe	0.35 μm CMOS	0.35 μm CMOS
Input range (V)	1.8	3.3	2.7–4.2
Output range (V)	1–2	1.8	1.2–2
Load capability (mA)	0–200	0–200	0–500
Clock frequency (MHz)	10	0.4–1.2	6
Peak efficiency (%)	95	95	93
Noise peak (dB)	N/A	< –75(*)	< –69
Load regulation (%)	< 1	N/A	1
Line regulation (%)	< 1	N/A	2.7
Output voltage ripple (%)	0.7	1.3	1.4
Inductor (μH)	1	10	2.2
Capacitor (μF)	10	600	4.7
Integration level	External L,C	External L,C	External L,C

*Simulation results

to average the sensing voltage V_1. The load current is given by

$$I_{\text{load}} = \frac{V_{\text{dd}}}{V_{\text{out}}}\overline{I_{\text{MP}}} = K\frac{V_{\text{dd}}}{V_{\text{out}}}\frac{V_{\text{S}}}{R_{\text{S}}}, \tag{2}$$

where K is the mirroring ratio. The R in the low pass filter is implemented by an n-type MOSFET. The MOSFET works in the off region, which makes it possible to obtain a low cut-off LPF with a small capacitor.

3.4. Low-power sigma–delta modulator

A second-order sigma–delta modulator is proposed to move out low-frequency noise in the control signal. The block diagram is shown in Fig. 11. The modulator consists of two integrators. One is active-RC and the other is G_{m}–C. The two integrators can provide enough gain to suppress low-frequency noise. Current branch I2a, I2b is applied to compensate current branch I1a, I1b. This means that the amplifier does not need to source current to respond the charge to capacitor C_1 from I1a, I1b. The improvement can make the input of the amplifier closer to virtual ground and reduce the power consumption of the active-RC integrator[5].

4. Experimental results

The proposed buck DC–DC converter with sigma–delta modulation is implemented in the 0.35 μm 2P4M CMOS process and the area is about 2 mm^2. The die photograph is shown in Fig. 12.

Figure 13 shows the measurement results of the output spectrum of the PWM converter and sigma–delta converter. There are clock-referred spikes in the output spectrum of the PWM converter, while the sigma–delta converter is spectrally quiet. In contrast to PWM modulation, the peak noise spike is reduced by 30 dB with sigma–delta modulation.

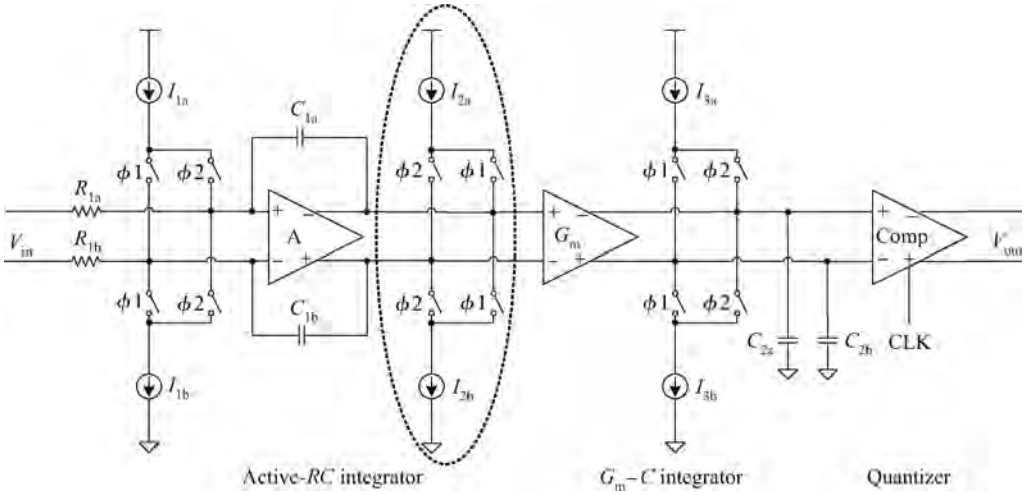

Fig. 11. Second-order continuous-time sigma–delta modulator.

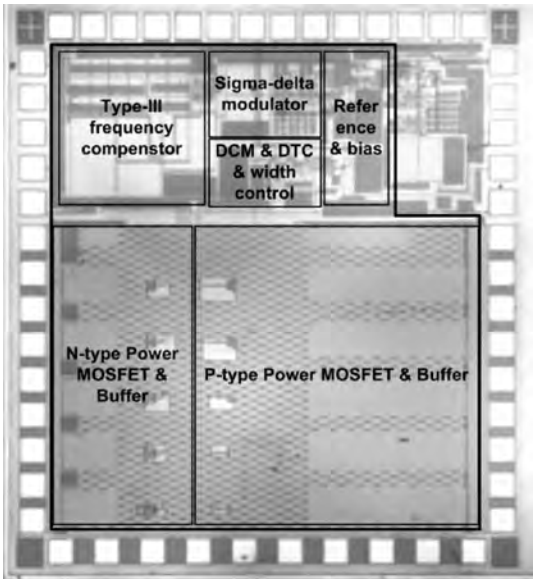

Fig. 12. Micrograph of buck DC–DC converter.

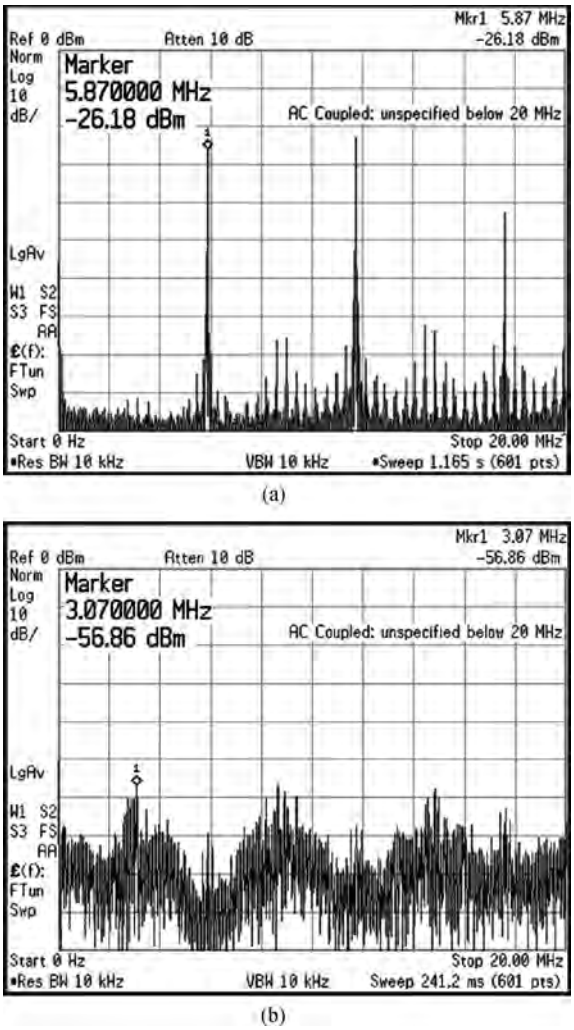

Fig. 13. Output spectrum of buck DC–DC converter. (a) PWM modulation. (b) Sigma–delta modulation.

Dead-time control is one of the key features of the high-efficiency driver. As shown in Fig. 14(a), the voltage V_{sw} will stay too long below –0.7 V when the dead time control is unavailable. This indicates that the body-diode of the NMOS is turned on and corresponding power loss exists. In Fig. 14(b), dead time is optimized by the controller and the body-diode power loss is removed.

Figure 15 shows the DCM controller how to set off-time of the NMOS when the converter is supplying a light load. When the voltage V_{sw} changes its direction, the controller switches off NMOS. Then the node sw becomes floating, and the parasitic capacitance at node sw and inductor forms a L–C oscillator. So the voltage V_{sw} begins to oscillate.

Figure 16 shows that the output of the converter varies by 18.6 mV when the load current jumps from 50 to 500 mA. This means that the load regulation of the converter can reach 1%.

The efficiency of the buck converter with sigma–delta modulation under different loading conditions is shown in Fig. 17. By utilizing the proposed efficiency improvement measures, the converter maintains efficiency of greater than 85% for nominal load currents and reaches peak efficiency of 93% at 400 mA load. A DCM controller can improve the efficiency by 10% for a light load. A dead-time controller (DTC)

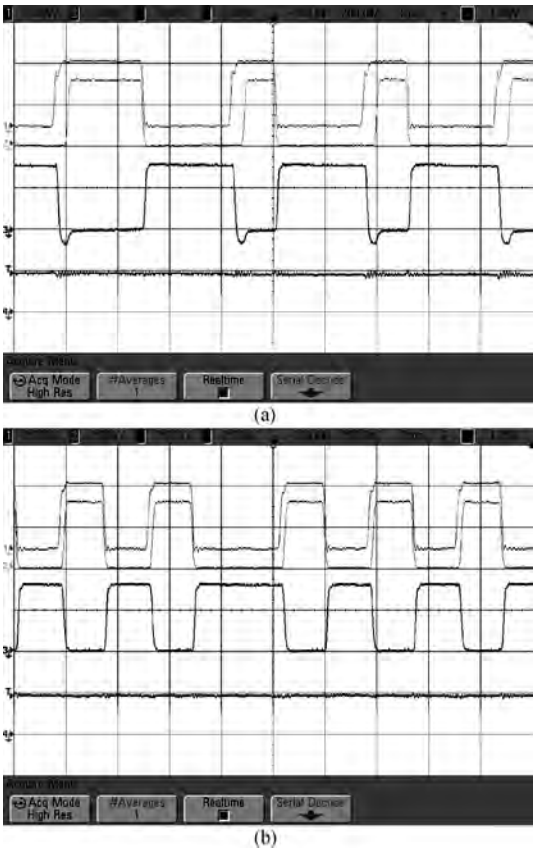

Fig. 14. Waveforms when (a) dead time control is off or (b) dead time control is on (from top to bottom: V_{gpi}, V_{gni}, V_{sw}, V_{out}).

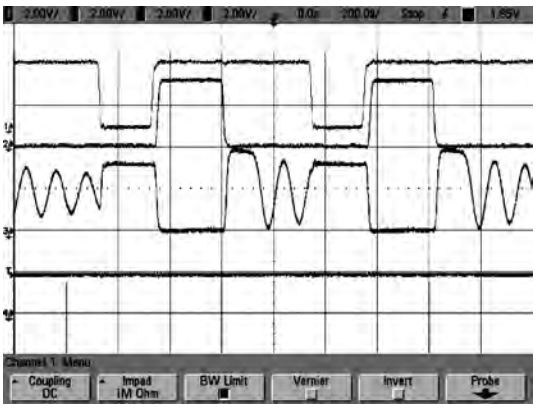

Fig. 15. Waveforms when DCM control is on (from top to bottom: V_{gpi}, V_{gni}, V_{sw}, V_{out}).

can improve the efficiency by 3% for a wide load range, even 5% for some load. If without width control (WC), the efficiency will decrease as the load decreases. This means that the width control is of great help to improve the efficiency for a medium or light load.

Table 1 shows a comparison of previously reported buck DC–DC converters with sigma–delta modulation. Compared with Ref. [6], this work supports a wider load range. The clock frequency of Ref. [7] is very small, which means that the sigma-delta modulator has a limited capacity of noise suppression. It forces us to use a large inductor and capacitor to

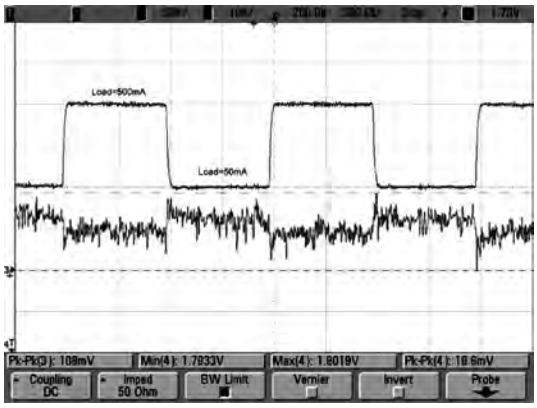

Fig. 16. Response of the converter when the load current is varied from 50 to 500 mA.

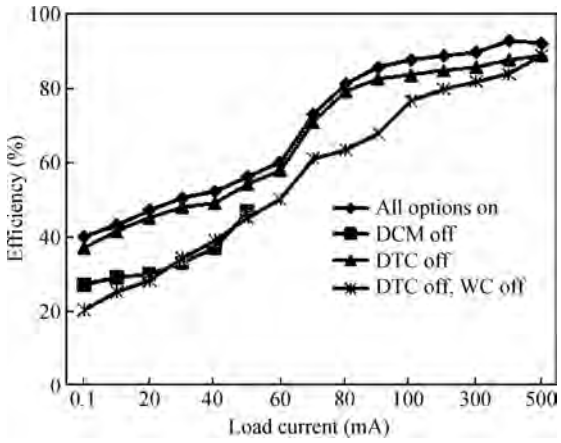

Fig. 17. Efficiency versus load current for the converter with sigma–delta modulation.

enhance the capacity of noise suppression, which will degrade the transient response of the converter. So the performance of the load regulation and line regulation will not be very good.

5. Conclusion

A noise-shaped buck converter based on a 2rd-order continuous-time sigma–delta modulator has been presented. A carefully designed power MOSFET driver, including a dead time controller, a DCM controller and a gate width controller, has been proposed to improve efficiency. An averaging current-sensing circuit for a buck converter with sigma–delta modulation has been applied to measure load current. Compared with the traditional PWM buck converter, the proposed converter effectively suppresses the clock-referred spike by 30 dB with a peak efficiency of 93%.

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