An energy detection receiver for non-coherent IR-UWB*

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Abstract: A non-coherent receiver for impulse radio ultra-wide band (IR-UWB) is presented. The proposed receiver front-end consists of a high gain LNA, a high frequency detector and an intermediate frequency (IF) amplifier to amplify the recovered signal and drive an external test instrument. To meet the requirements of high gain and a low noise figure (NF) under moderate power consumption for the LNA, capacitor cross coupled (CCC) and current reuse techniques were adopted. The detector consists of a squarer and an integrator. The overall circuit consumes 41.2 mA current with a supply voltage of 1.8 V at a 400 MHz pulse rate. The resulting energy efficiency is 0.19 nJ/pulse. A chip prototype is implemented in 0.18-μm CMOS. The die area is 2.1×1.4 mm^2 and the active area is 1.7×0.98 mm^2.

Key words: receiver; IR-UWB; non-coherent; LNA; detector
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1. Introduction

Since the Federal Communications Commission (FCC) opened the unlicensed 3.1–10.6 GHz frequency spectrum in 2002, the capability of high rate transmission in this open spectrum has attracted a lot of attention. Without reaching an agreement in the standard between different organizations，UWB systems tend to fall into two broad categories: multi-band-orthogonal-frequency-division-multiplexing (MB-OFDM) and IR-UWB. One of the competing proposals to IR-UWB, which makes use of extremely short pulses to transmit information, has gained much attention for its potential to achieve high performance with low complexity, low cost and low power consumption.

Two main data demodulation schemes exist in the IR-UWB system, including coherent and non-coherent schemes, which show much difference in the architectures' complexity. Many works have been conducted in both schemes[1−5]. The author in Ref. [1] proposes a distributed pulse correlation receiver achieving a 250 Mbps data rate. References [2, 3] realize energy detection or demodulation with a squarer but References [4, 5] with a passive self-mixer. In Ref. [6], an ON/OFF keying (OOK) receiver is presented and the data rate can reach 500 Mbps. However, the communication distance is restricted to 30 cm. With the characteristic of less complexity and no synchronization requirements, the non-coherent scheme shows a huge advantage over its counterpart. But to meet the demand of wireless high-definition video transmission, the performances of the front-end circuit should be ensured to make the receiver capable of working at data rates up to several hundred of megahertz. This makes the high-data-rate design of a non-coherent receiver a challenge because of its sensitivity to environmental noise and interference.

Figure 1(a) shows a proposed low complexity receiver with an energy detector and an open-loop comparator. This receiver was aimed at accommodating a communication system with a multi-megahertz data rate and a short range.

In this paper, a high performance OOK modulation receiver front-end (Fig. 1(b)) based on an energy doctor (ED) is proposed. The received pulse is firstly amplified by a high performance LNA, which exhibits over 46 dB gain, over 2 GHz bandwidth and NF of 2.5 dB, and is then detected by an ED to recover the transmitted data. To make sure that the recovered signal is detected properly by an open-loop comparator, a low frequency buffer amplifier is added to make the output signal reach the comparator's threshold voltage. The LNA consists of an LNA with input matching, a high frequency amplifier and a high frequency buffer amplifier, which use capacitor cross couple (CCC) and current reuse techniques to reduce the noise figure and power consumption. The detector consists of a squarer and a flipped-voltage follower current sensor (FVF-CS). The complete structure is shown in Fig. 1(b). The prototype is implemented in a 0.18-μm CMOS process.

2. Receiver system consideration

The structure of the proposed non-coherent IR-UWB receiver is illustrated in Fig. 1(a) and the front-end structure is shown in Fig. 1(b). This receiver front end system features large gain and low NF LNA, wide bandwidth IF blocks. The larger gain of the LNA makes less noise contribution from the next stage, making a lower NF receiver for higher sensitivity and data rate, which are priority demands of the system. Wideband IF blocks consisting of a squarer and an amplifier are designed to accommodate high data rate communication. A 1 bit ADC, i.e. a comparator, is implemented by a high gain open loop amplifier with less complexity compared to an ADC with clocks, reducing the system's power consumption. Moreover, the system's requirement on linearity of the front-end is also reduced. To drive the open-loop comparator, the input full scale

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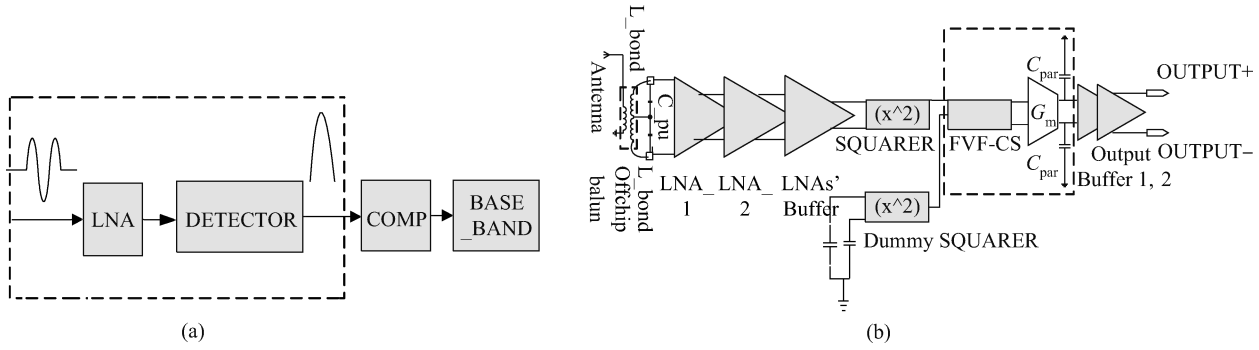


Fig. 1. (a) System structure of the OOK receiver. (b) Proposed front end system for the OOK receiver.

voltage has to be large with a high signal-to-noise ratio (SNR), so an IF amplifier is needed. Compared with a system of multi-bits ADC, there is no need for a variable gain amplifier, thereby simplifying the structure of IF amplifier.

Since in our transceiver system the transmitter is implemented as a narrow pulse modulated by a ring oscillator, and the input signal sequences of the receiver can be modeled as a zero order Gaussian pulse with a carrier, it can be expressed as

$$s_{\text{in}}(t) = \sum_{k=-\infty}^{\infty} p(t - kT) \times [a_k \cos(2\pi f_0 t)], \tag{1}$$

where T is the pulse period, $p(t)$ is the zero order Gaussian pulse, f_0 is the oscillation frequency of the ring oscillator, and a_k represents the binary information symbol, $a_k \in \{0, 1\}$ for a OOK modulation scheme. The demodulated signal is then represented as

$$\begin{aligned} s_{\text{out}}(t) &= \sum_{k=-\infty}^{\infty} \{p(t - kT) \times [a_k \cos(2\pi f_0 t)]\}^2 \\ &= \sum_{k=-\infty}^{\infty} [a_k\, p(t - kT)]^2 \times \frac{1}{2} [1 - \cos(4\pi f_0 t)]. \end{aligned} \tag{2}$$

As a high frequency component in Eq. (2) would be filtered out by the limited bandwidth of the IF blocks, the transmitted data are recovered, demonstrating the functionality of the squarer as a demodulation block.

3. Receiver front-end circuit design

3.1. LNA design and analysis

The performances of the LNA show significant impact on the receiver. It should provide sufficient gain to amplify the weak signal from the antenna without introducing much noise to improve the sensitivity of the receiver. Other performances, such as bandwidth, output P1dB, input matching, ESD protection and power consumption, are also very important. It should cover a frequency range of 3–5 GHz, which is the transmitted signals' frequency spectrum. The lowest output voltage swing of the LNA is required to get over minimum input voltage of the squarer in the energy detector. To meet so many rigid requirements, a LNA with three gain stages is designed. The first stage, shown in Fig. 2(a), is designed as a common gate amplifier with CCC[7] and current reuse techniques. A standalone version is designed and the measured results are shown in Section 4.1. The second stage illustrated in Fig. 2(b) is a RF gain stage that also uses the current reuse technique to save power consumption. Inductor shunt peaking is used for the load of the two stages, and the spiral inductors are optimized to save chip area. Finally, a capacitor cross couple buffer depicted in Fig. 2(c) is used to boost the gain and output voltage swing.

This receiver front-end is expected to be employed in the wireless high-definition video transmission system, therefore ESD protection and the interface with the antenna should be considered. The antenna is connected with differential LNA input through an off-chip balun and bonding wire. The bonding wire and off-chip balun is modeled and taken into simulation, as shown in Fig. 2(a). Although a common-gate amplifier is less sensitive to the ESD pulse, an extra ESD protection diode is added to further improve the system's robustness.

Voltage gain transfer functions of each stage are expressed as

$$\begin{aligned} A_{\text{V1}} \approx{}& \frac{Z_{\text{L1}}(1 + 2g_{\text{m1}}r_{01})}{(1 + g_{\text{m1}}r_{01})R_{\text{s}} + (Z_{\text{L1}} + r_{01})[1 + 4C_{\text{gs1}}sR_{\text{s}}]} \\ &\times g_{\text{m3}}\{[(1 + g_{\text{m3}}r_{05})r_{03} + r_{05}]//Z_{\text{L2}}\}, \end{aligned} \tag{3}$$

$$A_{\text{V2}} \approx g_{\text{m7}}Z_{\text{L5}} \times g_{\text{m9}}\{[(1 + g_{\text{m9}}r_{011})r_{09} + r_{011}]//Z_{\text{L7}}\}, \tag{4}$$

$$A_{\text{V3}} \approx (g_{\text{m13}} + g_{\text{m15}})/g_{\text{m13}}. \tag{5}$$

The NF of the cascaded LNA can be expressed as

$$F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2}, \tag{6}$$

where F_1, F_2, F_3 are the NF of each stage, and G_1, G_2 are the gain of the first and second stage. As G_1, G_2 are sufficiently high, the NF contributions from F_2 and F_3 can be neglected, and then the total NF is determined by the first stage LNA. Due to the CCC technique, the NF of the common gate LNA is improved and its NF is[7]

$$1 + \frac{\gamma}{2\alpha}\Big|_{2g_{\text{m1}} = \frac{1}{R_{\text{s}}}},$$

while the NF of the conventional common gate LNA is

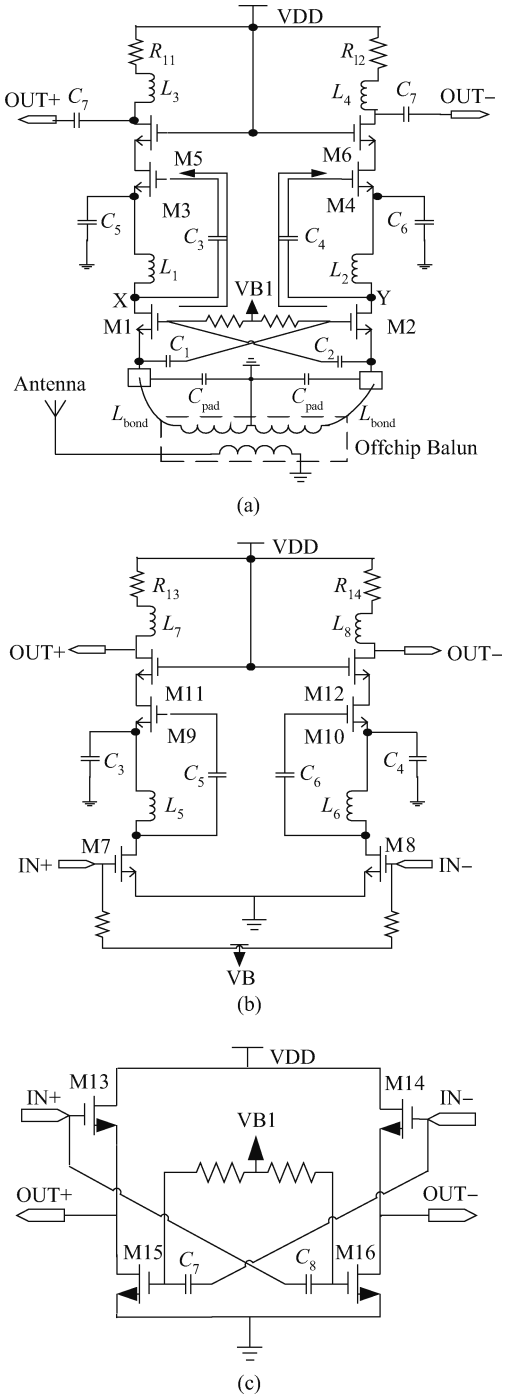


Fig. 2. (a) The first stage of the LNA. (b) The second stage of the LNA. (c) The third stage of the LNA.

$$1+\frac{\gamma}{2\alpha}\Big|_{g_{m1}=\frac{1}{R_S}}.$$

This improvement is achieved with a reduction in power consumption compared with a conventional common gate LNA, but sacrificing a little additional area for extra capacitors.

Although no stringent linearity performance is required in such a OOK receiver with a 1-bit ADC, the large output swing of the LNA is necessary to get over the detection sensitivity of the squarer. A conventional source follower buffer is a popular buffer with high reverse isolation, but its output swing is limited by its quiescent current because of class-A operation of this amplifier. Therefore the differential cross-coupled buffer in Fig. 2(c) is employed. This is a class-AB amplifier that is similar to a simple inverter, but it provides much better reverse isolation and produces less loading Miller capacitance for the second stage of the LNA than the inverter. A larger output swing can be achieved by this cross-coupled buffer than the source follower as its peaking output current is larger than its quiescent current. Thus, this differential cross-coupled buffer is a better candidate in this application.

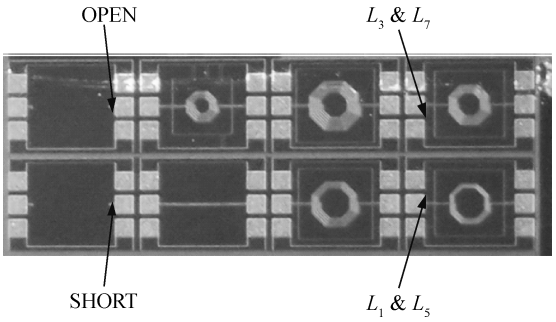


Fig. 3. Chip photo of the inductors.

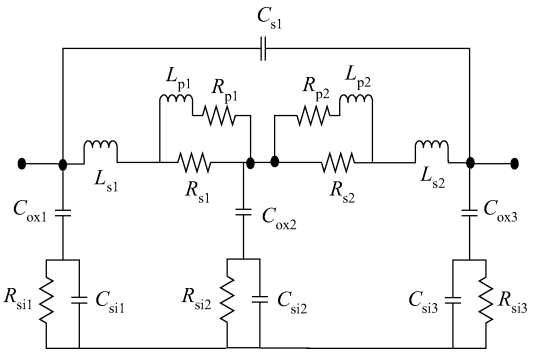


Fig. 4. Equivalent 2-π model for the spiral inductor.

Inductors are of great important as they can boost the gain and bandwidth of the LNA，which are required by the UWB system. To make an accurate prediction of the performances of the LNA, all of the inductors used in the LNA are simulated and optimized through EM simulation, then on wafer probe test are taken to correct the simulation. The test layout of the inductors with an open-short de-embedding structure is shown in Fig. 3.

Measured result after de-embedding gives the Y parameters of the inductor, and then the inductance and quality factor can be yielded as

$$L=\frac{\mathrm{Imag}(1/Y_{11})}{2\pi f},\qquad Q=\frac{\mathrm{Imag}(1/Y_{11})}{\mathrm{Real}(1/Y_{11})}. \tag{7}$$

To take the measured results of the inductors into the circuit simulation, a modified 2-π[8] model that is suitable for wideband parameter extraction is exploited. The model is shown in Fig. 4. Measured and simulated results of the inductors are shown in Fig. 5. The difference between them is less than 5%.

As shown in Fig. 5, the peak of the quality factor of the

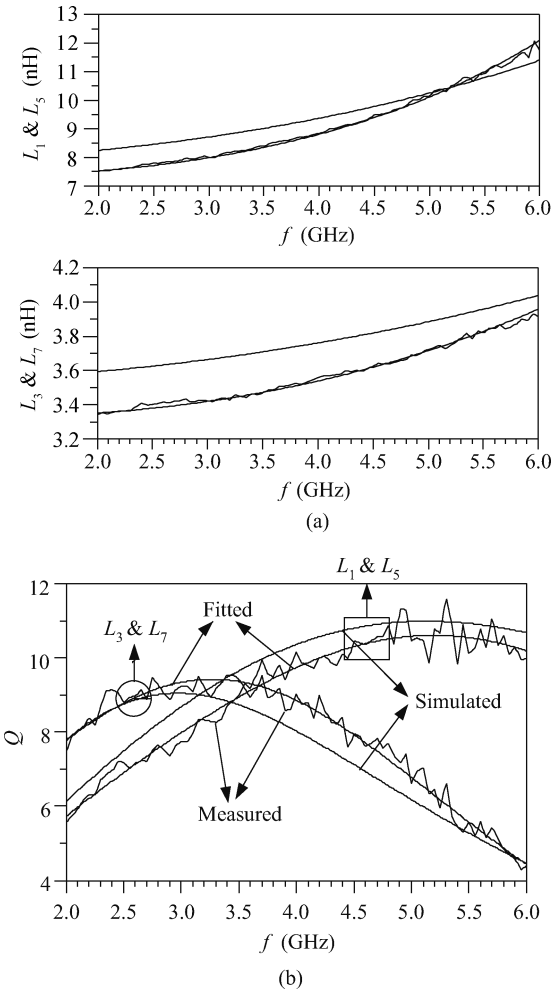


Fig. 5. Measured and simulation results of the spiral inductor. (a) Inductance of the inductors. (b) Quality factor of the inductors.

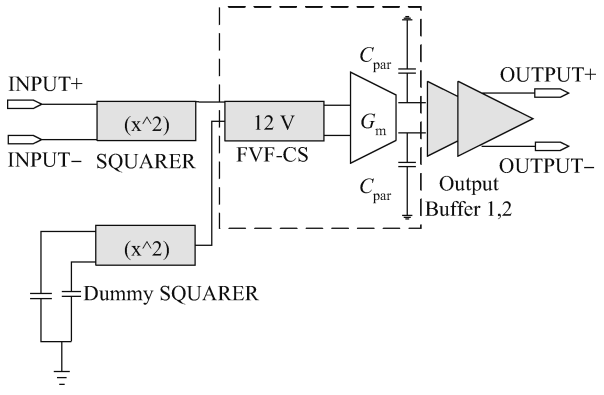


Fig. 6. Detector structure.

inductors is located at 3 and 5 GHz; such frequency selection characteristic of the inductors is profitable because unwanted interferers can be attenuated. A two stage LC amplifier enhances this attenuation[9], making this receiver relatively robust to interferers outside the 3–5 GHz band. To further mitigate interference from a WLAN device, a notch filter can be added[10].

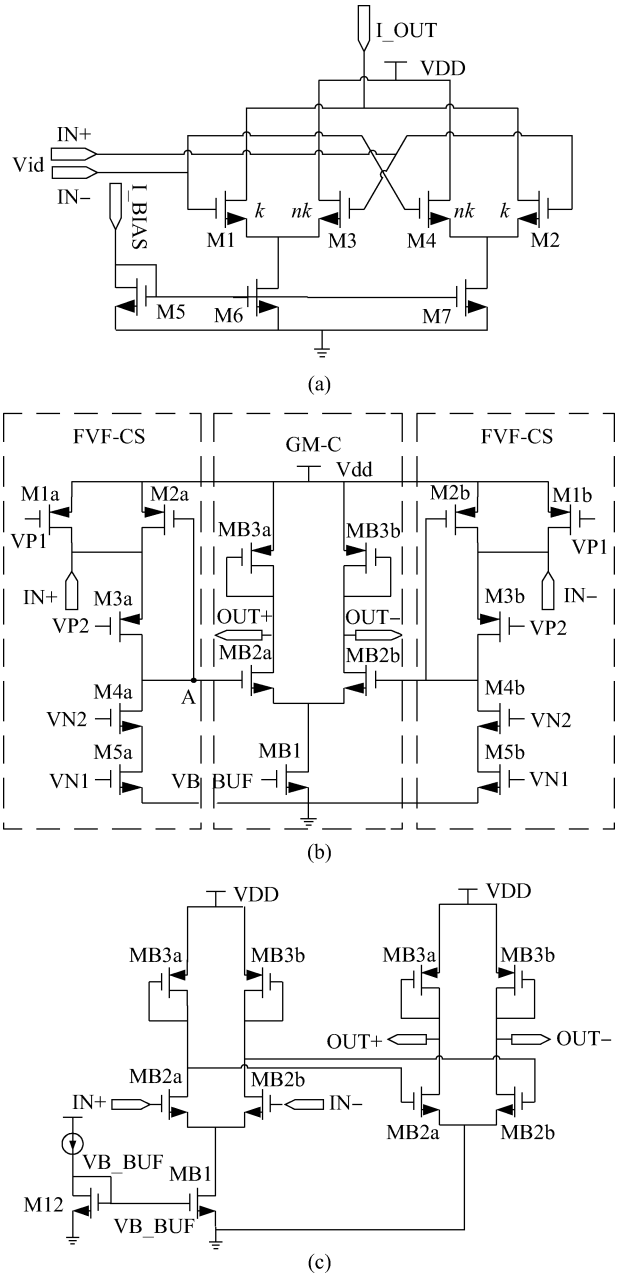


Fig. 7. Detector circuits implementation. (a) Squarer circuit. (b) FVF-CS and G_m–C integrator circuit. (c) Output buffer circuit.

3.2. Energy detector design

The detector is used to recover the envelope of the pulse, which is often implemented as a self-mixer[3, 4] and step recovery diode (SRD). The self-mixer shows a large conversion loss and the SRD is difficult to integrate into standard CMOS technology. In this paper, the squarer and the G_m–C integrator are applied to demodulate the data, which are shown in Fig. 6. The function of the squarer can be represented as[11]

$$I_{OUT} = 2I_B + kV_{id}^2, \qquad V_{id} \in \left\{ -\sqrt{\frac{I_B}{k}}, \sqrt{\frac{I_B}{k}} \right\}, \tag{8}$$

where I_{OUT} is the output of the squarer, I_B is the static current of I_{OUT}, and k denotes the current gain of the squarer. The circuit structure is shown in Fig. 7(a). The squarer's output current

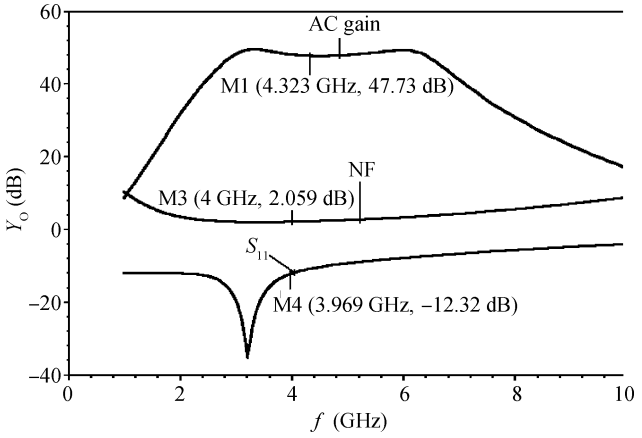


Fig. 8. Simulation results of the LNA.

is injected into the in+ of the FVF-CS. Another squarer with AC ground input is also added to make a static current $2I_B$ injection into in- of another FVF-CS, therefore only a differential small signal is processed by the following circuits. I_{OUT} is converted into voltage by the FVF-CS, which is shown in Fig. 7(b), then is integrated by the G_m–C circuit to fully recover the envelope, while the high frequency component ($2f_0$) in Eq. (2) is filtered out by the limited bandwidth of the circuit. The G_m–C circuit is implemented as a common source amplifier with a diode. The received energy can be demonstrated as[12]

$$E_p \propto \omega_0 \int_{\tau}^{\tau+T} R_{conv} I_{OUT} dt, \tag{9}$$

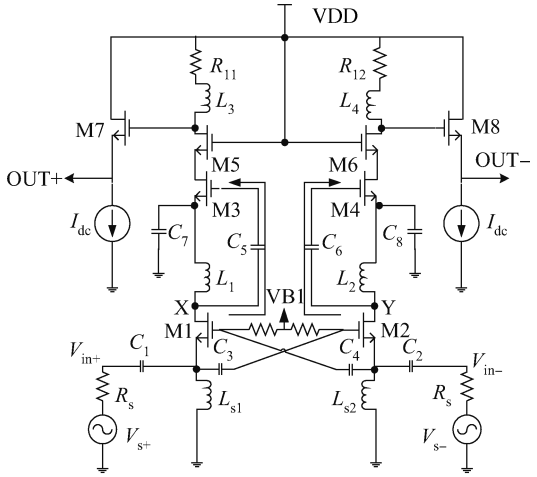
where R_{conv} is the transimpedance gain of the FVF-CS, ω_0 is the unity gain of the G_m–C integrator, and T is the integration duration, which is set to be the time duration of the pulse.

As this receiver front end is targeted for high data rate transmission, a wideband frequency response of each block should be required. So the transistors in the squarer are chosen with relatively small size and large current consumption to trade off between bandwidth, noise, and power consumption. The conversion gain and bandwidth of the FVF-CS should be traded off as the R_{conv} is inversely proportional to the transconductance of M2a[11]. The G_m cell of the G_m–C integrator is designed to be a common source amplifier with a diode connected load, which has a large bandwidth but small gain. To boost the output voltage swing and drive the test instrument, a similar two-stage amplifier shown in Fig. 4(c) is added to improve the output voltage and drive the test instrument while maintaining a large bandwidth. The buffer amplifier isn't needed for a fully integrated chip with a comparator, and then the amplifier could be modified to save power consumption. In addition, the output of the amplifier is also ESD protected.

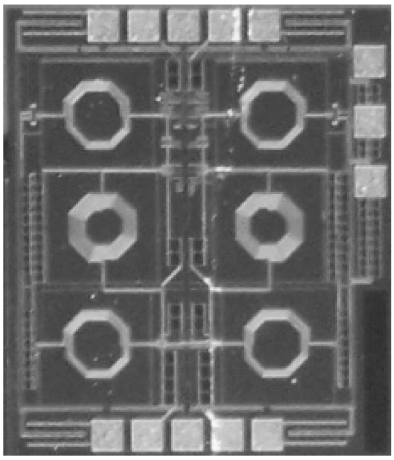
4. Simulated and measured results

4.1. LNA simulation results and their validation

The LNA's post simulation results are shown in Fig. 8. This shows that the first stage LNA and the second stage amplifier contribute 22 dB and 20 dB voltage gain, respectively, while the cross couple buffer offers an extra 6 dB without any spiral inductor. The overall gain of this LNA gets over 47 dB.



(a)



(b)

Fig. 9. (a) Schematic of the stand-alone LNA. (b) Its chip photo.

Such a high gain amplifier is easy to trigger to oscillate by many hint feedback paths, such as power and ground bond wires. Another possible feedback is through mutual inductance between the inductors, and this might cause a disastrous stability problem, therefore strategic layout techniques should be used to reduce it. Two methods are adopted in this paper. First, every inductor has its own substrate contacts ring[13], which are placed around 50 μm (about twelve line widths compared with traditional five line widths) away from the inductor. Additionally, the floor plan of every two inductors in proximity is chosen to have their current perpendicular with each other, which is shown in the chip photograph in Fig. 12(a).

The simulated results of this LNA can be further validated by a standalone LNA, which is the same as the first stage of the LNA. It has the same component size as the first stage amplifier, but inductors at the input of the LNA are omitted in the receiver to reduce the chip area. A source follower is added to drive a 50 Ω measurement instrument, introducing a nearly 6 dB voltage gain loss. Its circuit and chip photo are shown in Fig. 9.

On wafer probe tests are carried out. An Agilent 4-port vector network analyzer (VNA) is used to measure the S parameters. The test result is shown in Fig. 10. Good agreement between measurement and simulation S_{21} is achieved except

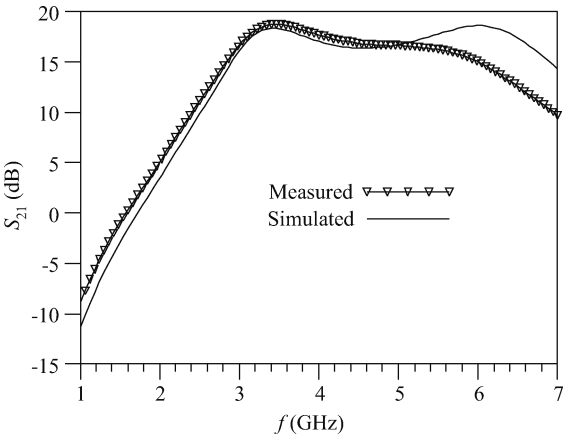
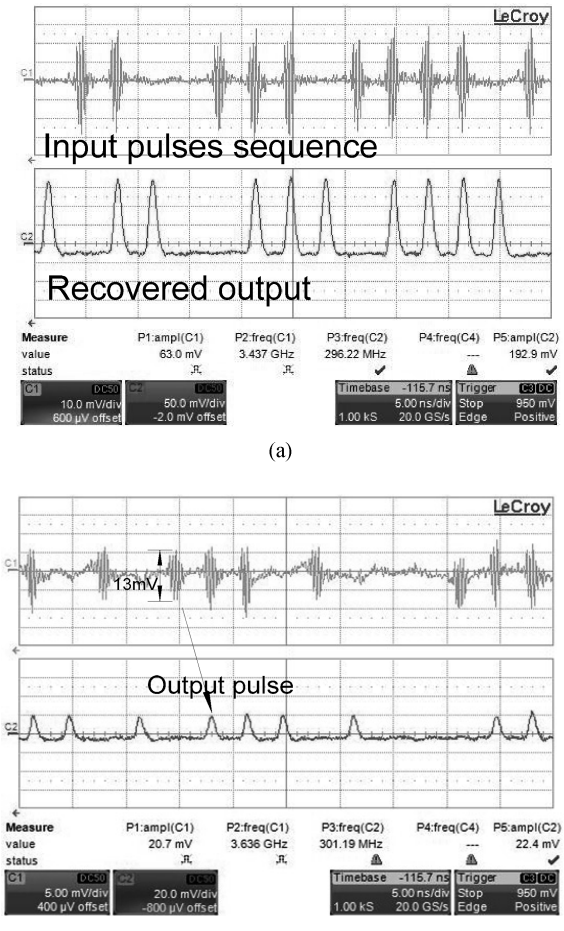


Fig. 10. Measured S_{21} of the stand-alone LNA.



(a)

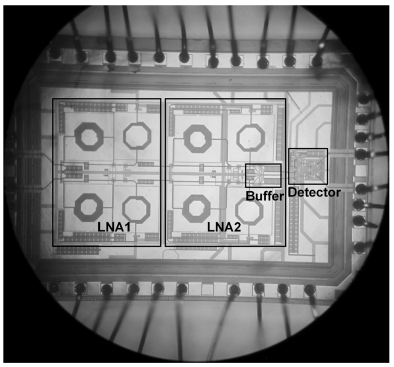
(b)

Fig. 11. Performance of the detector. (a) Transient response of the energy detector. (b) Detection sensitivity of the detector.

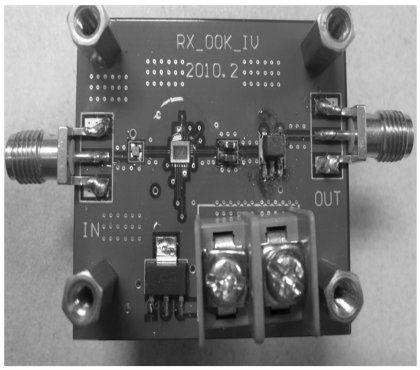
for a difference at a frequency above 5 GHz. Therefore, it is reasonable to conclude that the gain of the LNA in the receiver is accurately predicted by simulation.

4.2. Detector's simulation and measurement results

A stand-alone detector is tested to verify its function. A common-gate input matching circuit and a common source amplifier with a resistor load is added compared with the one in the receiver front-end.



(a)



(b)

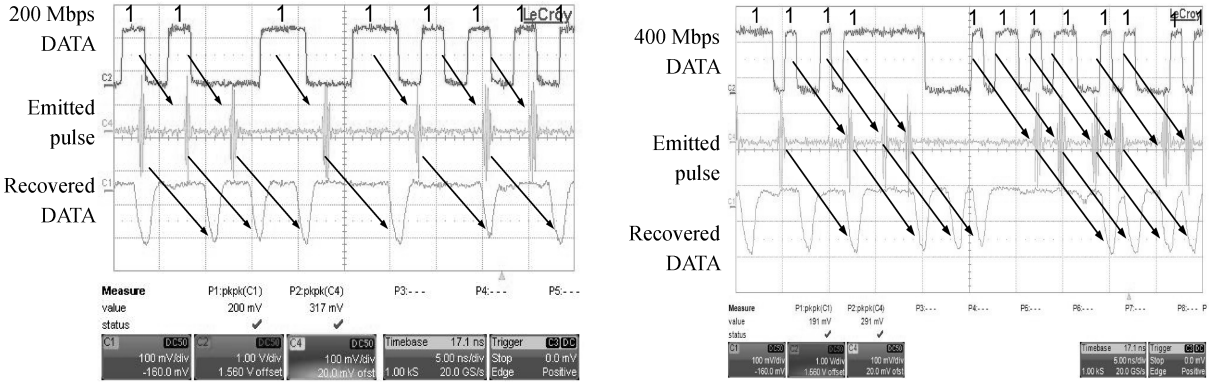
Fig. 12. Photographs of the (a) chip and (b) PCB.

To verify its functionality and measure the detection sensitivity of the detector, an OOK transmitter and an attenuator are used to send a variable amplitude input pulse. Measured results shown in Fig. 11 indicate normal function of the detector with 9.5 dB conversion gain and detection sensitivity of about 13 mV (peak-to-peak).

4.3. Receiver front-end measurement

The chip is measured in a chip-on-board system. The conversion gain of this system is estimated to be 57 dB from simulated and measured data. Figure 12 is a photograph of the chip and test PCB. The die size is 1.7×0.98 mm^2, and is 2.1×1.4 mm^2 including the pads and ESD ring. The LNA including its buffer, two squarers, integrator, output buffer and bias circuit draw 22, 3.6, 6.2, 6.5, 3.1 mA respectively from a 1.8 V supply, and the total power consumption is 74.2 mW.

To verify the functionality of the receiver front end, a wired test bench is set up. An OOK transmitter is used as the input of the receiver, and an attenuator is added to model free space path loss. Pseudo-random bit sequences (PRBS) are used to modulate the transmitter, and the recovered data from the receiver is captured by a Lecroy's oscillograph. When the attenuator is set to 50 dB and the output signal power of the attenuator is –56.5 dBm, the recovered output signal is 200 mV (Fig. 13), which is sufficient to drive the open-loop comparator. The sensitivity of the receiver front end can be deduced from the sensitivity of the detector and the gain of the LNA. The sensitivity of the stand-alone detector is –33 dBm. After de-embedding the gain of the input matching and common source amplifier



(a) 200 Mbps (b) 400 Mbps

Fig. 13. Measurement of received pulse sequences.

Table 1. Performance comparison of receivers.

Parameter	This work	Ref. [1]	Ref. [3]	Ref. [14]	Ref. [6]
Freq (GHz)	3.1–5	3–10	3.1–5	3.1–5	3.1–5□
Modulation scheme	OOK	OOK	OOK	PPM*	OOK
Max PRF (MHz)	400	250	1	200	500
Energy efficiency (nJ/pulse)	0.19	0.17	3.1	0.405	0.022
Die area (mm^2)†	1.67	1.2	2.8◯	4.42△	0.29
Technology (μm)	0.18	0.18	0.18	0.18	0.18

† Active area ◯ Core size of transceiver * Pulse-position modulation (PPM) △ Transceiver □ Target at 3.1–5 GHz, actually at 2.6–4.5 GHz

(8 dB), the sensitivity of the detector in the receiver is –25 dBm, then the receiver's sensitivity is deduced to be –72 dBm at a 400 Mbps data rate.

The maximum data rate is around 400 Mbps as it is restricted by the recovered pulse duration. If the data rate is set higher, the pulses will overlap with each other, causing inter symbol interference (ISI) and degrading the bit error rate (BER) of the receiver. The optimum power efficiency is 0.19 nJ/bit at a 400 Mbps data rate.

The measured performances of the proposed receiver are compared with some other UWB receivers, as shown in Table 1.

5. Conclusion

A CMOS non-coherent IR-UWB receiver based on energy detection is presented. Proposed receiver circuit blocks are used to support high speed data transmission under moderate power consumption. Circuit techniques and a size optimization strategy have been proposed in this high data rate receiver, including CCC and current reuse for the LNA and its buffer to achieve sufficient gain and bandwidth with less power consumption, transistors' sizing strategy for the detector to attain a large bandwidth and layout considerations to reduce mutual inductance coupling. Made by 0.18-μm CMOS technology, the receiver front end consumes 74.2 mW and has a die area of 1.67 mm^2. Up to a 400 MHz data rate has been achieved with a power efficiency of 0.19 nJ/bit. It has been successfully used in a demo system for wireless high-definition video transmission.

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