# A 0.18 $\mu$m CMOS low noise amplifier using a current reuse technique for 3.1–10.6 GHz UWB receivers*

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**Abstract:** A new, low complexity, ultra-wideband 3.1–10.6 GHz low noise amplifier (LNA), designed in a chartered 0.18 $\mu$m RFCMOS technology, is presented. The ultra-wideband LNA consists of only two simple amplifiers with an inter-stage inductor connected. The first stage utilizing a resistive current reuse and dual inductive degeneration technique is used to attain a wideband input matching and low noise figure. A common source amplifier with an inductive peaking technique as the second stage achieves high flat gain and wide –3 dB bandwidth of the overall amplifier simultaneously. The implemented ultra-wideband LNA presents a maximum power gain of 15.6 dB, and a high reverse isolation of −45 dB, and good input/output return losses are better than –10 dB in the frequency range of 3.1–10.6 GHz. An excellent noise figure (NF) of 2.8–4.7 dB was obtained in the required band with a power dissipation of 14.1 mW under a supply voltage of 1.5 V. An input-referred third-order intercept point (IIP3) is –7.1 dBm at 6 GHz. The chip area, including testing pads, is only $0.8 \times 0.9$ mm$^2$.

**Key words:** CMOS; low noise amplifier; ultra-wideband; current reuse; common source; noise figure
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## 1. Introduction

Since the Federal Communications Commission (FCC) allocated 7500 MHz bandwidth for ultra-wideband (UWB) applications in the 3.1–10.6 GHz frequency range, the related technologies have attracted much attention from both industry and academia. This new standard provides low cost, low complexity, low power consumption, high security, and high data-rate wireless communication capabilities, which can be used in wireless personal area networks (WPAN), medical-image systems, and vehicular communications[1]. Due to the FCC's stringent power emission limitation (–41.3 dBm/MHz) at the transmitter and the transmission path loss, the received UWB signal exhibits very low power spectral density at the receiver antenna. The ultra-wideband LNA determines the overall system sensitivity because it is the first block to amplify the received signal from the antenna. It becomes a critical component in providing sufficient gain over bandwidth. Compared to traditional narrow-band LNAs, the design of an ultra-wideband LNA is quite different and provides challenges in radio frequency (RF) receivers, such as good broadband input impedance matching to minimize the return loss, sufficient and flat gain, a low noise figure (NF), low power consumption, and good linearity within the entire frequency band[2].

Much research on CMOS ultra-wideband LNA designs in submicron technologies has been presented in recent years, such as the distributed amplifier, the filter matching network amplifier, the resistive shunt feedback amplifier and the current reuse amplifier. A distributed amplifier, which is often applied to improve gain at high frequency and hence can extend the bandwidth, has the inherent advantages of wideband power gain and temperature-insensitive wideband input/output impedance matching, but it consumes more power and area for the cascade of several stages[3−5]. The filter matching network amplifier can achieve wideband input matching and show good wideband performances while dissipating a small amount of power. However, the filter at the input requires a number of reactive elements, which could lead to NF degradation and a large chip area, in the case of on-chip implementation[6, 7]. The resistive shunt feedback amplifier can provide good impedance matching and improve gain flatness. However, it is hard to satisfy gain and noise requirements simultaneously[8, 9]. The current reuse amplifier is useful for high gain and low power dissipation, but the reported wideband is not enough for 3.1–10.6 GHz applications[10].

In this paper, a two-stage broadband LNA for ultra-wideband applications in 0.18 $\mu$m RFCMOS technology is proposed. In the proposed ultra-wideband LNA, a resistive current reuse and dual inductive degeneration techniques are adopted in the first stage for broadband simultaneous noise and input impedance matching. Meanwhile, an inductive peaking technique is adopted in the second stage for bandwidth enhancement. With these techniques, the ultra-wideband LNA demonstrates an excellent noise performance as low as 2.8–4.7 dB in the required band with a maximum power gain of 15.6 dB while consuming only 14.1 mW under a supply voltage of 1.5 V.

## 2. Operational principle and circuit implementation

### 2.1. Resistive current reuse theory

The conventional cascode topology has numerous bene-

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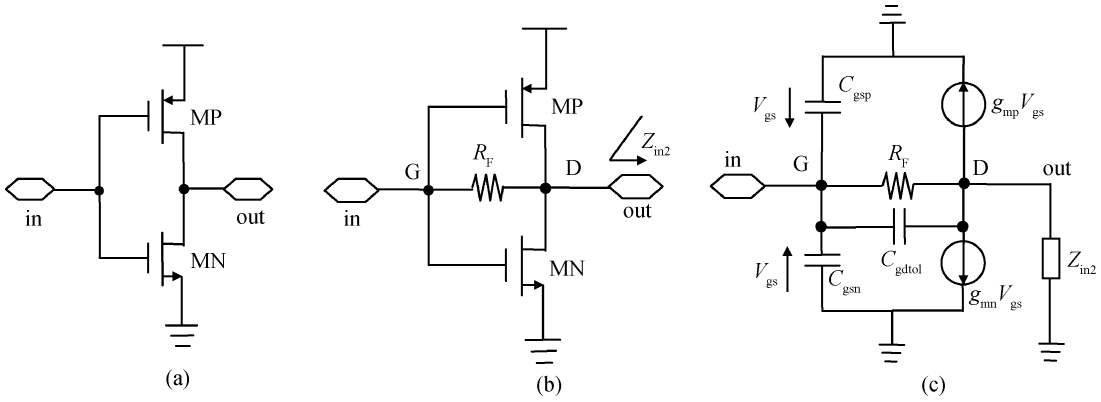


Fig. 1. Schematic of (a) traditional current reuse amplifier, (b) resistive current reuse amplifier and (c) its simplified equivalent circuit.

fits, such as good reverse isolation, quasi flat band large gain and a low noise figure, which make it very popular in the ultra-wideband LNA designs. Nevertheless, stacking two NMOS transistors, it suffers from a nominal supply voltage, which is not suited to aggressive scaling of the advanced CMOS technologies. In this paper, combining a PMOS and a NMOS transistor between the two supply rails, the current reuse topology allows it to be low voltage compatible. Figure 1(a) is a traditional current reuse amplifier, and Figure 1(b) is a resistive current reuse wideband amplifier, which can be studied along with the simplified small signal model depicted in Fig. 1(c). The resistive current reuse amplifier boosts circuit transconductance and utilizes DC current reuse to save power consumption. Indeed, stacking both NMOS and PMOS transistors, the overall equivalent transconductance is increased from $g_{mn}$ to $g_{mn} + g_{mp}$ for the same biasing current. Furthermore, this configuration holds on the transistors in saturation region under a minimum supply voltage, without a stringent design tradeoff. The resistive current reuse topology is one technique that is commonly used to desensitize a circuit and make the power gain and input impedance less sensitive to parasitics, temperature and process variations.

In Fig. 1(c), it is assumed that the circuit is connected to a source generator whose $R_S$ impedance is typically 50 Ω. In the first approximation, we can derive the analytic expressions of the voltage gain ($A_V$), noise figure and input impedance ($Z_{in1}$) as

$$A_V \approx \left(g_{mn} + g_{mp}\right)\left(R_F // r_{dsN} // r_{dsP} // Z_{in2}\right), \quad (1)$$

$$\mathrm{NF} \approx 1 + \frac{2}{3}\frac{1}{\left(g_{mn} + g_{mp}\right) R_S}\left(\frac{1}{R_S} + \frac{R_S}{R_F^2}\right) + \frac{2}{3}\left(g_{mn} + g_{mp}\right) R_S \left(\frac{f}{f_T}\right)^2 + \frac{R_S}{R_F}, \quad (2)$$

$$Z_{in1} \approx \frac{R_F + r_{dsN} // r_{dsP} // Z_{in2}}{1 + A_V}. \quad (3)$$

In a –3 dB bandwidth ($\mathrm{BW}_{-3\mathrm{dB}}$) defined as it follows,

$$\mathrm{BW}_{-3\mathrm{dB}} = (1 + A_V) / \left[R_F\left(C_{gstol} + (1 + A_V) C_{gdtol}\right)\right], \quad (4)$$

with $C_{gstol} = C_{gsn} + C_{gsp}$ and $C_{gdtol} = C_{gdn} + C_{gdp}$, where $g_m$, $C_{gs}$ and $C_{gd}$ are the transconductance, gate to source and gate to drain capacitors of MN (MP), respectively. $f_T$ is the cutoff frequency of the MOS transistor, $Z_{in2}$ is the input impedance of the following stage and $R_F$ is the feedback resistance. It can deduce from Eqs. (1)–(4) some design tunes leading to the optimization of the different characteristics. With the resistive current reuse approach, a large feedback resistance $R_F$ contributes to a lower NF in Eq. (2), while the increased transconductance $g_{mn} + g_{mp}$ achieves a higher $A_V$ for a reasonable current consumption in Eq. (1). At the same time, the growth of $A_V$ mitigates the growth of parasitic capacitor value to keep a wide –3 dB bandwidth in Eq. (4). When dealing with NF and bandwidth, high $A_V$ and small $R_F$ lead to wider –3 dB bandwidth. However, smaller $R_F$ is not a desirable approach in Eq. (2), while $R_F$ is limited in Eq. (3) for a fixed input impedance, typically 50 Ω. The price to pay for the improvement in input matching and the –3 dB bandwidth with the use of resistive current reuse in ultra-wideband LNA is an increase in noise figure.

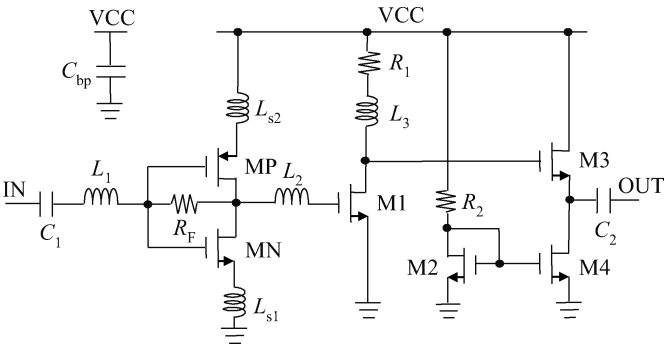


Fig. 2. The proposed ultra-wideband LNA architecture.

To relax the design constraints, the various techniques brought into play are described in the next section. By combining the resistive current reuse and dual inductive degeneration techniques, we've managed to design a new topology that is well suited to low voltage and UWB applications. The first stage of the proposed ultra-wideband LNA is optimized for wideband input matching and a low noise figure, while the second stage is optimized to extend the –3 dB bandwidth of the overall amplifier, respectively. The combination of stages can provide flat high gain, low noise figure and wide bandwidth simultaneously.

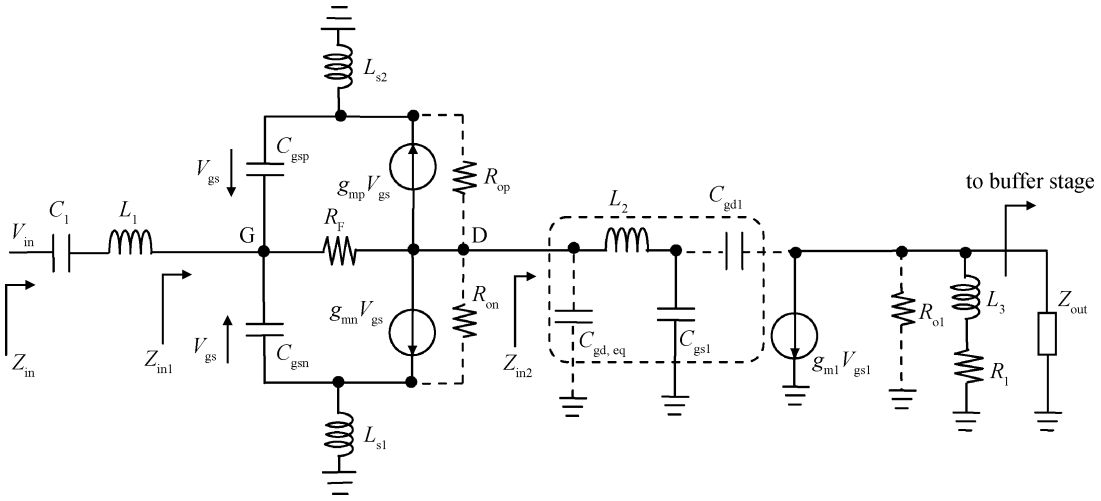


Fig. 3. Small signal equivalent circuit of the first and second stage amplifier in Fig. 2.

### 2.2. Circuit design

The circuit diagram of the proposed ultra-wideband LNA, including the biasing circuit, is shown in Fig. 2, which is composed of two simple amplifiers with an inter-stage inductor connected. In the first stage of the ultra-wideband LNA, to increase the voltage gain and with low DC power under a minimum supply voltage, it adopts a current reuse topology (MN and MP) with the self-biasing by a feedback resistor, $R_F$, as presented in the previous section. The main problem with the use of resistive current reuse in the LNA is that the parasitic capacitances due to the Miller effect lead to degradation in input impedance and the –3 dB bandwidth at high frequency. To overcome this problem, dual source degenerated inductors ($L_{S1}$ and $L_{S2}$) and inter-stage inductor $L_2$ are adopted for the partial tuning-out of the parasitic capacitances.

For input matching, the LC network ($L_1$ and $C_1$) combined with the dual degenerated inductors ($L_{S1}$ and $L_{S2}$) and the intrinsic capacitances of current reuse topology to form a multisection LC ladder network to achieve a wideband matching characteristic to 50 Ω. The small signal equivalent circuit of the first stage is illustrated in Fig. 3, where $Z_{in2}$ is the input impedance of the second stage. Note that, due to the existence of $C_{gd}$ and $R_F$, the input stage is treated as a bilateral two-port network and the input impedance is influenced by the output impedance of the first stage. We assume that the input Miller effect of the overlap capacitance $C_{gdn}+C_{gdp}$ is relatively small, which is generally the case in practical designs. Therefore, focusing on the first stage in Fig. 3, the total transconductance $g_{m,tol}$ in this stage is

$$g_{m,tol}=\frac{g_{mn}}{1+j\omega L_{S1}g_{mn}}+\frac{g_{mp}}{1+j\omega L_{S2}g_{mp}}. \tag{5}$$

The voltage gain $A_{V1}$ of the first stage LNA shown in Fig. 3 is

$$A_{V1}\approx g_{m,tol}\left[(1+j\omega L_{S1}g_{mn})\,R_{on} /\!/ \left(1+j\omega L_{S2}g_{mp}\right)R_{op} /\!/ Z_{in2}\right]. \tag{6}$$

From Fig. 3, using the small signal equivalent circuit analysis, it can calculate the input impedance $Z_{in}$ as

$$Z_{in}\approx j\omega L_1+Z_{sd} /\!/ Z_{fb}, \tag{7}$$

and

$$Z_{sd}=\left(j\omega L_{S1}+\frac{1}{j\omega C_{gsn}}+\frac{g_{mn}L_{S1}}{C_{gsn}}\right) /\!/ \left(j\omega L_{S2}+\frac{1}{j\omega C_{gsp}}+\frac{g_{mp}L_{S2}}{C_{gsp}}\right), \tag{8}$$

$$Z_{fb}=\left\{R_F+\left[(1+j\omega L_{S1}g_{mn})\,R_{on} /\!/ \left(1+j\omega L_{S2}g_{mp}\right)R_{op}\right]\right\} \times\left\{1+g_{m,tol}\left[(1+j\omega L_{S1}g_{mn})\,R_{on} /\!/ \left(1+j\omega L_{S2}g_{mp}\right)R_{op} /\!/ Z_{in2}\right]\right\}^{-1}, \tag{9}$$

where $\omega$ is the operation frequency, $R_{on}$ and $R_{op}$ are the output resistances of MN and MP, respectively, $Z_{sd}$ is the input impedance from the dual source inductive degeneration technique, and $Z_{fb}$ is the input impedance from the shunt feedback technique (which can be derived as Eq. (3)). Meanwhile, the total noise figure of the proposed two-stage amplifier in Fig. 2 is dominated by the first stage. The NF of the second stage contributed from the common source amplifier (M1, $R_1$ and $L_3$) is reduced by the gain of the first stage. In the proposed LNA topology, the use of dual inductive degeneration through $L_{S1}$ and $L_{S2}$ with current reuse configuration is also beneficial to low noise design. Based on the methodology in Ref. [11], simultaneous input impedance and noise matching over the 3.1–10.6 GHz band of interest can be achieved by appropriately selecting the values of $L_1$, $L_{S1}$, $L_{S2}$, $R_F$ and the size of transistor MN (MP). In this design, the inductors $L_1$, $L_{S1}$ and $L_{S2}$ are chosen to be the same as 0.45 nH, the feedback resistor $R_F$ is chosen as 900 Ω and the width of MN (MP) is set to 160 $\mu$m.

Because of the influence of parasitic capacitors from the two-stage amplifier, the gain performance of the ultra-wideband LNA degrades at high frequency, and an inter-stage peaking inductor $L_2$ is inserted between the first stage and the second stage to isolate the parasitic capacitances from each other to enhance the gain bandwidth[12]. As can be seen in Fig. 3, $L_2$, $C_{\mathrm{gd,\,eq}}$ of current reuse topology (MN and MP), and $C_{\mathrm{gk}}$ of M1 form a broadband $\pi$ section LC network. Here, the capacitor $C_{\mathrm{gd,\,eq}}$ stands for the output Miller capacitance of MN and MP, which is equal to $(C_{\mathrm{gdn}} + C_{\mathrm{gdp}})(1 + 1/A_{\mathrm{V1}})$, and the capacitor $C_{\mathrm{gk}}$ represents the sums of the gate source capacitance $C_{\mathrm{gs1}}$ and the input Miller capacitance of $C_{\mathrm{gd1}}$. Proper choice of inductor $L_2$ can resonate with the parasitic capacitors that create gain peaking to compensate for the high frequency gain roll-off of the devices, achieving the best flatness gain of the LNA. The simulated optimal value of $L_2$ can be obtained to get high flat gain and bandwidth response, and the value of $L_2$ is chosen as 1.0 nH.

In the second stage of the ultra-wideband LNA, a common source amplifier (M1, $R_1$ and $L_3$) is designed for further signal amplification and a shunt peaking inductor $L_3$ is added to extend the –3 dB bandwidth. Due to the parasitic capacitor at the drain of M3, the impedance at this node is reduced with increasing operating frequency. Because the impedance of the inductor increases with increasing frequency, the peaking inductor $L_3$ is adopted as the load of the second stage to compensate for the influence of the parasitic capacitor. The load resistor $R_1$ is designed to achieve flat gain over the whole bandwidth, which can be added to increase the low frequency gain. By optimizing the size of $L_3$ and $R_1$, the second stage compensates for the gain roll-off of the first stage at high frequency and also provides good flatness over the frequency band of interest. In this design, the width of M1 is set to 80 $\mu$m, the inductor $L_3$ is chosen as 1.92 nH and the resistor $R_1$ is chosen as 40 Ω.

In addition, two capacitors $C_{\mathrm{bp}}$ (40 pF and 10 pF) are the on-chip filtering capacitors to lower the noise induced by the supply voltage, which can be used to maintain a constant bounce between $V_{\mathrm{CC}}$ and ground. On-chip capacitors ($C_1$, $C_2$) are used as the DC-blocking capacitors to isolate the input and output port from the DC source. The source follower has been added as an output buffer and provides the required wideband output impedance to drive the 50 Ω input port of the network analyzer. The output buffer is only for measurement purposes and is not required later on for the completely integrated UWB receiver. The wideband output impedance $Z_{\mathrm{out}}$ is given as[13]

$$\begin{aligned} Z_{\mathrm{out}} &= \frac{1 + \mathrm{j}\omega Z'(\omega) C_{\mathrm{gs3}}}{g_{\mathrm{m3}} + \mathrm{j}\omega C_{\mathrm{gs3}}} // r_{\mathrm{o3}} // r_{\mathrm{o4}} \\ &\approx \frac{1 + \mathrm{j}\omega Z'(\omega) C_{\mathrm{gs3}}}{g_{\mathrm{m3}} + \mathrm{j}\omega C_{\mathrm{gs3}}}, \end{aligned} \tag{10}$$

where $Z'(\omega)$ is the impedance of the LC tank formed by $L_3$ with $C_{\mathrm{gd1}} + C_{\mathrm{gd3}}$. Equation (10) shows that the parasitic capacitance of M3 severs as the output load of the ultra-wideband LNA, and a smaller $C_{\mathrm{gs3}}$ is desired to minimize the degradation, thus the width of M3 is set to only 80 $\mu$m and the width of M4 is the same as M3. The source follower is biased by means of a current mirror. To minimize the power consumption, the resistor $R_2$ is chosen as 900 Ω and the width of M2 is set to 24 $\mu$m.

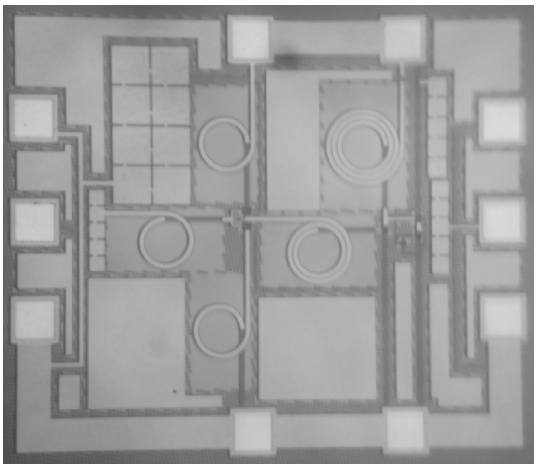

Fig. 4. Photomicrograph of the fabricated UWB LNA.

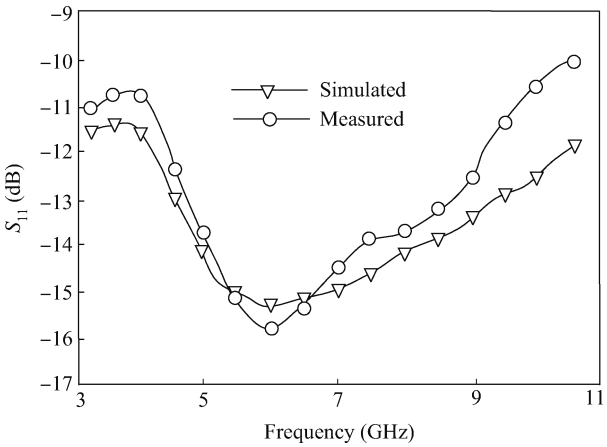


Fig. 5. Measured and simulated input return loss $S_{11}$ of the LNA.

## 3. Measurement results

The proposed ultra-wideband LNA is fabricated by chartered 0.18 $\mu$m single-poly six-metal CMOS technology. All of the components in this design, including spiral inductors and metal-insulator-metal (MIM) capacitors, are on-chip implemented. A micrograph of the fabricated UWB LNA is shown in Fig. 4. The die size of the test chip is $0.8 \times 0.9$ mm$^2$, including testing pads. The testing board has been built by directly bonding the die on a two-layer F4B substrate. The F4B PCB board was manufactured with just microstrip lines and microwave boarding techniques, such as a separated ground filled area. From the supply voltage of 1.5 V, the power consumption of the UWB LNA is 14.1 mW, including the output buffer stage.

Figure 5 presents the measured and simulated input reflection coefficients. As can be seen, the well-matched $S_{11}$ demonstrates a successful design of the resistive current reuse along with dual inductive degeneration techniques as the input matching network. The measured $S_{11}$ is lower than –10 dB over the 3.1–10.6 GHz band of interest. The measured and simulated output reflection coefficients are shown in Fig. 6. The

Table 1. Performance summary of the proposed UWB LNA and comparison with other published work.

| Specification | Ref. [2] | Ref. [4] | Ref. [8] | Ref. [13] | This work |
|---|---|---|---|---|---|
| Technology | 0.18 $\mu$m CMOS | 0.35 $\mu$m SiGe BiCMOS | 0.18 $\mu$m CMOS | 0.18 $\mu$m CMOS | 0.18 $\mu$m CMOS |
| Frequency (GHz) | 3.1–10.6 | 1.6–12.1 | 3.1–10.6 | 3.1–10.6 | 3.1–10.6 |
| Input return loss $S_{11}$ (dB) | < –9.7 | < –8 | < –9.7 | < –9 | < –10 |
| Output return loss $S_{22}$ (dB) | < –8.4 | < –8 | — | < –13 | < –10.5 |
| Power gain (dB) | 11.4 | 12 | 9.2 | 17.5 | 15.6 |
| Reverse isolation $S_{12}$ (dB) | < –40 | < –30 | — | — | < –45 |
| Supply voltage (V) | 1.9 | 0.8 | 1.0 | 1.8 | 1.5 |
| Noise figure (dB) | 4.12–5.16 | < 6.5 | 4.1–7.0 | 3.1–5.7 | 2.8–4.7 |
| IIP3 @ 6 GHz (dBm) | 0.72 | –10* | 7.25 | — | –7.1 |
| Power dissipation (mW) | 22.7 | 6.4 | 23.5 | 33.2 | 14.1 |
| Die size (mm$^2$) | 0.6 × 0.7 | 1.0 × 1.4 | 0.8 × 1.0 | 0.7 × 0.7 | 0.8 × 0.9 |

* At 10 GHz

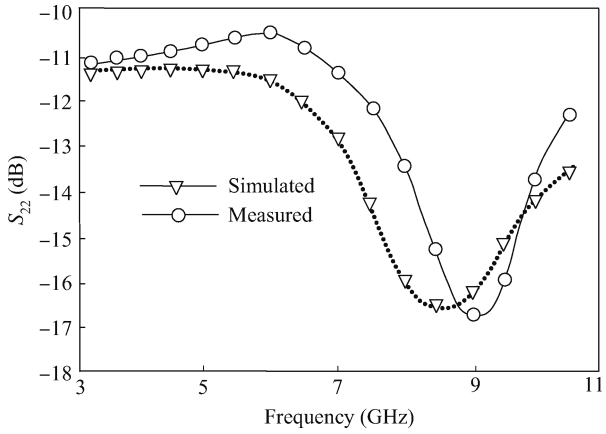


Fig. 6. Measured and simulated output return loss $S_{22}$ of the LNA.

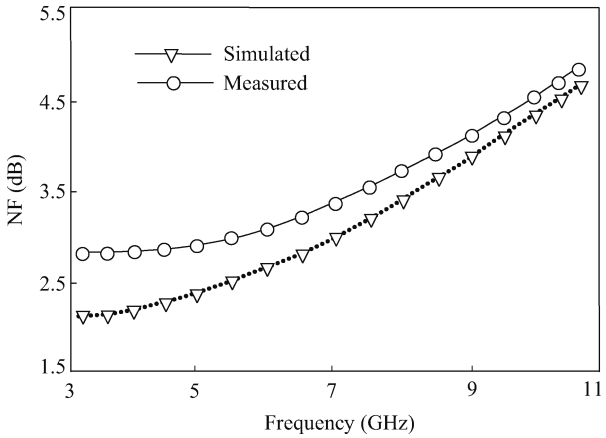


Fig. 8. Measured and simulated noise figures of the LNA.

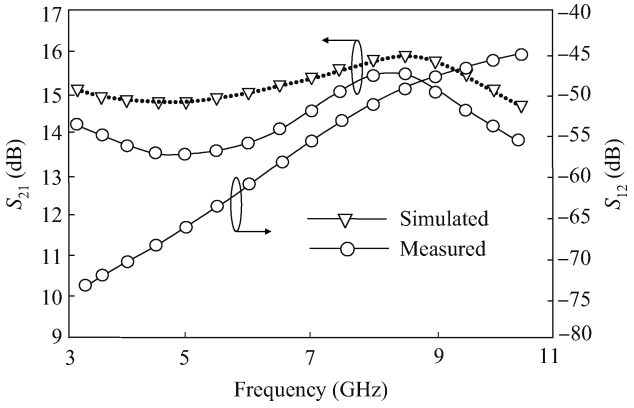


Fig. 7. Measured and simulated power gain and reverse isolation.

measured $S_{22}$ is approximately less than –10.5 dB in the full band. The degradation of measured $S_{11}$ and $S_{22}$, compared to the simulation, is presumably caused by the improper modelling of the inductors and the parasitic capacitance of the input/output testing pads.

The simulated and measured power gain characteristics are shown in Fig. 7. The measured $S_{21}$ shows a maximum power gain of 15.6 dB with the –3 dB bandwidth from 3.1 to 10.6 GHz. The full-band gain flatness is about ± 1.0 dB. Moreover, the gain flatness in every band group is less than ± 0.5 dB except for band group three, in which the gain flatness is ± 0.78 dB. The curve shape of the measured $S_{21}$ is similar to that of the simulated $S_{21}$. Figure 7 also shows the measured reverse isolation $S_{12}$ against frequency characteristics of the ultra-wideband LNA. The reverse isolation $S_{12}$ is below –45 dB within the required bandwidth.

As far as noise is concerned, Figure 8 compares both the measured and the simulated noise figure. The measured result shows an excellent noise performance of 2.8–4.7 dB in the frequency range of 3.1–10.6 GHz. The measured noise figure is a little larger than simulated, which probably results from parasitic elements of the chip, or the substrate loss, or the inaccurate noise model of the transistor. The parasitic effect related to the substrate in CMOS circuits is not negligible because it will induce the degradation of performance at high frequency.

To observe the non-linear behavior, the two-tone signals with equal power levels at 6 GHz and 6.1 GHz are applied to the ultra-wideband LNA. The measurement results indicate that the LNA has an input-referred third-order intercept point (IIP3) of –7.1 dBm and an input 1 dB compression point ($P_{1\text{dB-in}}$) of –16.5 dBm (not shown here). These results show that the ultra-wideband LNA achieves enough linearity. Circuit performance is summarized and listed in Table 1 and compared with that of prior references. As can be seen, compared with other work, the proposed ultra-wideband LNA exhibits a high flat power gain and a good noise figure, and it also has a small chip area and a low power consumption.

## 4. Conclusion

In this paper, a novel ultra-wideband LNA configuration is reported by applying an improved current reuse structure. From a combination of dual inductive degeneration and shunt inductive peaking techniques, the current reuse topology proposed in narrow-band LNA designs has been successfully extended to UWB applications. Fabricated by a 0.18 $\mu$m RFCMOS process, the implemented two-stage ultra-wideband LNA can provide higher power gain, wideband input matching and lower noise simultaneously. The measurement results show a maximum power gain of 15.6 dB, higher than 10 dB of input and output return losses, and a noise figure of 2.8–4.7 dB in the frequency range of 3.1–10.6 GHz while dissipating 14.1 mW under a supply voltage of 1.5 V. The excellent results have shown that the proposed LNA is suited to the UWB system applications.

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