A low-voltage low-power CMOS voltage reference based on subthreshold MOSFETs

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Abstract: This paper describes a CMOS voltage reference using only resistors and transistors working in weak inversion, without the need for any bipolar transistors. The voltage reference is designed and fabricated by a 0.18 μm CMOS process. The experimental results show that the proposed voltage reference has a temperature coefficient of 370 ppm/℃ at a 0.8 V supply voltage over the temperature range of –35 to 85 ℃ and a 0.1% variation in supply voltage from 0.8 to 3 V. Furthermore, the supply current is only 1.5 μA at 0.8 V supply voltage.

Key words: bandgap reference; CMOS; subthreshold
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1. Introduction

A precision voltage reference circuit is very important in the design of many mixed-signal and analog integrated circuits, such as oscillators, comparators, low-dropout regulators (LDOs) and data converters. The voltage references are required to be stabilized over process, voltage, and temperature variations and are also expected to be implemented in the standard fabrication process.

Undoubtedly, a bandgap voltage reference, which was firstly proposed by Widlar[1] and was further developed by Kuijk[2], is the most popular high performance voltage reference used in integrated circuits today. Moreover, the bandgap references that are less than 1 V are used more and more in low voltage applications. Therefore, many researchers have also developed bandgap voltage references that are less than 1 V. Banba and Leung[3,4] proposed two bandgap voltage references. The concept is basically a current-mode method to scale down the bandgap reference voltage by a factor defined by a resistor ratio. Jiang[5] proposed a bandgap reference using a transimpedence amplifier. However, all of the above bandgap voltage references require big area diodes or parasitic bipolar junction transistors (BJTs). In this paper, we introduce a new low-voltage low-power voltage reference based on subthreshold MOSFETs. The proposed bandgap voltage reference can operate from a supply as low as 0.8 V and the supply current is only 1.5 μA.

2. Conventional bandgap voltage reference

Figure 1 shows the structure of the conventional bandgap reference. M1 and M2 have the same transistor size. The input voltages of the error amplifier, V_c and V_d, are controlled to keep the same voltage and there is $R_2 = R_3$.

So the voltage across the resistor R_1, which is the forward voltage difference between the two bipolar transistors Q_1 and Q_2, can be shown as

$$\Delta V_{be} = V_{be2} - V_{be1} = V_t \ln N. \quad (1)$$

The output reference voltage V_{ref} can be expressed as

$$V_{ref} = V_{be2} + \frac{R_3}{R_1} V_t \ln N. \quad (2)$$

Here, N is the emitter area ratio and V_t is the thermal voltage. The $V_t \ln(N) R_3/R_1$ term is proportional to the absolute

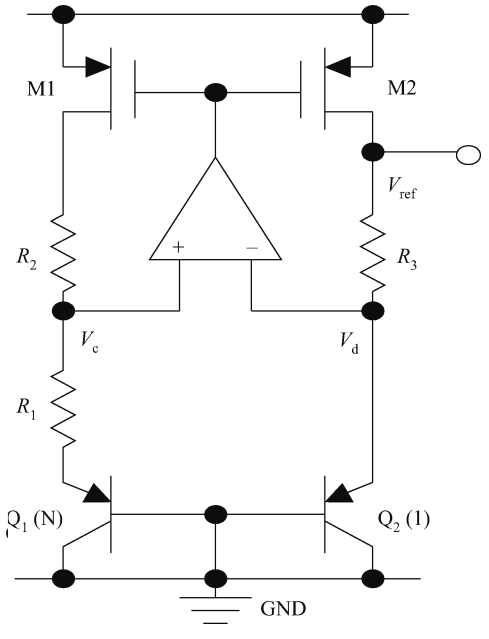

Fig. 1. The conventional bandgap reference circuit.

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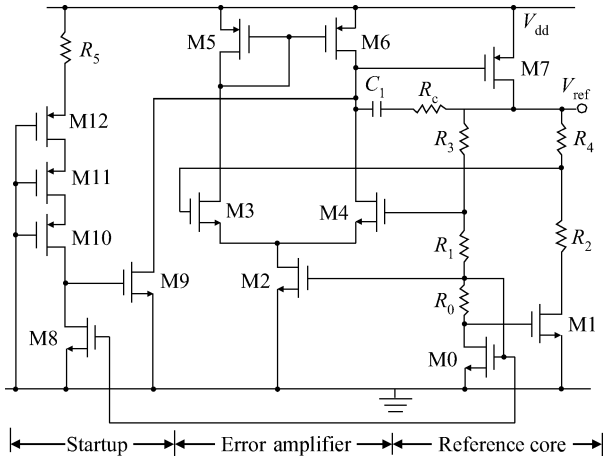

Fig. 2. Structure of the proposed bandgap reference.

temperature (PTAT), which is used to cancel the negative temperature coefficient of V_{be}. Therefore, we can choose a proper ratio of resistors to obtain an output reference voltage with low temperature coefficient.

3. Circuit design of the proposed bandgap voltage reference

Recently, a study of the MOSFET temperature behavior pointed out clearly that below a certain technology-dependent bias point, the gate–source voltage of a MOSFET, biased with a fixed drain current, decreases with temperature in a quasi-linear fashion[6, 7]. For the MOSFET operating in the weak-inversion region, with the condition of $V_{DS} \geqslant 3V_t$, its drain current can be given as

$$I_d = K\mu V_t^2 \sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\phi_s}} \exp\frac{V_{GS} - V_{TH} - V_{OFF}}{nV_t}, \quad (3)$$

where $K = W_{eff}/L_{eff}$ is the transistor aspect ratio, μ is the mobility of the carrier in the channel, ε_{si} is the permittivity of silicon, N_{ch} is the channel doping concentration, ϕ_s is the surface potential, n is the subthreshold slope factor, V_{OFF} is a corrective constant term used in BSIM3v3 models[8] and V_{TH} is the threshold voltage. Furthermore, for a given drain current, the relation between gate–source voltage V_{GS} and V_{TH} as a function of temperature is

$$V_{GS}(T) = V_{TH}(T) + V_{OFF} + \frac{n(T)}{n(T_0)} \times [V_{GS}(T_0) - V_{TH}(T_0) - V_{OFF}]\frac{T}{T_0}. \quad (4)$$

The threshold voltage, which has a negative temperature coefficient, can be expressed as[9]

$$\begin{aligned} V_{TH}(T) &= V_{TH}(T_0) + \alpha_{VT}(T - T_0) \\ &= V_{TH}(T_0) + \alpha_{VT}T_0\left(\frac{T}{T_0} - 1\right) \\ &= V_{TH}(T_0) + K_T\left(\frac{T}{T_0} - 1\right), \end{aligned} \quad (5)$$

where α_{VT} is the temperature coefficient of the threshold voltage and it is generally between –4 and –1 mV/℃. Assuming that $n(T)$ has small variations with temperature, we can get

$$V_{GS}(T) \approx V_{GS}(T_0) + [K_T + V_{GS}(T_0) - V_{TH}(T_0) - V_{OFF}]\left(\frac{T}{T_0} - 1\right). \quad (6)$$

From Eq. (6), we can see that V_{GS} decreases with temperature and has a similar temperature performance to V_{be}, so we can generate the reference voltage with the V_{GS} voltage instead of using the V_{be} voltage.

Figure 2 shows the complete schematic of the proposed voltage reference. The startup circuit is composed of M8–M12 and R_5. M2–M6 form the error amplifier. M0, M1 and R_0–R_4 are the core circuit, which can generate the reference voltage, and there is $R_3 = R_4$. C_1 and R_C are the compensation capacitor and resistor. From Eq. (3), the drain current of M0 and M1 can be expressed as

$$I_{d0} = K_0\mu_n V_t^2 \sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\phi_s}} \exp\frac{V_{GS0} - V_{TH} - V_{OFF}}{nV_t}, \quad (7)$$

$$I_{d1} = K_1\mu_n V_t^2 \sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\phi_s}} \exp\frac{V_{GS1} - V_{TH} - V_{OFF}}{nV_t}, \quad (8)$$

where $K_0 = W_0/L_0$, $K_1 = W_1/L_1$ and $K_1 = NK_0$. Because the current $I_{d0} = I_{d1}$, we have

$$V_{GS0} - V_{GS1} = nV_t \ln N. \quad (9)$$

From Fig. 2, we can see that

$$V_{GS0} = V_{GS1} + I_{d0}R_0. \quad (10)$$

From Eqs. (9) and (10), we have

$$I_{d0} = \frac{V_{GS0} - V_{GS1}}{R_0} = \frac{nV_t \ln N}{R_0}. \quad (11)$$

Then the voltage across the resistors R_1 and R_3 is

$$V_{R1} + V_{R3} = I_{d0}(R_1 + R_3) = \frac{R_1 + R_3}{R_0}nV_t \ln N, \quad (12)$$

where $(R_1 + R_3)/R_0$ is the temperature independent resistor ratio, so the voltage is proportional to the absolute temperature. From Eqs. (6) and (12), we can see that the expression for the reference voltage is

$$V_{ref} = V_{GS0} + V_{R1} + V_{R3} = V_{GS}(T_0) + [K_T + V_{GS}(T_0) - V_{TH}(T_0)]\left(\frac{T}{T_0} - 1\right) + \frac{R_1 + R_3}{R_0}nV_t \ln N. \quad (13)$$

So we can choose a proper resistor ratio of $(R_1 + R_3)/R_0$ to achieve the temperature compensation.

In the voltage reference proposed by Giustolisi[6], the voltage reference is generated by the V_{GS} of the MOS transistors working in the subthreshold region. The voltage reference proposed by Leung[10] is based on the ΔV_{GS} of a NMOS transistor

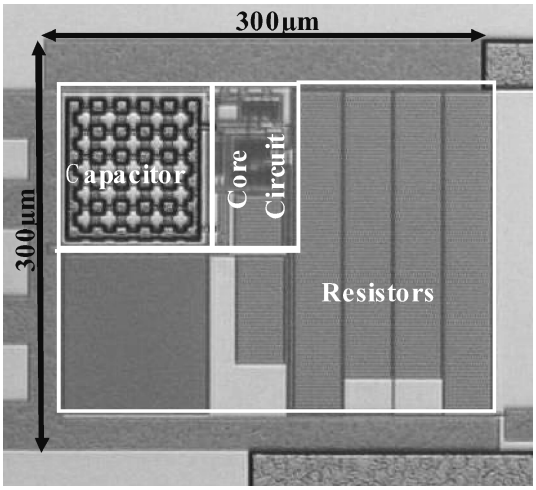

Fig. 3. Micrograph of the proposed bandgap reference.

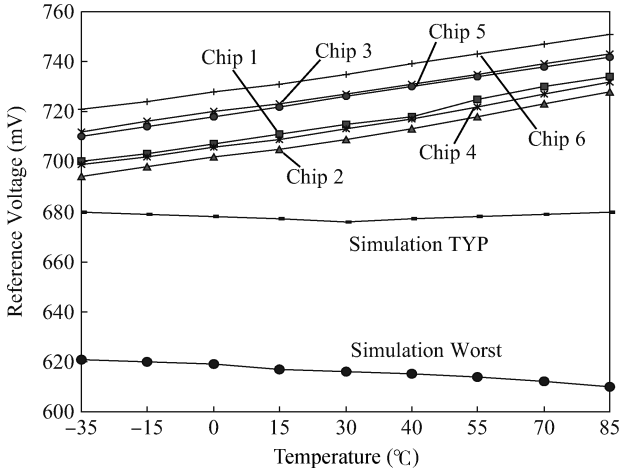

Fig. 4. Measured and simulated temperature dependence of the voltage reference.

and a PMOS transistor. In our design, we generated the voltage reference with the ΔV_{GS} of two NMOS transistors, which are working in the subthreshold region. Furthermore, an error amplifier is used to improve the performance of the voltage reference. As shown in Table 1, the PSRR and line regulation performance of the proposed voltage reference are much better than the voltage reference previously reported in the literature.

4. Experimental results

The proposed voltage reference is designed and fabricated by a 0.18 μm CMOS process, as shown in Fig. 3. The proposed circuit occupies a 0.09 mm^2 chip area. At room temperature, the supply current is 1.5 μA at a 0.8 V supply voltage. The chip area is very small and the supply current is extremely low due to the simple circuit structure.

As shown in Fig. 4, the measured temperature coefficients of the proposed reference circuit for 6 chips at a 0.8 V supply are about 370 ppm/℃, approximately 6 times the circuit simulation result at typical condition of 57 ppm/℃, and even more than twice that in the worst condition of 158 ppm/℃. Therefore, it can be seen that except for resistance mismatch or the

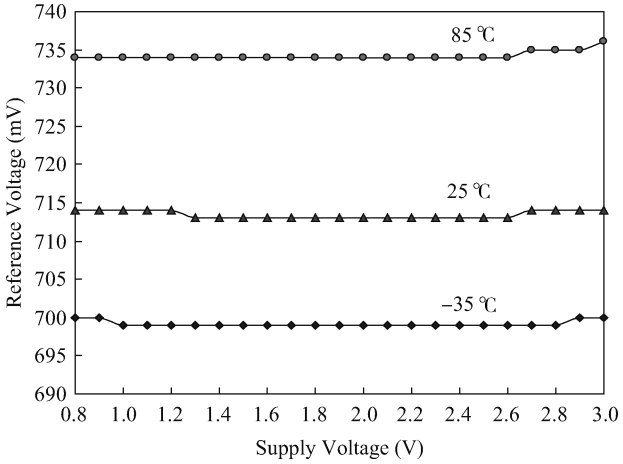

Fig. 5. Measured supply voltage dependence of the voltage reference at different temperatures of chip 1.

transistors' characteristic fluctuation possibly caused by process variations, another more important reason is that the simulation model is not so accurate as to agree rather well with experiment, especially for the transistors working in the weak inversion region. But fortunately, this inconsistency can be reduced by the adjustment of device sizes according to Eq. (3). A better temperature coefficient can be achieved by properly adjusting the resistance ratio of $(R_1 + R_3)/R_0$ in the circuit design or by using resistance trimming technology. Figure 5 shows the reference voltage dependence of the supply voltage, and the calculated line regulation is about 0.3 mV/V at room temperature for the supply voltage from 0.8 to 3 V.

The power-supply rejection ratio (PSRR) is used to measure the ability of signal suppression of a bandgap, and it is given by PSRR $= 20\lg|v_o(f)/v_{in}(f)|$, where $v_{in}(f)$ and $v_o(f)$ are the input signal and the output signal, respectively. The spectrum analyzer with a high input impedance ($R_{in} = 1$ MΩ) is used to measure the signal level at the input and output of the bandgap, and the input sine wave at the input of the bandgap is 0.1 V. The experimental results show that the PSRR is –67 dB @ 10 kHz at a 1 V supply voltage.

Table 1 summarizes the performance of the proposed voltage reference compared to the voltage reference previously reported in the literature and the conventional bandgap voltage reference based on the parasitic bipolar junction transistors.

5. Conclusion

In this paper, a low-voltage low-power CMOS voltage reference based on subthreshold MOSFETs has been introduced. It does not use any diodes or BJT. With a power supply voltage of 0.8 V, the proposed voltage reference circuit presents an output voltage of 700 mV with a temperature coefficient of 370 ppm/℃ over the temperature range of –35 to 85 ℃. The power supply current of the whole circuit is only 1.5 μA at room temperature. This circuit is suitable for low power, low voltage applications.

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Table 1. Comparison of the voltage reference available in the literature.

Parameter	Conventional[11]	Ref. [6]	Ref. [10]	This work
Technology (μm)	0.9	1.2	0.6	0.18
Supply voltage (V)	2.7–5.5	1.2–4	1.4–3	0.8–3
Supply current (μA)	300	3.6	9.7	1.5
Reference voltage (V)	1.236	0.3	0.310	0.7
Temperature coefficient (ppm/℃)	85	120	62	370*
PSRR (dB)	−80 @10 kHz	−40 @ 5 kHz	−47 @ 1 kHz	−67 @ 10 kHz
Line regulation (%/V)	—	—	0.225	0.036
Area (mm^2)	—	0.23	0.055	0.09
Year	1995	2003	2003	2010

* The temperature coefficient performance can be improved by the trimming procedure or by modifying the transistors sizes of M1 and M2.

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