A pseudo differential G_m–C complex filter with frequency tuning for IEEE802.15.4 applications*

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Abstract: This paper presents a CMOS G_m–C complex filter for a low-IF receiver of the IEEE802.15.4 standard. A pseudo differential OTA with reconfigurable common mode feedback and common mode feed-forward is proposed as well as the frequency tuning method based on a relaxation oscillator. A detailed analysis of non-ideality of the OTA and the frequency tuning method is elaborated. The analysis and measurement results have shown that the center frequency of the complex filter could be tuned accurately. The chip was fabricated in a standard 0.35 μm CMOS process, with a single 3.3 V power supply. The filter consumes 2.1 mA current, has a measured in-band group delay ripple of less than 0.16 μs and an IRR larger than 28 dB at 2 MHz apart, which could meet the requirements of the IEEE802.15.4 standard.

Key words: IEEE802.15.4 standard; complex filter; G_m–C filter; frequency tuning
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1. Introduction

Recently, with the rapid development of the CMOS process, more and more wireless communication systems are integrated on a single chip to reduce power consumption and costs. For high integration, zero-IF and low-IF structures are mainly adopted in receiver design, between which the zero-IF structure suffers from the problems of DC offset, flick noise and even-order distortion[1], especially in narrow band systems such as Bluetooth and IEEE802.15.4[2], in which the power of the signals centralized locate at the narrow band near the DC frequency[3]. Compared with zero-IF structure, the low-IF structure solves those problems but has less imagine rejection ratio (IRR)[4]. To intensively improve the IRR, a complex filter is widely used in low-IF receivers[5, 6].

There are two types of complex filters, namely passive RC complex filter and active complex filter. The former has the disadvantages of limited range of operating frequency and lossy gain, while the latter has the general virtues of low power dissipation, small chip area and high signal gain. However, an active RC filter cannot work at a higher frequency due to opamp frequency limitations, and the need for a much larger opamp bandwidth over the filter cut-off frequency leads to high power consumption[7]. To reduce the power consumption, G_m–C architecture with full differential OTA is commonly used, but it needs an additional common mode feedback (CMFB) circuit to fix the common mode potential at different high impedance nodes and suppress the common mode signal, which introduces excess power consumption and stability problems. Meanwhile, the input dynamic range of a full differential OTA is limited because of the tail current source.

To accurately tune the center frequency is the major challenge for a high precision complex filter realization. The majority of the reported frequency tuning circuits adopt phase lock loop (PLL)[8] or tunable capacitor and resistor topology[9], together with an envelope detection technique to cancel the mismatch in the process so as to optimize the performance of the filter. Conventional PLL based tuning maintains a high accuracy with the cost of complexity in circuit design, while the tuned passive component topology lacks accuracy due to the limitations of the process.

This paper presents a pseudo differential OTA topology and also a simplified tuning method for high dynamic input range G_m–C complex filter design. With the combination of configurable CMFB and a common mode feed-forward (CMFF) technique, the OTA has been proved by experiment with excellent performances in terms of both linearity and input dynamic range. The tuning method based on a relaxation oscillator has been validated with high tuning accuracy. Much detailed analysis of non-ideality about this OTA and tuning method is elaborated and the related methods for optimization as well. Such analysis results should facilitate analogous designs.

2. Complex filter basic

Different from the real filter, a complex filter could achieve asymmetrical amplitude and phase responses in the frequency domain, which could be explained easily by complex signal processing theory, as discussed in some of the literature[10]. For simplicity, assuming that the RF signal contains imagine part located symmetrical with the desired signal around the LO

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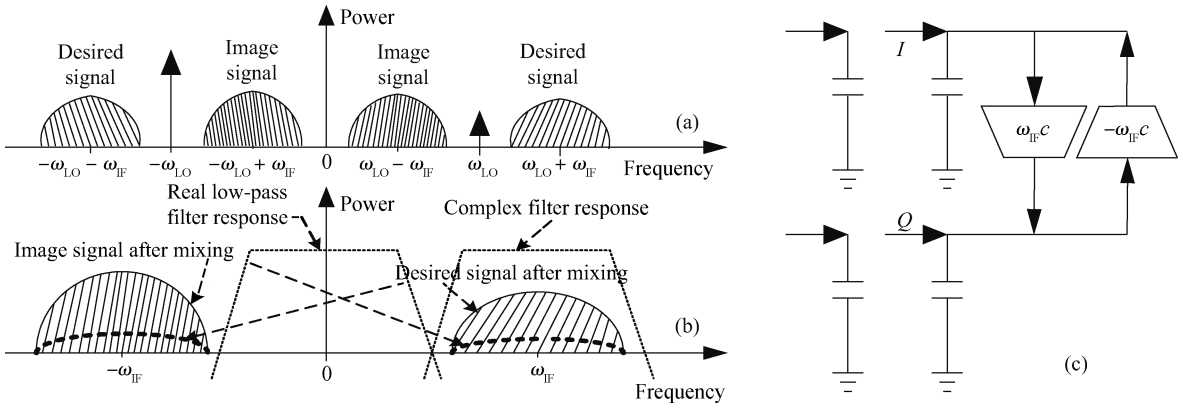

Fig. 1. (a) Before complex mixing. (b) After complex mixing. (c) Grounded capacitor in complex filter.

frequency, and the LO signal has the undesired part due to the mismatch of the I/Q path in an orthogonal receiver, as illustrated in Fig. 1(a). Thus, the desired signal at the mixer output will be destroyed by the imagine signal, as shown in Fig. 1(b), which requires a positive pass filter (PPF) or negative pass filter (NPF) to reject the undesired signal.

As depicted in Fig. 1(b), an obvious way to implement a PPF in a low-IF receiver is to use a real lowpass filter, by using $s - j\omega_{IF}$ to replace s in a Laplace transformation so as to translate the center frequency from zero to ω_{IF}. To realize asymmetrical responses in the frequency domain, additional components are needed in circuit implementation, to cross couple the real and imaginary signal paths, which use the same real lowpass filter. Figure 1(c) shows a schematic of the commonly used grounded capacitor in a complex filter, which is implemented by cross coupling transconductance with different signs, and results in admittance of $j(\omega - \omega_{IF})C$.

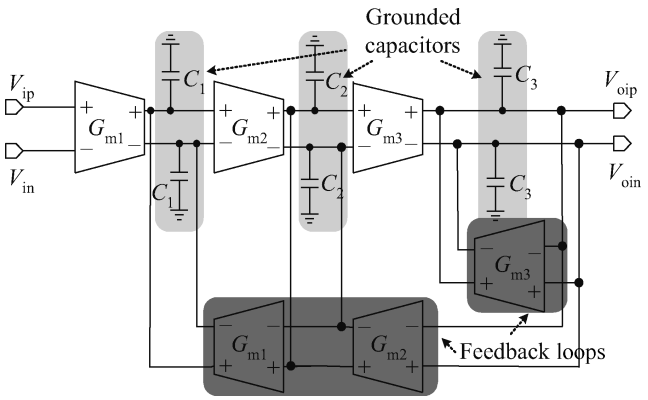

Fig. 2. Differential third-order Butterworth low-pass filter.

3. Filter architecture

Based on the requirements of the IEEE802.15.4 standard, which gives a jamming resistance of 0 dB rejection at the adjacent channel (2 MHz apart from the desired signal) and 30 dB rejection at the other channel, a third-order Butterworth complex filter with a corner frequency of 650 kHz is designed to meet the requirements with some margins. In order to minimize the component numbers, compared with other types, the multiple integrator loop feedback architecture[11] with the advantages of no floating capacitors and less sensitivity is chosen as the real lowpass filter prototype.

As shown in Fig. 2, the differential topology is chosen to achieve multiple feedback loops more conveniently than the single-ended type in a cascade design of a filter. Note that the whole complex filter in the low-IF receiver (PPF or NPF) can be implemented using two such low pass filters with grounded capacitors cross coupled, as shown in Fig. 1(c), which means that the frequency shift is only determined by cross coupled transconductance. Obviously, the transconductor plays a key role in this design. Its performances will limit the filter transfer characteristics, noise performance, linearity and power consumption. The accuracy of the center frequency is determined by the tuning method. Thus, in this work, we focus on the design of a transconductor and the center frequency tuning, respectively.

4. Proposed OTA architecture

Usually, the transconductor in a complex filter adopts a fully differential OTA to achieve good performance. In general, a fully differential structure has an improved dynamic range over its single-ended counterpart. This is due to the properties of any differential structure: better common mode noise rejection, better distortion performance, and increased output voltage swing[12]. However, the fully differential structure needs an extra CMFB circuit to fix the common mode potential at different high impedance nodes that are not stabilized by the negative differential feedback, and to suppress the common mode signal on the whole band of differential operation. The CMFB loop has to be designed carefully to avoid potential stability problems, which increases the design complexity, power consumption, and silicon area. Moreover, the frequency response of the differential path is also degraded due to the added parasitic components involved in conventional CMFB schemes.

Consider the aforementioned disadvantages of fully differential OTAs, and note that the node potential of cross coupled and feedback transconductors in the filter can be fixed by other transconductors, as shown in Fig. 2, in which only the transconductors in the main path (without darken) need CMFB. A pseudo differential transconductor with a configurable CMFB loop is proposed here. Compared with a fully

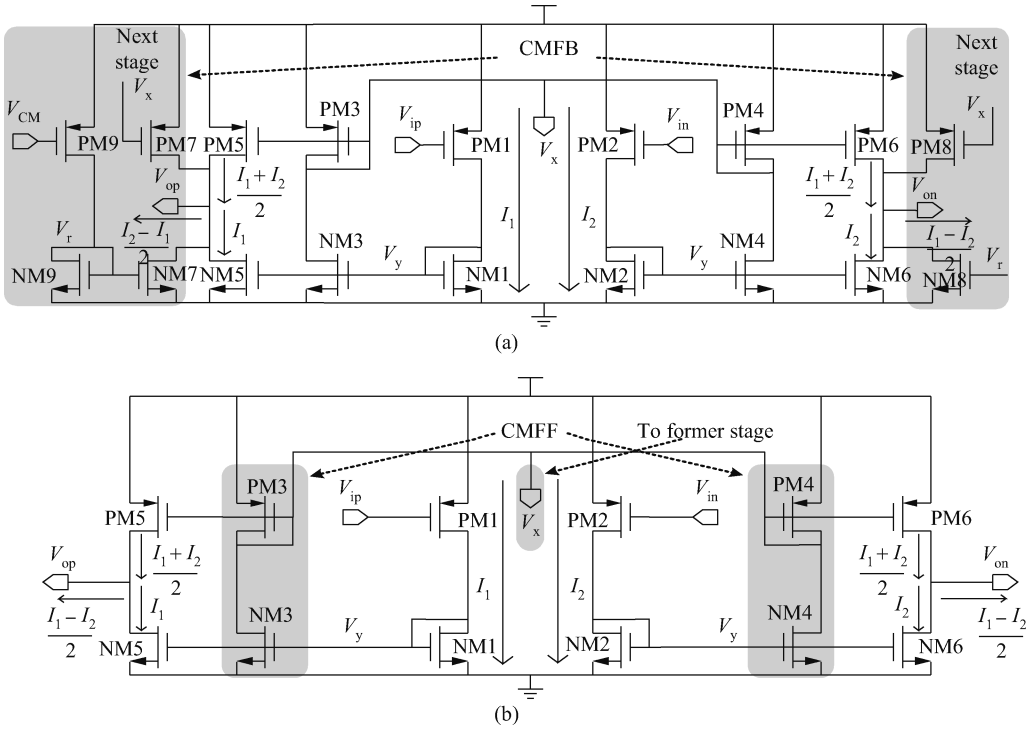

Fig. 3. Pseudo differential OTA structure (a) with CMFB and (b) without CMFB.

differential structure, the pseudo differential one can provide a larger input dynamic range and ease the stability problems. In Fig. 3(a), the normal transconductor has a CMFB loop consisting of PM7–PM9, NM7–NM9, while the OTA without CMFB is shown in Fig. 3(b).

To improve the rejection to common mode signal at the output, CMFF technique is adopted in this OTA. As illustrated in Fig. 3(b), the CMFF is provided by four transistors of NM3, NM4, PM3, and PM4. The current $I_1 + I_2$ contains the information of common mode level of the inputs $V_{\rm ICM}$ as follows (neglecting short channel effects),

$$I_1 + I_2 = K_{\rm p}(W/L)_1[(V_{\rm DD} - V_{\rm ICM} - |V_{\rm TP}|)^2 + 0.25V_{\rm d}^2]. \quad (1)$$

It should be noted that $(I_1 + I_2)/2$ is being mirrored to the output, yielding the desired extraction of the common mode information $V_{\rm ICM}$. Thus, the common mode current $(I_1 + I_2)/2$ is subtracted at the OTA output nodes. CMFF not only suppresses the common mode signal generated by this stage but also detects the common mode signal of the former stage and forms a CMFB loop to the former stage, as shown in Fig. 3(b), which makes it suitable in the cascade design of the complex filter.

Assuming PM3–PM6 have the same size, and as well as NM1–NM6, the differential gain of the OTA is extracted as

$$g_{\rm m} = g_{{\rm pm}_1}\frac{g_{{\rm nm}_1}}{g_{{\rm nm}_1} + sC_{\rm y}} = \frac{g_{{\rm pm}_1}}{1 + s/\omega_{\rm y}}, \quad (2)$$

where $C_{\rm y}$ is the total parasitic capacitors associated to node $V_{\rm y}$.

The CMFB loop gain can be expressed as

$$A_{\rm CMFB} = \frac{g_{{\rm pm}_1}}{g_{{\rm nm}_1} + sC_{\rm y}}\frac{g_{{\rm nm}_3}}{g_{{\rm pm}_3} + sC_{\rm x}}\frac{g_{{\rm pm}_7}}{g_{\rm o} + sC_{\rm L}}, \quad (3)$$

where $C_{\rm x}$ is the total parasitic capacitors associated to node $V_{\rm x}$, $g_{\rm o}$ is the output conductance of the OTA, and $C_{\rm L}$ is the load capacitor, which also compensates the stability of the OTA.

The CMFF gain is given by

$$A_{\rm CMFF} = \frac{g_{{\rm pm}_1}}{g_{{\rm nm}_1} + sC_{\rm y}}\frac{g_{{\rm nm}_3}}{g_{{\rm pm}_3} + sC_{\rm x}}. \quad (4)$$

The total common mode gain is thus derived as

$$A_{\rm CM} = \frac{A_{\rm CMFF}}{1 + A_{\rm CMFB}}. \quad (5)$$

Note that $A_{\rm CM}$, at low frequency, is much less than unity. This is a result of the actions of both CMFB and CMFF circuits. With this low common mode gain, the proposed OTA achieves a higher input dynamic range and good convenience in cascade design without the sacrifice of the common mode rejection ratio (CMRR).

Since the proposed OTA has an inherently common mode detector, the CMFB is efficiently implemented. With appropriate arrangement of cascaded pseudo differential OTAs, a separate CMFB circuit can be avoided; for instance, in a complex filter, the potential at the cross coupled node only needs one CMFB from the next stage to fix. This approach takes advantage of the OTAs used for differential mode operation to render high rejection for common mode signals without extra circuitry. So, the power consumption caused by the additional CMFB circuit as in the traditional OTA structure can be reduced.

An output common mode control voltage $V_{\rm CM}$ can be applied to tune the $g_{\rm m}$ of this OTA, as illustrated in Fig. 3(a). Also, each stage can be designed with the same input and output common mode level to ease the cascade conditions, which means that the biasing circuits of the OTA can be settled easily only by one extra control voltage from the tuning circuit. Thus, the tuning circuit only needs to give a common mode control voltage $V_{\rm CM}$.

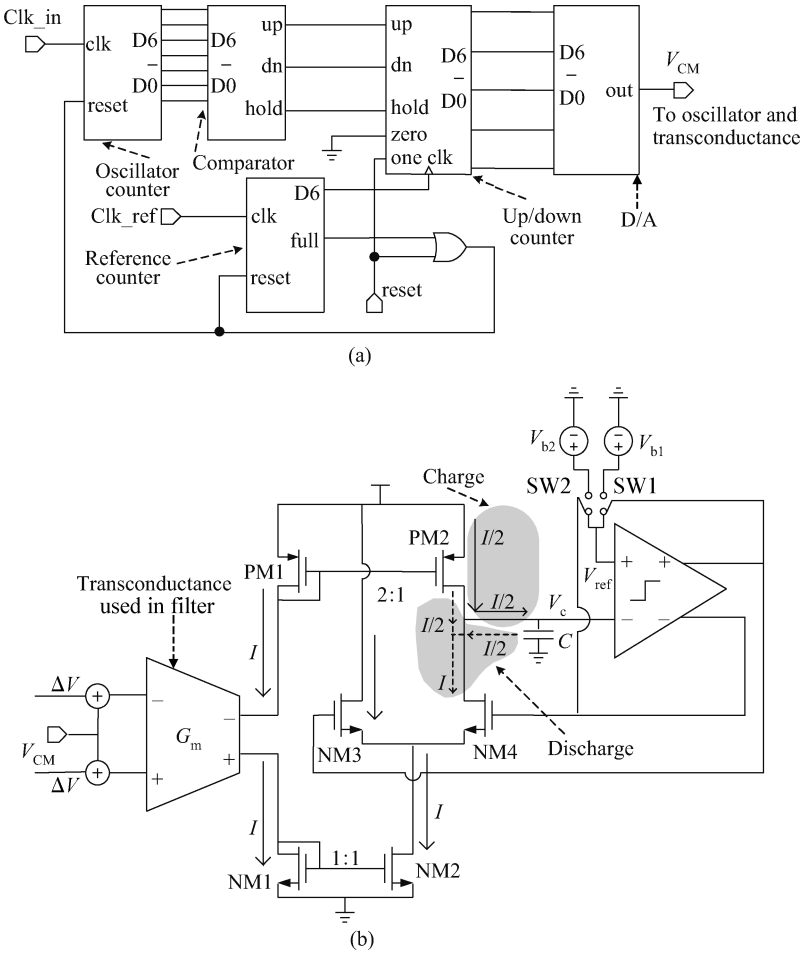

Fig. 4. (a) Frequency tuning method diagram. (b) Relaxation oscillator.

5. Frequency tuning

5.1. Tuning method diagram

The center frequency of the complex filter is always different from the designed value due to the process variations. Thus, a frequency tuning circuit is needed for compensation. The traditional frequency tuning methods are commonly based on the PLL technique, which is complex to design, though it has a high tuning accuracy. Moreover, the oscillator in the PLL has restricted conditions for initialization, which results in design complexity. To avoid the frequency pulling effect, the load capacitances of the integrator in the PLL and the filter vary a lot, which leads to a poor match, and results in degradation of the tuning accuracy. Another tuning method using the tuned passive components lacks accuracy due to the limitations of the process.

The tuning method proposed here consists of a relaxation oscillator, two counters to measure the oscillator and reference frequencies, a digital comparator, an up/down counter and a simple DAC, as shown in Fig. 4(a). The relaxation oscillator is based on the same OTA architecture used in the filter. Under nominal conditions, the frequency of the relaxation oscillator is equal to the desired reference center frequency (1 MHz).

The operation of the tuning circuit is described as follows. After system reset, the 7-bit reference and oscillator counters start counting until the reference counter reaches 64. At this moment, the up/down counter is clocked to count up or down, or held according to the output of the digital comparator, which compares the content of the oscillator counter with $D_{\rm ref} = 64$. The content of the 7-bit up/down counter is then converted to an analog voltage $V_{\rm CM}$ (via a 7-bit DAC) to control the frequency of the oscillator (by controlling the value of $g_{\rm m}$ through $V_{\rm CM}$, as shown in Fig. 4(b)). When the reference counter overflows (reaches 128), it sends a reset signal to the oscillator counter to begin a new frequency comparison cycle based on the updated oscillator frequency. Eventually, the oscillator frequency will reach the reference frequency within an error depending on the DAC resolution. The same control voltage $V_{\rm CM}$ is applied to the common mode control circuits to tune the frequency to the correct value. The 7-bit DAC is implemented using a resistive string to ensure monotonicity and, hence, stability of the tuning loops.

5.2. Relaxation oscillator

The relaxation oscillator, as shown in Fig. 4(b), consists of an OTA, two switches (SW1, SW2), two reference voltages ($V_{\rm b1}$, $V_{\rm b2}$), an integrating capacitor, and a fully differential comparator. The transconductance of the OTA is controlled by changing its common mode input level ($V_{\rm CM}$). By applying a constant differential voltage ΔV to the OTA, the output single-ended current will be given by

$$I = G_{\mathrm{m}}\Delta V. \tag{6}$$

This output current is mirrored to the tail current source (NM2) of a differential pair with an equal proportional ratio. Another output current is also mirrored but with a proportional ratio of 2 : 1 to a current source (PM2). The output current of the differential pair is determined by these two current sources and integrated on the capacitor C. The value of the output current is always $I/2$, but the polarity of that is controlled by the differential pair transistors. When NM4 turns off and NM3 turns on, the current from PM2 charges the capacitor, as shown in Fig. 4(b) by a solid arrow. In contrast, the capacitor is discharged with a current value of $I/2$, as shown in Fig. 4(b) by a dotted arrow.

The comparator compares the voltage on the capacitor (V_{c}) with the reference voltage, which is selected by switches between V_{b1} and V_{b2} (V_{b1} is larger than V_{b2}). The comparison results control the switches and determine which transistor (NM3 or NM4) is turned on. Thus, the voltage V_{c} is changed between V_{b2} and V_{b1}, forming a triangular signal with the corresponding slope of $G_{\mathrm{m}}\Delta V/2C$. The oscillation period including the charged and discharged cycle is calculated as follows,

$$\frac{I}{2}\frac{T}{2} = \frac{G_{\mathrm{m}}\Delta V}{2}\frac{T}{2} = (V_{\mathrm{b1}} - V_{\mathrm{b2}})C. \tag{7}$$

So, the oscillation frequency can be expressed as

$$f = \frac{1}{T} = \frac{G_{\mathrm{m}}}{4C}\frac{\Delta V}{V_{\mathrm{b1}} - V_{\mathrm{b2}}}. \tag{8}$$

A closer look at this equation indicates that the oscillation frequency is determined by the transconductance G_{m}, which is tuned by the common mode potential V_{CM}. Therefore, after tuning, a correct common mode potential V_{CM} will be given to the main filter to regulate the center frequency.

Apparently, the comparator used in this relaxation oscillator doesn't need to design with hysteresis. Assuming that V_{c} is larger than V_{b1}, the output of the comparator will control the switches to select the smaller reference voltage V_{b2}. Also during discharge, when V_{c} becomes smaller than V_{b2}, a higher reference voltage of V_{b1} is selected. Thus, the comparison results won't be corrupted by the small jitter as in a traditional comparator, because at the decision edge, once the decision is made, the reference voltage is changed simultaneously, which enlarges the difference between the two comparison input voltages.

6. Non-ideality analysis and optimization

6.1. OTA non-ideality analysis

The filter performance will be influenced by the non-ideality of the proposed OTA, including the finite input and output resistances and the parasitic capacitances and mismatches[13, 14]. As in the complex filter, the integrator is composed with OTA and C. The non-ideal integrator will modify the filter transfer function in terms of phase and amplitude.

The most bothersome modification is in phase with the transfer function of the integrator, which is ideally –90° at all frequencies. The finite output resistance causes the phase of the integrator at the unity-gain frequency larger than –90°, making an error in phase, namely the 'lead phase'. This deviation of the real G_{m}–C integrator from its ideal behavior may introduce significant distortions in the transfer function of G_{m}–C filters. The differential mode transconductance of this proposed OTA can be written as Eq. (2). Thus the 'lead phase' $\Delta\phi$ is given by

$$\Delta\phi = -\tan^{-1}\frac{\omega}{\omega_{\mathrm{y}}}. \tag{9}$$

Hence, the designed transconductance should have a high output resistance. To improve it, a cascode structure is commonly adopted[15], but this introduces another phase error problem, namely 'excess phase'. The transconductance of the OTA with a cascode structure has two poles. The lower one is caused by output impedance, while the other is caused by the inner node that always presents higher than unity-gain bandwidth. The presence of the higher pole makes the phase of the transfer function of the integrator at the unity-gain bandwidth smaller than –90°, for example, –94°, which also modifies the transfer function of the filter near the passband edge frequency, leading to distortion. Therefore, the cascode structure is not used in this OTA design, avoiding the above problem. Instead, long channel transistors are adopted to improve the output impedance.

Real transconductors have parasitic input and output capacitances associated with them. For low frequency applications, these parasitic capacitances are much smaller than the capacitances of the real capacitors used in filters to obtain their integrators. But for high frequency applications, the real capacitors are forced to be small to get the high filter poles that we need. Notice that the poles of a filter are given by expressions of the type g_{m}/C. So, to increase the pole frequency, we must decrease the capacitance or increase the transconductance g_{m}. However, higher g_{m} means larger input devices, which in turn mean larger parasitic input capacitances. At high frequency, we are also interested in increasing the output current capabilities of the transconductor to be able to charge the capacitors faster. However, again, more current capability of the output devices comes along with larger output devices, which means increased parasitic output capacitances.

At high frequency, these parasitic capacitances are no longer negligible compared with the real capacitors in the filter, if not taken properly into account, and will modify the transfer function of the filter significantly, changing the intended positions of the poles or, even worse, creating additional poles. One approach is to calculate these parasitic capacitances and take them into account in the final value of the capacitors that will be connected to the circuit. Another approach is to make all of the capacitances of all the nodes the same by construction, including parasitic capacitances, by adding appropriate dummy devices.

6.2. Tuning error analysis

The maximum error in this frequency tuning method depends on the accuracy of the DAC and relaxation oscillator. Assuming in the implementation of this 7-bit DAC, the resistive string has $\pm 10\%$ variation due to the process, which will introduce a maximum frequency error of $\pm 0.078\%$ for a 1 MHz center frequency. The accuracy of the relaxation oscillator is more complex, which is affected by various factors, including

Table 1. Performance parameters of the complex filter chip.

Parameter	Chen[9]	Teo[16]	This work
Filter type	3rd-order Butterworth	5th-order Bessel-Chebyshev	3rd-order Butterworth
Center frequency (MHz)	4.092	20	1
Tuning accuracy (%)	3	7	0.3
IIP3 (dBm)	19	–7	9
Group delay ripple (μs)	—	6	0.16
Noise (μVrms)	80	—	18.5
Power supply (V)	1.8	1.8	3.3
Current (mA)	2.6	6	2.1
Process (μm)	0.18	0.18	0.35

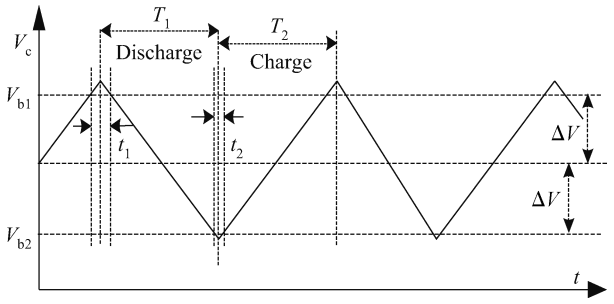

Fig. 5. Voltage variations during charge and discharge operation.

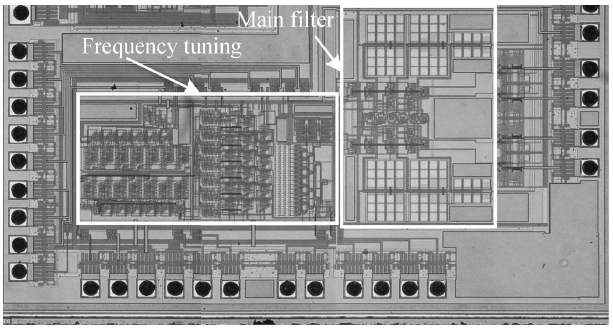

Fig. 6. Die micrograph of the fabricated complex filter.

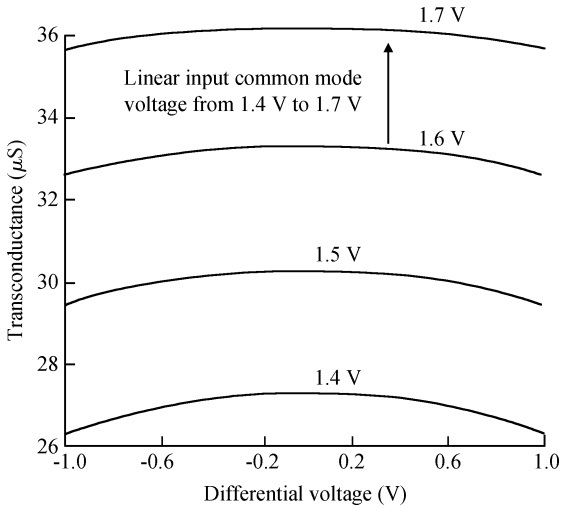

Fig. 7. Transconductance varies with differential voltage and common mode voltage.

comparator speed and delay time of digital circuits and also non-ideal switches.

Figure 5 shows the voltage on the charging capacitor during charge and discharge operation. At ideal operation, when charged to V_{b1}, V_c will be decreased because the charge operation changes to discharge operation by the switches immediately. In contrast, V_c starts to increase when discharged to V_{b2}. Clearly, we can see that when the switches are not ideal, and the comparator has limited speed, digital circuits have delay time, V_c will be charged to exceed V_{b1} and discharge to below V_{b2} until the operation has been switched. As shown in Fig. 5, t_1 and t_2 may be different and asymmetric due to the different delay, which results in a square wave without a 50% duty cycle, as shown in the measurement results. The delay time of the digital circuits is within several nanoseconds, and a corresponding maximum tuning error of $\pm 0.2\%$ is reasonable for 1 MHz center frequency. Charge injection and clock feed-through due to the non-ideal switches can be mitigated by using dummy transistors. Tuning accuracy will also be affected by the accuracy of $\Delta V/(V_{b1}-V_{b2})$, as in Eq. (8). If the voltages V_{b1}, V_{b2} and ΔV are obtained from the same resistive string of the DAC, a high accuracy can be achieved. Thus, this tuning method can obtain a total tuning accuracy within $\pm 0.3\%$, making only 3 kHz error in the filter center frequency, which is quite tolerable for the IEEE 802.15.4 standard.

7. Implementation and measurement results

According to the design optimization methods summarized in the previous sections, we have designed a CMOS complex filter for an IEEE802.15.4 low-IF receiver, in which the pseudo differential OTA and frequency tuning method are employed.

The complex filter chip was designed in a 0.35 μm 4-metal 2-poly n-well CMOS process. Figure 6 shows the die micrograph of the fabricated circuit. The circuit dissipates about 6.93 mW from a single 3.3 V supply. The performance parameters of the chip are summarized in Table 1, together with some other works for comparison. Chen has chosen a tunable capacitors and resistors scheme for frequency tuning, and the noise level is relatively high. Teo has adopted PLL schemes that show large power and poor tuning accuracy due to mismatch.

Figure 7 validates the transconductance of the proposed OTA versus the input differential voltages and common mode voltages. The output shows great linearity with linear common mode input voltages from 1.4 to 1.7 V, which should simplify

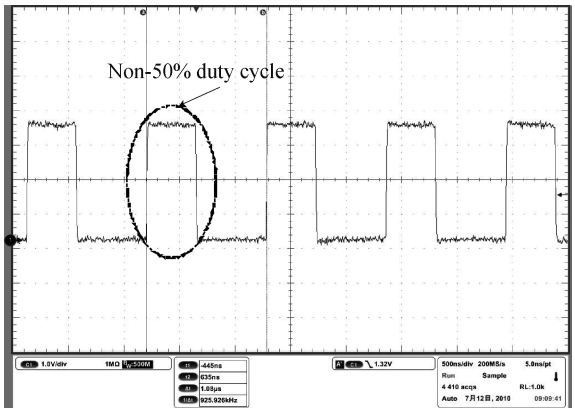

Fig. 8. Oscillator output of a square wave without a 50% duty cycle.

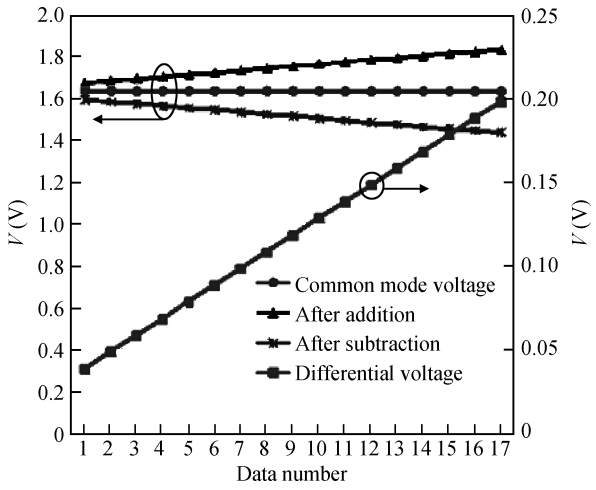

Fig. 9. Addition and subtraction of the common mode voltage and the differential voltage.

the design of the tuning circuits, such as the resistive string. Also, when the differential voltage varies from –1 to 1 V, the transconductance nearly keeps constant, which shows the large input dynamic range.

Figure 8 gives the output wave of the relaxation oscillator, which has a frequency of 1 MHz but a non-50% duty cycle. This curve validates the previous analysis of the non-ideality of the relaxation oscillator.

Figure 9 gives the addition and subtraction function of the common mode voltage and differential voltage in the input of the relaxation oscillator. When a 1.64 V DC voltage is applied as the common mode voltage, together with a linear differential input voltage from 0.04 to 0.2 V, the circuit exhibits a great linearity, as shown in the curve.

The transfer function of the complex filter is measured by a frequency spectrum analyzer. Normally, an S-parameter analyzer is needed to measure the negative frequency response, because the complex filter has an asymmetric response in the frequency domain. Thanks to the characteristics of the complex filter, the different phase sequence means a different frequency shift direction but the same filter transfer function. So, to measure the negative frequency response, the input 4-orthogonal phase should switch its sequences. For instance, a phase sequence (0°, –180°) and (–90°, –270°) of I/Q path individually

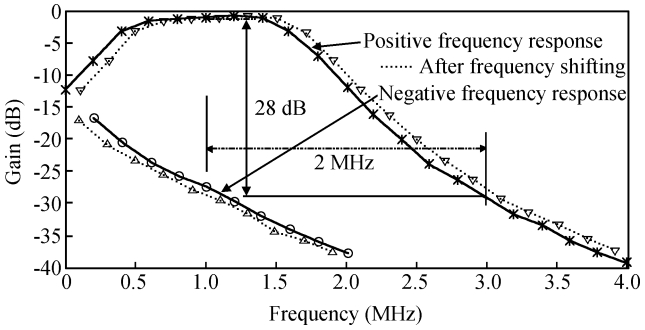

Fig. 10. Complex filter transfer function.

results in a positive frequency shifting, as in this design. Thus, for a 1 MHz center frequency, to measure the filter response at –1 MHz, which is 2 MHz apart from its center frequency, we can change the phase sequence to (0°, 180°) and (90°, 270°), then measure the response at 1 MHz, which is also 2 MHz apart from its current center frequency (–1 MHz).

A passive polyphase network is used to generate a 4-orthogonal signal. However, it only generates the same amplitude and the exact orthogonal phase at one frequency[17]. Considering the difficulty of generating a wideband orthogonal signal, we tune the passive R and C to generate an orthogonal signal with a space of 200 kHz in this test. Figure 10 shows an attenuation of 1 dB at the center frequency due to the finite output resistance of the transconductor and an image rejection ratio (IRR) larger than 28 dB at 2 MHz apart, which could meet the requirements of the IEEE802.15.4 standard. The solid line with '*' shows the positive response of the complex filter, while 'o' denotes the negative response, which is apparently asymmetric in the frequency domain. To verify the reliability of the tuning circuit, a common mode voltage is set different from the designed value and the chip is tested without the tuning circuit. The response as shown in Fig. 10 with a dotted line looks like a shift just from the solid line. This test validates that, if there are some variations in process (represented by the dotted line), the tuning circuit will tune the center frequency correctly to the designed value (represented in the solid line).

8. Conclusion

A CMOS third-order Butterworth complex filter for an IEEE802.15.4 low-IF receiver has been analyzed in terms of OTA non-ideality and tuning accuracy to identify the limiting factors, and then the optimized filter has been implemented. For the proposed pseudo differential OTA, the cascade design in filter has been effectively achieved by the inner CMFF and CMFB technique, and the design of a cross coupled transconductor is simplified. Long channel transistors are adopted to optimize the non-ideality of this OTA, which only results in a 1dB attenuation at the center frequency. The analysis also indicates that the delay and non-ideality switches are critical issues for the tuning accuracy. However, by using dummy switches and a high-speed comparator, the filter has shown great immunity to such non-ideality. The complex filter chip has been fabricated and measured. An IRR larger than 28 dB at 2 MHz apart is achieved and an in-band group delay ripple less than 0.16 μs, a tuning accuracy within 0.3% are also achieved, making

the complex filter meet the requirements of the IEEE802.15.4 low-IF receiver.

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