SPICE compatible analytical electron mobility model for biaxial strained-Si-MOSFETs

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Abstract: This paper describes an analytical model for bulk electron mobility in strained-Si layers as a function of strain. Phonon scattering, columbic scattering and surface roughness scattering are included to analyze the full mobility model. Analytical explicit calculations of all of the parameters to accurately estimate the electron mobility have been made. The results predict an increase in the electron mobility with the application of biaxial strain as also predicted from the basic theory of strain physics of metal oxide semiconductor (MOS) devices. The results have also been compared with numerically reported results and show good agreement.

Key words: mobility; SiGe; strained-Si; phonon; surface roughness; columbic
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1. Introduction

CMOS technology has contributed significantly to the microelectronics industry, thus playing an important role in the overall development of all of the countries. The performance and density of a CMOS chip can be improved through device scaling, which is inevitable as also propounded by Moore's law, which states that the transistor density of a CMOS chip doubles approximately after every one and a half years[1]. Continuing with Moore's law, the gate length of the MOSFET will eventually shrink to 10 nm in 2015[2]. Seeing the trend of down scaling, continuous improvements in VLSI MOSFET device models are required so that the exact behavior of deep submicron and nanometer scale MOSFETs can be described with accuracy. The reduction in carrier mobility is a major cause of drain current degradation. But as we scale down the MOSFET, carrier mobility decreases due to the high vertical electrical fields in the substrate. This reduces the speed of the device. To control these effects, strained silicon technology has evolved in the past few years as a replacement of silicon in substrate. An attempt has been made in this paper to analytically model the electron mobility. In detail, this paper deals with the physics of strained silicon MOSFET, presents the effect of strain on the silicon band structure, and gives some modeling issues in the strained silicon MOS technology.

2. Strain effect on mobility

When a layer of a crystal is grown over another layer, a strain is developed in the upper layer due to the mismatch of the lattice constants of two layers without decreasing the dimensions of the devices to achieve the high speeds without scaling down the devices. The strain is a very useful parameter in devices as carrier mobility significantly increases by altering the band structure at the channel. The alteration of band structure in the channel layer provides lower effective mass and also suppresses intervalley scattering, which is a prime cause of enhancement of carrier mobility and the drive current. The mobility becomes roughly twice that of conventional Si substrate[3]. The conduction band splitting has been shown in Fig. 1. Each energy level of silicon is composed of six energy states in three dimensions. These are named as two perpendicular Δ_2 states and four Δ_4 states parallel to the plane. When stress is applied, the Δ_2 states and Δ_4 states are split up into lower and higher energy states. This band alteration gives an alternative lower site for electrons to reside in, i.e. Δ_4. The difference in the energy levels causes repopulation of the electrons. The effective mass of electrons in the lower energy states is less than the higher states. Due to this, the electron mobility increases. Besides this, the inter-valley phonon scattering between the lower and upper states is suppressed due to the strain induced larger energy difference. The mathematical equation (1) proves this theory. Mathematically, carrier mobility is

$$\mu = q\tau/m^*, \tag{1}$$

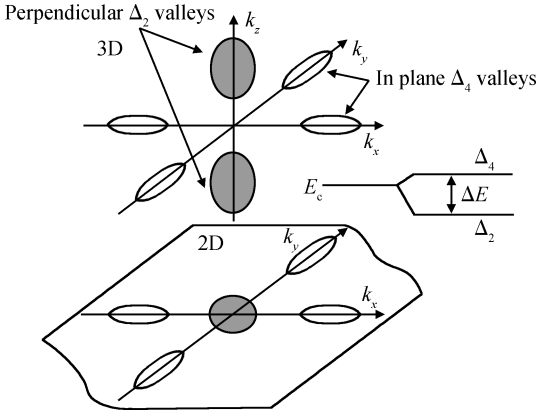

Fig. 1. Energy band splitting due to biaxial strain in conduction bands.

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where $1/\tau$ = scattering rate and m^* = conductivity effective mass. The mobility is directly related to the carrier velocity v and applied external electric field E, as shown by

$$v = \mu E. \tag{2}$$

It can be seen that increasing the carrier mobility increases the velocity, which is directly proportional to the switching speed of the device and the drain current. This process is especially useful at nanometer scales where the carrier mobility is affected the most, as explained in Section 1.

3. Modeling of electron mobility

Electron mobility is a very important parameter in the overall MOSFET modeling process. This is because parameters like drain current and hence trans-conductance strongly depend on mobility. There are three major scattering mechanisms that affect a MOSFET's inversion layer carrier mobility, as given below.

3.1. Phonon scattering due to lattice vibrations

Phonon scattering is due to lattice vibrations. The scattering rate is found from the calculations carried out using the deformation potential, as reported in Ref. [5]. The main problem is calculation of the electrical field at the oxide/silicon interface. The phonon scattering is evaluated as

$$\mu_{\rm ph}^{-1} = (\mu_{\rm pho}\beta^{-1})\left[1 + (E_{\rm s}/E_{\rm o})^{0.2\alpha}\right], \tag{3}$$

where $\beta = 1 + a_1\{1 + (0.4a_1)^{b_1}\}^{-1/b_1}$, $\alpha = 1 + a_2\{1 + (1.1a_2)^{b_2}\}^{-1/b_2}$. $\mu_{\rm pho} = 1470\ {\rm cm^2/(V{\cdot}s)}$, $E_{\rm o} = 7 \times 10^4$ V/cm, $a_1 = 11, b_1 = 15, a_2 = 3, b_2 = 25$ are the constants as obtained from Ref. [5]. $E_{\rm s}$ = effective vertical electrical field from the substrate to the oxide.

3.2. Surface roughness scattering due to the microscopic roughness of the Si–SiO_2 interface

The microscopic roughness at the surface of the oxide/silicon interface causes a decrease in electron mobility due to scattering from the surface. Moreover, the electrical fields increasing due to the massive downscaling of the technology tend to pull the electrons towards the interface further. The empirical formula for the surface roughness of Ref. [5] is

$$\mu_{\rm sr} = \delta \times 10^{14}/E_{\rm s}^2, \tag{4}$$

where $\delta = \delta_o + a_3\{1 + (a_3/\Delta\delta)^{b_3}\}^{-1/b_3}$, $\delta_{\rm o} = 3.8$, $a_3 = 7$, $\Delta\delta = 2.1$, $b_3 = 15$.

3.3. Coulomb scattering due to impurity scattering

The coulomb mobility is calculated as

$$\mu_{\rm c}^{-1} = qCN_{\rm a}/Q_{\rm inv}, \tag{5}$$

where $C = 46 \times 10^{-9}$ V/cm, $Q_{\rm inv}$ is the inversion charge density and $N_{\rm a}$ = doping concentration ($\rm cm^{-3}$).

The total mobility of the electrons is calculated as follows from Mathiessen's rule,

$$\mu_{\rm Total}^{-1} = \mu_{\rm ph}^{-1} + \mu_{\rm sr}^{-1} + \mu_{\rm c}^{-1}. \tag{6}$$

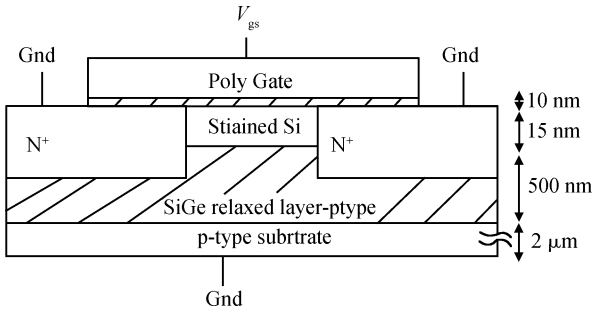

Fig. 2. Cross-sectional view of biaxially strained-Si–SiGe bulk-Si MOSFET.

4. Calculation of effective electrical field

There is no proper analytical solution of Eqs. (3)–(5) in the existing literature[5, 6]. This may be due to the analytical formulations of inversion charge density, depletion charge density and threshold voltage of biaxial strained MOSFETs seldom being available in the literature. In this paper, we have solved all of these equations analytically and no approximations have been used. The first parameter in solving these equations is the surface electrical field.

The total charge density in the substrate (due to both the inversion region and the depletion region) is given by Gauss's law,

$$E_{\rm s} = (\eta Q_{\rm inv} + Q_{\rm depl})/\varepsilon_{\rm Si}\varepsilon_0, \tag{7}$$

where $\eta = 0.75$, is the correction in inversion charge density in the (100) surface. $Q_{\rm inv}$ is the inversion charge density, $Q_{\rm depl}$ is the depletion charge density, $\varepsilon_{\rm Si}$ is the relative permittivity of silicon substrate, and ε_0 is the air permittivity.

4.1. Calculation of depletion charge density

The depletion charge density is given by

$$Q_{\rm depl} = qN_{\rm a}x_{\rm d}, \tag{8}$$

where $x_{\rm d}$ is the depletion width in the substrate. $x_{\rm d}$ is calculated as dividing the MOS substrate region in three parts, such as (1) p-type silicon/silicon germanium interface; (2) silicon germanium interface/strained silicon layer interface; and (3) strained silicon/oxide layer interface.

4.1.1. Hetero-interface I: p-type substrate and the SiGe relaxed layer p-type

Consider the MOSFET structure shown in Fig. 2. The depletion region extends in the p-type substrate and the SiGe relaxed layer. Let the thickness of SiGe relaxed layer be $x_{\rm SiGe}$ and the depletion region in the p-type substrate be $x_{\rm s}$. Applying the Poisson equation at this interface, for getting the potential distribution in the substrate and keeping substrate at zero bias, we get in the limits from $0 < x < x_{\rm d}$ towards the oxide,

$$\mathrm{d}^2\phi/\mathrm{d}x^2 = qN_{\rm a}/\varepsilon_{\rm o}\varepsilon_{\rm Si}. \tag{9}$$

Integrating Eq. (9) by applying boundary conditions, the electrical field at the interface I is given by

$$\mathrm{d}\phi/\mathrm{d}x = -E_{\mathrm{Si}} = qN_{\mathrm{a}}x_{\mathrm{d}}/\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{Si}}, \tag{10}$$

$$\phi_1(x) = qN_{\mathrm{a}}x^2/2\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{Si}}. \tag{11}$$

At $x = x_{\mathrm{d}}$,

$$\phi_1(x_{\mathrm{d}}) = qN_{\mathrm{a}}x_{\mathrm{d}}^2/2\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{Si}}, \tag{12}$$

is the potential at the substrate and SiGe relaxed layer hetero-interface. This can be called at the top of the substrate or at the bottom of the SiGe relaxed layer.

4.1.2. Hetero-interface II: SiGe relaxed layer p-type and p-type strained Si

The SiGe relaxed layer is assumed to be of constant electrical field and hence no depletion region exists in this area. The electrical field in the hetero interface I is the same as at the hetero interface II. The electrical field is given in Eq. (10). Solving Poisson equation in the SiGe relaxed layer. Integrating Eq. (10) in the SiGe channel, from $x = x_{\mathrm{d}}$ to $x = x_{\mathrm{d}} + x_{\mathrm{SiGe}}$, and putting boundary conditions for the potential ϕ_2, we get

$$\phi_2(x) - \phi_1(x_{\mathrm{d}}) = qN_{\mathrm{a}}x_{\mathrm{d}}x/\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{Si}}, \tag{13}$$

$$\phi_2(x_{\mathrm{SiGe}} + x_{\mathrm{d}}) = qN_{\mathrm{a}}x_{\mathrm{d}}^2/2\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{Si}} + qN_{\mathrm{a}}x_{\mathrm{d}}x_{\mathrm{SiGe}}/\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{Si}}.$$

4.1.3. Hetero-interface III: p-type strained Si and silicon oxide

The electrical field at the bottom of the strained silicon cap layer is the same as given by Eq. (10) due to the continuity of electrical fields at the hetero interface III. The electrical field at the strained silicon/oxide interface is calculated. Integrating Eq. (10) in the SiGe channel, from $x = x_{\mathrm{d}}$ to $x = x_{\mathrm{d}} + x_{\mathrm{SiGe}} + x_{\mathrm{ssi}}$, and putting boundary conditions for the potential ϕ_3, we get

$$\begin{aligned}\phi_{\mathrm{s}}(x) - \phi_1(x_{\mathrm{d}}) &= qN_{\mathrm{a}}x_{\mathrm{d}}x/\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{Si}},\\ \phi_{\mathrm{s}}(x_{\mathrm{d}} + x_{\mathrm{SiGe}} + x_{\mathrm{ssi}}) &= qN_{\mathrm{a}}x_{\mathrm{d}}x_{\mathrm{ssi}}/\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{Si}} + qN_{\mathrm{a}}x_{\mathrm{d}}^2/2\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{Si}}\\ &\quad + qN_{\mathrm{a}}x_{\mathrm{d}}x_{\mathrm{SiGe}}/\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{Si}}.\end{aligned} \tag{14}$$

Now, $\phi_3(x_{\mathrm{d}} + x_{\mathrm{SiGe}} + x_{\mathrm{ssi}})$ is the surface potential, which is constant and is equal to

$$\phi_{\mathrm{ss}} = 2\phi_{\mathrm{f}} - \Delta E_{\mathrm{C}}(x), \tag{15}$$

where $\Delta E_{\mathrm{C}}(x)$ is the conduction band offset due to strain in the lattice and ϕ_{f} is the Fermi potential, a parameter which is a function of doping. $\phi_{\mathrm{f}} = kT/q\ln(N_{\mathrm{a}}/n_{\mathrm{i}})$, where n_{i} is intrinsic carrier concentration, equals $(N_{\mathrm{c}}N_{\mathrm{v}})^{1/2}\exp(-E_{\mathrm{g}}/2kT)$. Using Eqs. (14) and (15) and solving the quadratic equation, we get the maximum depletion width in the substrate,

$$x_{\mathrm{d}} = -(x_{\mathrm{SiGe}} + x_{\mathrm{ssi}}) + \{(x_{\mathrm{SiGe}} + x_{\mathrm{ssi}})^2 + 2(\phi_{\mathrm{ss}}\varepsilon_{\mathrm{Si}}/qN_{\mathrm{a}})\}^{1/2}. \tag{16}$$

Using Eq. (16) in Eq. (8), we get the depletion charge density.

Table 1. Strained silicon MOSFET parameters used in simulation.

Parameter	Value
Germanium content in SiGe relaxed layer	0–0.4
Relaxed SiGe film thickness t_{SiGe}	0–15 nm
Source/Drain and poly silicon doping	2×10^{20} cm^{-3}
Substrate doping	5×10^{17} cm^{-3}
Gate oxide thickness	8.0 nm
Work function of gate material	4.35 eV
Strained silicon film thickness t_{si}	0–15 nm

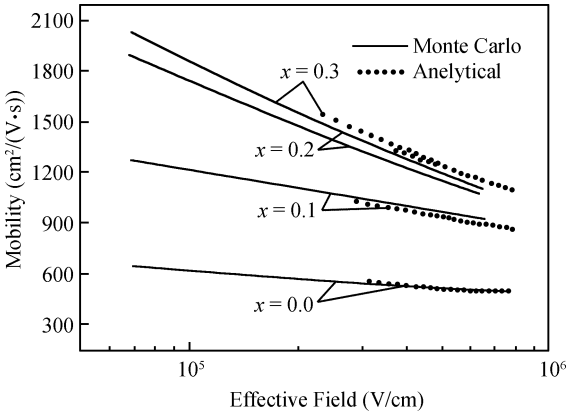

Fig. 3. Modeled results of electron phonon mobility with effective electrical field for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature. Reported results are shown by the black lines. Data calculated with the model developed in this paper are shown by the symbols.

4.2. Modeling of inversion electron density

The inversion charge density including weak and strong inversion can be found by solving Poisson's Equation and applying the necessary boundary conditions. The total charge density is

$$Q_{\mathrm{inv}} = C_{\mathrm{ox}}\left(V_{\mathrm{gs}} - V_{\mathrm{Ts}}\right), \tag{17}$$

where C_{ox} is the oxide capacitance (F/m^2), $kT/q = V_{\mathrm{t}} = 0.026$ V at room temperature, ϕ_{f} is the Fermi potential in the substrate, equals $(kT/q)\ln(N_{\mathrm{a}}/n_{\mathrm{i}})$, and

$$V_{\mathrm{Ts}} = V_{\mathrm{fbs}} + \phi_{\mathrm{ss}} + \phi_{\mathrm{ox}}. \tag{18}$$

The flat band voltage for a metal gate strained silicon MOSFET is hence given by[7]

$$V_{\mathrm{fbs}} = \phi_{\mathrm{m}} - \{\chi_{\mathrm{s}} + E_{\mathrm{g}}^{\mathrm{sige}} - V_{\mathrm{t}}\ln(N_{\mathrm{v}}^{\mathrm{sige}}/N_{\mathrm{a}})\}, \tag{19}$$

where $\chi_{\mathrm{s}} = 4.35 + 0.58x$, $N_{\mathrm{v}}^{\mathrm{sige}} = 1.04 + x\ (0.6 - 1.04) \times 10^{19}$ cm^{-3}, $\phi_{\mathrm{ss}} = 2\ \phi_{\mathrm{f}} - \Delta E_{\mathrm{g}}$, $E_{\mathrm{g}} - \Delta E_{\mathrm{g}} = E_{\mathrm{g}}^{\mathrm{sige}}$, $E_{\mathrm{g}} = 1.12$ eV, $\Delta E_{\mathrm{g}} = 0.4x$, $\phi_{\mathrm{oxs}} = qN_{\mathrm{a}}x_{\mathrm{d}}/C_{\mathrm{ox}}$ obtained from Eq. (8). So, using Eqs. (8) and (17) in Eq. (7), we get the effective surface electrical field. So using Eq. (7), Equations (3)–(6) can be solved explicitly. The following are the results obtained after calculating these above equations.

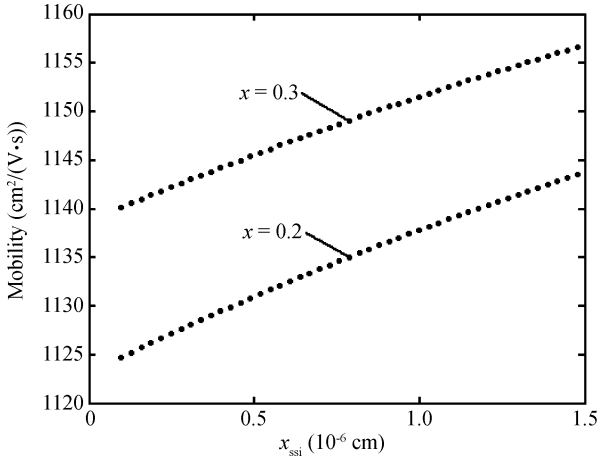

Fig. 4. Modeled results of electron phonon mobility with strained silicon thickness for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature with a gate to source voltage of 3 V.

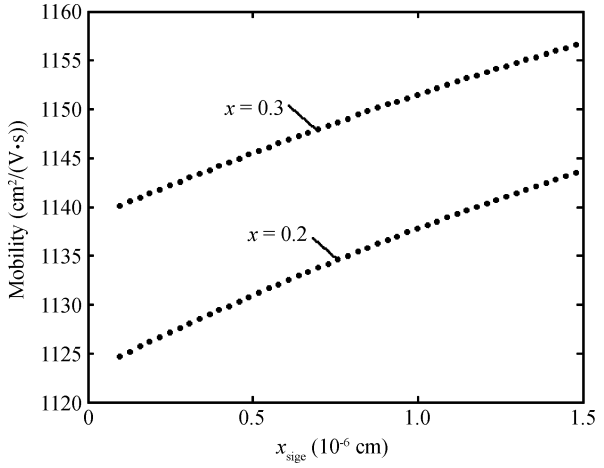

Fig. 5. Modeled results of electron phonon mobility with silicon germanium thickness for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature with a gate to source voltage of 3 V.

5. Results and discussion

We have modeled electron mobility for the biaxial strained silicon/SiGe MOSFET for various device parameters. The parameters used in our simulation are given in Table 1. Figure 3 shows the phonon mobility variation with the effective surface electrical field. The influence of strain due to increased germanium content is clearly seen as the mobility increases with the increased germanium content, even at high electrical fields. The results match closely with reported results[5]. Figure 4 shows the phonon mobility variation with the strained silicon thickness. The influence of strain due to increased germanium content is clearly seen as the mobility increases with the increased germanium content at high strained silicon thickness. Figure 5 shows the phonon mobility variation with the relaxed silicon germanium layer thickness. The influence of strain due to increased germanium content is clearly seen as the mobility increases with the increased germanium content. The results match closely with reported results[5].

Figure 6 shows the columbic mobility variation with the

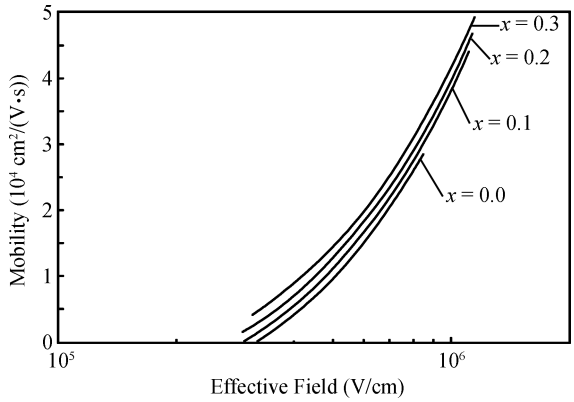

Fig. 6. Modeled results of electron coulomb mobility with effective electrical field for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature.

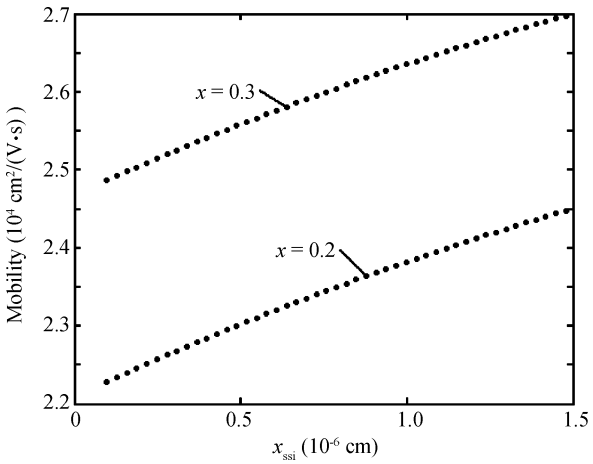

Fig. 7. Modeled results of electron coulomb mobility with strained silicon thickness for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature with a gate to source voltage of 3 V.

effective surface electrical field. The influence of strain due to increased germanium content is clearly seen as the columbic mobility increases with the increased germanium content, even at high electrical fields. The increase is not so sharp as compared to the phonon mobility increase, showing little impact of the strain on the columbic mobility. Figures 7 and 8 show an increasing trend of columbic mobility with the strained silicon thickness and relaxed silicon germanium thickness, respectively.

Figure 9 shows the surface roughness mobility variation with the effective surface electrical field. The influence of strain due to increased germanium content is clearly seen as the surface roughness mobility increases with the increased germanium content, even at high electrical fields. The increase is not so sharp as compared to the phonon mobility increase, showing little impact of the strain on the surface roughness mobility. Figures 10 and 11 show an increasing trend of columbic mobility with the strained silicon thickness and relaxed silicon germanium thickness, respectively.

Figure 12 shows the phonon and surface roughness mobility variation with the effective surface electrical field. The influence of strain due to increased germanium content is clearly

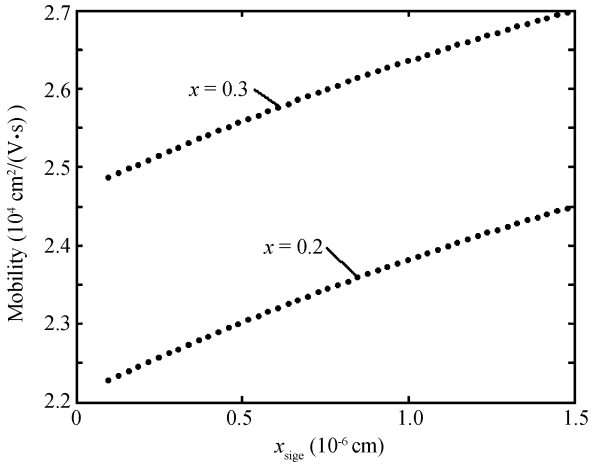

Fig. 8. Modeled results of electron coulomb mobility with relaxed silicon germanium thickness for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature with a gate to source voltage of 3 V.

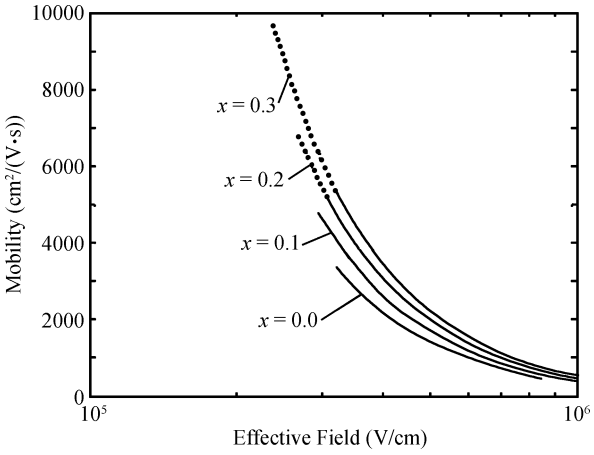

Fig. 9. Modeled results of surface roughness electron mobility with effective electrical field for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature.

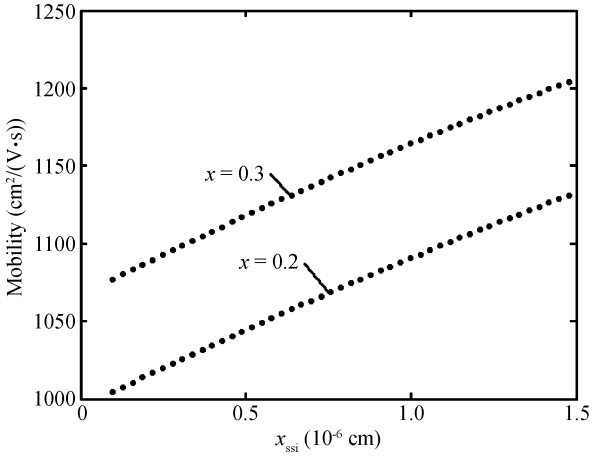

Fig. 10. Modeled results of surface roughness electron mobility with thickness of strained silicon region for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature with a gate voltage of 3 V.

seen as the surface roughness mobility increases with the increased germanium content, even at high electrical fields. The

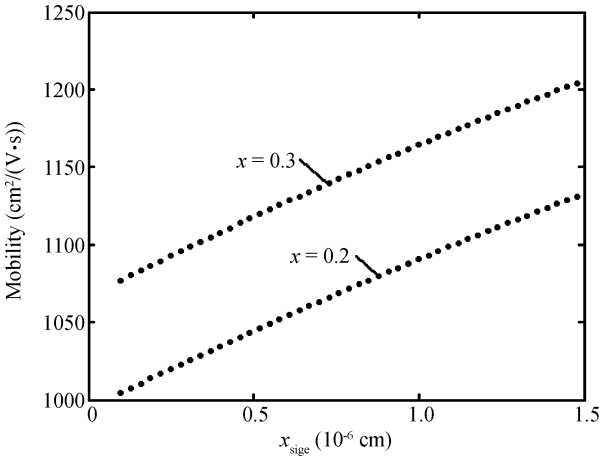

Fig. 11. Modeled results of surface roughness electron mobility with thickness of relaxed silicon germanium region for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature with a gate voltage of 3 V.

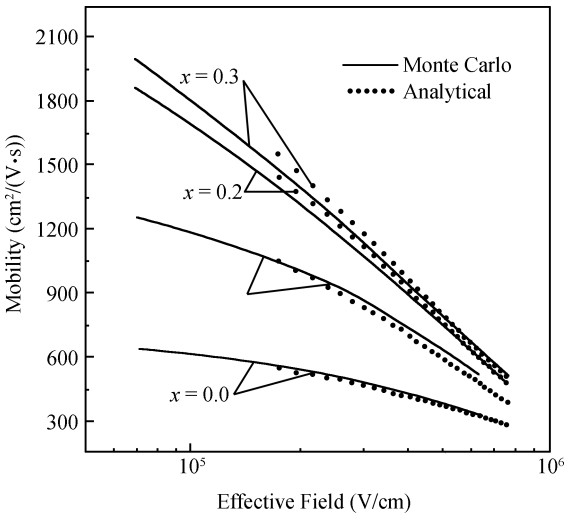

Fig. 12. Modeled results of electron mobility (accounting for phonon and surface roughness scattering mechanisms) with effective electrical field for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature. Reported results are shown by black lines. Data calculated with the model developed in this paper are shown by blue symbols.

results match closely with reported results[5]. Figure 13 shows all three mobility variation with the effective surface electrical field. The influence of strain due to increased germanium content is clearly seen as the surface roughness mobility increases with the increased germanium content, even at high electrical fields. The results match closely with reported results[5].

6. Conclusion

The semi analytical model developed in this paper shows an increase in electron mobility with the germanium concentration at a given electrical field. The results match closely with the numerical results produced using Monte Carlo simulations reported in literature.

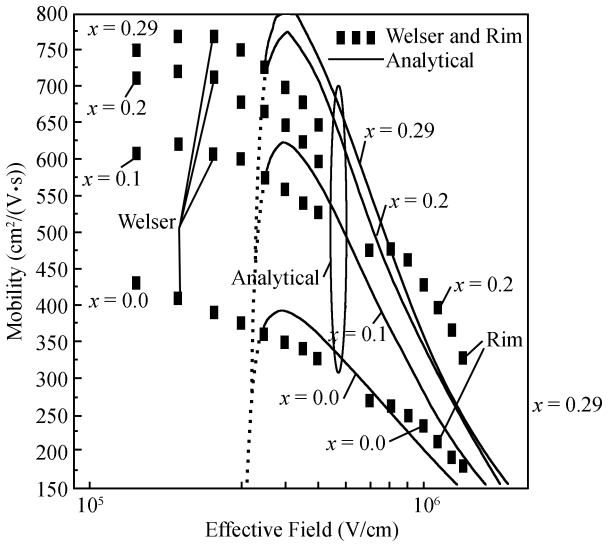

Fig. 13. Modeled results of electron mobility with effective electrical field for strained-Si on $Si_{1-x}Ge_x$ MOSFETs at room temperature. Data reported by Welser *et al.* and Rim *et al.* in Ref. [5] are shown by squares. Data calculated with the model developed in this paper are shown by lines. The mobility curves vary with the germanium content in the relaxed SiGe buffer layer.

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