A 16.3 pJ/pulse low-complexity and energy-efficient transmitter with adjustable pulse parameters*

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Abstract: This paper presents a novel, fully integrated transmitter for 3–5 GHz pulsed UWB. The BPSK modulation transmitter has been implemented in SMIC CMOS 0.13 μm technology with a 1.2-V supply voltage and a die size of 0.8×0.95 mm^2. This transmitter is based on the impulse response filter method, which uses a tunable R paralleled with a LC frequency selection network to realize continuously adjustable pulse parameters, including bandwidth, width and amplitude. Due to the extremely low duty of the pulsed UWB, a proposed output buffer is employed to save power consumption significantly. Finally, measurement results show that the transmitter consumes only 16.3 pJ/pulse to achieve a pulse repetition rate of 100 Mb/s. Generated pulses strictly comply with the FCC spectral mask. The continuously variable pulse width is from 900 to 1.5 ns and the amplitude with the minimum 178 mVpp and the maximum 432 mVpp can be achieved.

Key words: pulsed UWB; generator; BPSK; RLC

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1. Introduction

Short-range wireless communication is becoming popular as a replacement for cable-based systems due to its compact and high data rate. Pulsed ultra-wideband (UWB) is a short-range wireless communication technology that transmits information via ultra-narrow modulated pulses. Contrary to narrowband systems, UWB signals have an extremely low power spectral density (–41.3 dBm/MHz) and a very large spectrum occupying from 3.1 to 10.6 GHz with high data rates that can, in theory, reach up 500 Mb/s, as specified by the Federal Communication Commission (FCC)[1]. Because of the high interference by WLAN in the 5.1–6 GHz, the UWB pulse generation divides the whole spectrum into the low sub-band occupying from 3.1 to 5.1 GHz and another high sub-band from 6 to 10.6 GHz. The low band below 5.1 GHz is targeted in this paper.

UWB large current radiator antennas have come out and radio frequency designs are increasingly taking advantage of technology advances in CMOS of small scale and low cost, so this makes a high rate transmitter of sub-nanosecond scale pulses possible. The design of a pulsed UWB transmitter presents a unique virtue due to no up/down conversion or mixer. Consequently, the circuit implementation is simpler with substantial reduction in chip area and power consumption. There are commonly two types of impulse pulses, including the analog and the digital implementation. An analog approach[2] employs the square and the exponential functions of transistors biased in saturation and the weak inversion region, respectively. An ultra-wideband amplifier is needed because the amplitude of the pulse is very small. The basic concept of digital approaches[3−5] is that a digital signal and its inverted delayed signal can produce a narrow pulse via a gate of NAND or NOR. At farther stages, the narrow pulse is shaped and amplified.

The proposed novel BPSK transmitter architecture is shown in Fig. 1. The pulse generator block employs a digital approach to generate positive and negative impulse pulses. And then the positive and negative impulse pulses are combined in a pulse block and shaped by a proposed tunable RLC filter in a pulse shaping block. Finally, a proposed low-power output buffer connects the pulses to the emission antenna. In this paper, the digital approach and no mixer feature can lower the transmitter complexity greatly. Each transmitter block is based on, and improves on, the normal circuit architecture, so the total transmitter architecture and block circuits are of low complexity. The single-chip fully integrated BPSK modulation transmitter is implemented in SMIC 0.13 μm CMOS; and the output pulses feature adjustable parameters and achieve the low power of 16.3 pJ/pulse at a data rate of 100 MHz. The following section presents each circuit block and its principle in the literature. In Section 3, measurement results are shown and finally a conclusion is given.

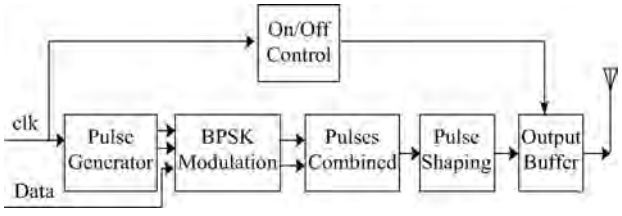

Fig. 1. Architecture of the transmitter.

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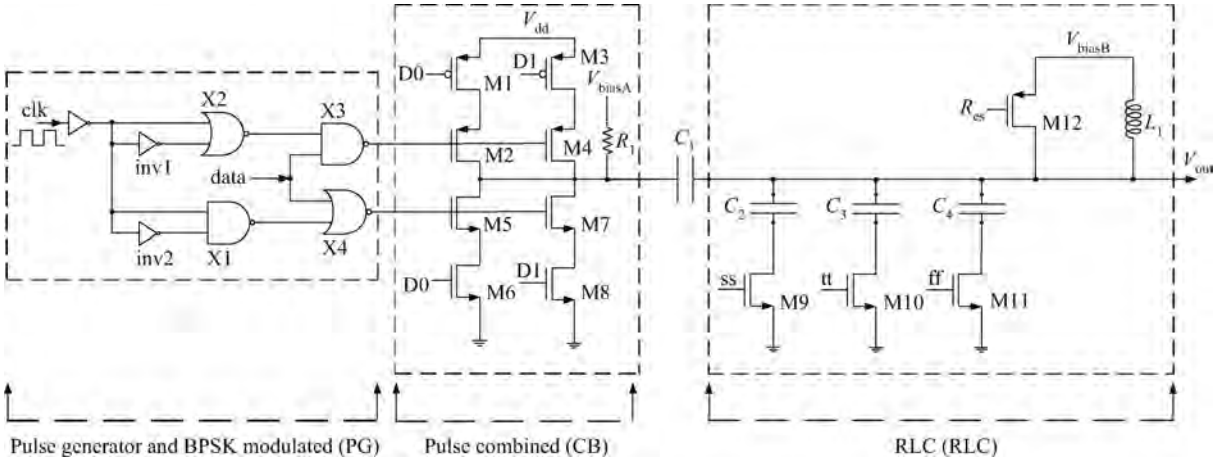

Fig. 2. Pulse generation and pulse shaping.

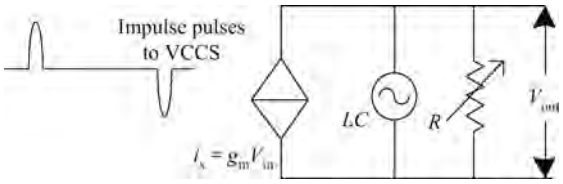

Fig. 3. Pulse generation principle.

2. Transmitter circuit and principle

2.1. Pulse generator and BPSK modulation (PG)

The proposed pulse generator block is shown in the first dashed block of Fig. 2. Considering low power, all of the gates are the minimum scale digital gates possible. Inverter inv1, NAND X1 and inverter inv2, NOR X2 generate two branches that contain positive phase pulses at the bottom and negative phase pulses on the top, respectively. The pulses are ultra-narrow and their bandwidths are extremely flat, so that the pulse bandwidth can be determined by the farther stage of the pulse shaping block.

NAND X3 and NOR X4 can achieve BPSK modulation. 'Data' is the digital baseband input signal. When 'data' is at a high level, the upper path is selected and NAND X3 outputs a negative narrow pulse. In contrast, the lower path is selected and NOR X4 outputs a positive narrow pulse. Assuming the input clock 'clk' is 100 MHz, when the digital baseband input 'data' is 100 MHz, NAND X3 and NOR X2 output positive or negative pulses at 100 MHz. However, if the 'data' falls to 50 MHz, there will be two identical pulses per bit of data. The bit error rate (BER) can be reduced by transmitting several identical pulses for one bit of data, but the available data rate and the power consumption per data bit are exacerbated.

2.2. Pulse combined block

As shown in the middle dashed block of Fig. 2, the bias voltage '$V_{\rm biasA}$' and the resistance R_1 are used to set the operating point. This can prevent the amplitudes of the positive and negative pulse from being the same caused by up and down transistor saturation or cut-off. In this block, positive and negative pulses are combined and three different amplitudes are realized. Transistors M1–M8 are not only used to combine positive and negative pulses but also to control pulse amplitude. The M1–M4 sizes are one-to-one proportional to the M5–M8 sizes. Considering D1 and D0 supply '11', '10' or '01', the pulse peak-to-peak amplitude can be one of three values for different transmission distances.

2.3. Pulse shaping filter with adjustable parameters

A well-known LC network can realize a frequency selection function, but here a tunable R is introduced and made parallel to the LC network. In Fig. 2, the transistor M12 is added as the tunable R. The tunable R and LC network comprise a tunable RLC pulse shaping filter. Figure 3 presents the basic principle network in this paper; it contains a voltage control current source (VCCS) and a tunable RLC filter.

Because the duty cycle of the input pulse is very low, there is no interference between the output pulses. The output pulse comprises two parts. The first part is obtained when the input impulse pulse is imposed on the VCCS and the energy in the LC tank is stored. Another is obtained when the LC tank discharges immediately when the input pulse disappears. Assuming the input pulse is a sine wave for simplicity, the VCSS current $i_{\rm s}$ can be approximated to a sine shape $i_{\rm s} = A\cos\omega_{\rm s}t$. The response '$V_{\rm out}$' v can be given by

$$v = \begin{cases} AL\omega_{\rm s}\left[\sin(\omega_{\rm s}t+\phi) - {\rm e}^{-\alpha t}\dfrac{B}{\omega_{\rm s}}\sin(\omega_{\rm d}t+\varphi)\right], \\ \qquad 0 \leqslant t \leqslant t_{\rm d}, \\ -CL{\rm e}^{-\beta(t-t_{\rm d})}\sin(\omega_{\rm T}(t-t_{\rm d})-\theta), \quad t > t_{\rm d}, \end{cases} \tag{1}$$

where

$$\omega_{\rm d} = \sqrt{1/LC - \alpha^2}, \quad \alpha = 1/2CR,$$

$$\omega_{\rm T} = \sqrt{1/LC - \beta^2}, \quad \beta = 1/2CR,$$

$$B = \sqrt{\left[\left(\frac{\alpha}{\omega_{\rm s}}\cos\phi - \sin\phi\right)^2 + \cos^2\phi\right](\omega_{\rm d}^2 + \alpha^2)},$$

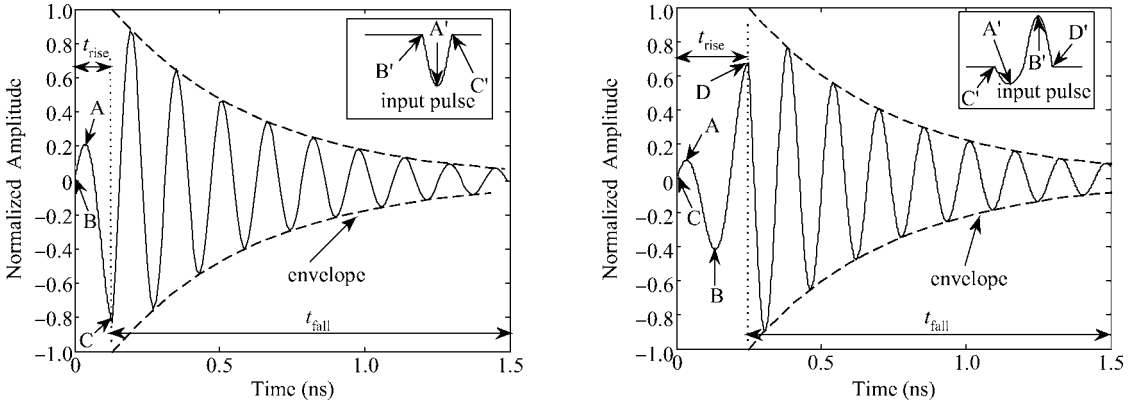

Fig. 4. Two different output pulse forms corresponding to two different input pulses, respectively.

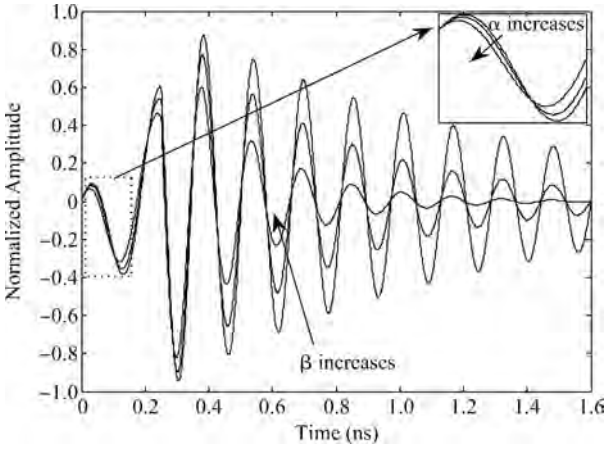

Fig. 5. Different output pulses with different α and β.

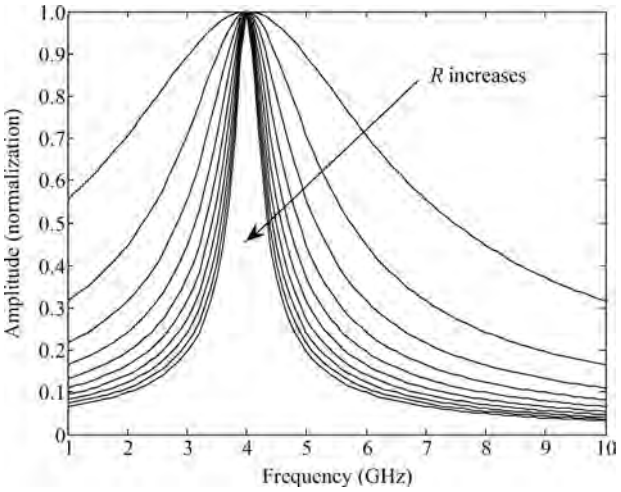

Fig. 6. Normalization frequency characteristic $|Z|$ of RLC when R is changing.

$$\varphi = \arctan \frac{\omega_s \alpha \cos\phi - \omega_d (\omega_s \sin\phi - \alpha \cos\phi)}{\omega_s \omega_d \cos\phi + \alpha (\omega_s \sin\phi - \alpha \cos\phi)},$$

$$C = \sqrt{\left(i_{La}(t_d)\frac{\omega_T^2 + \beta^2}{\omega_T} - \beta\frac{v_a(t_d)}{L\omega_T}\right)^2 + \left(\frac{v_a(t_d)}{L}\right)^2},$$

$$\theta = \arctan \frac{\omega_T v_a(t_d)}{L i_{La}(t_d)\left(\omega_T^2 + \beta^2\right) - \beta v_a(t_d)}.$$

According to Eq. (1), considering half a period and a period sine input signals, Figure 4 shows two output pulse waveforms v. The output pulse time is made up of t_{rise} and t_{fall}. The first corresponding output waveform is drawn by the top expression of Eq. (1); t_{rise} represents the time t_d. The second part decaying output waveform with the exponential envelope corresponds to the bottom expression of Eq. (1); t_{fall} is the decay time. There is a time one-to-one correspondence between the marks ABCD and A'B'C'D' in Fig. 4.

The tunable R can be employed to control the pulse width. Assuming $v_{o_{cycle}}$ is the output value at the time t_d and $v_{n_{cycle}}$ represents the output value at the time $\left(t_d + \frac{2\pi}{\omega_T} n_{cycle}\right)$, where the pulse second part $v = -CLe^{-\beta(t-t_d)} \sin(\omega_T(t-t_d) - \theta)$, the following expression can be given by $\frac{v_{o_{cycle}}}{v_{n_{cycle}}} = e^{-\beta(t-t_d)}$. The number n_{cycle} of the peaks

$$n_{cycle} = \frac{t - t_d}{2\pi\sqrt{LC}} = -\frac{1}{\beta} \ln \frac{v_{o_{cycle}}}{v_{n_{cycle}}} \Big/ 2\pi\sqrt{LC}, \quad (2)$$

where $v_{n_{cycle}} \leqslant 0.1 v_{o_{cycle}}$, can be regarded as the pulse end point. Equation (2) proves that the number n_{cycle} of output pulses can be controllable by β; and thus the tunable R can control the pulse width for $\beta = 1/2CR$. Figure 5 shows that the pulse decay speed or the pulse amplitude can be continuously variable at different α and β.

The resistance frequency characteristic of the proposed pulse shaping block is $Z = \frac{1}{SC} // SL // R \approx \frac{R}{1 + jR\sqrt{\frac{C}{L}}\frac{2(\omega-\omega_0)}{\omega_0}}$, where $\omega_0 = 1/\sqrt{LC}$ is the center frequency of the LC network. The modular algorithm $|Z|$ can be given by the following expression,

$$|Z| = \frac{R}{\sqrt{1 + \left(R\sqrt{\frac{C}{L}}\frac{2(\omega - \omega_0)}{\omega_0}\right)^2}}. \quad (3)$$

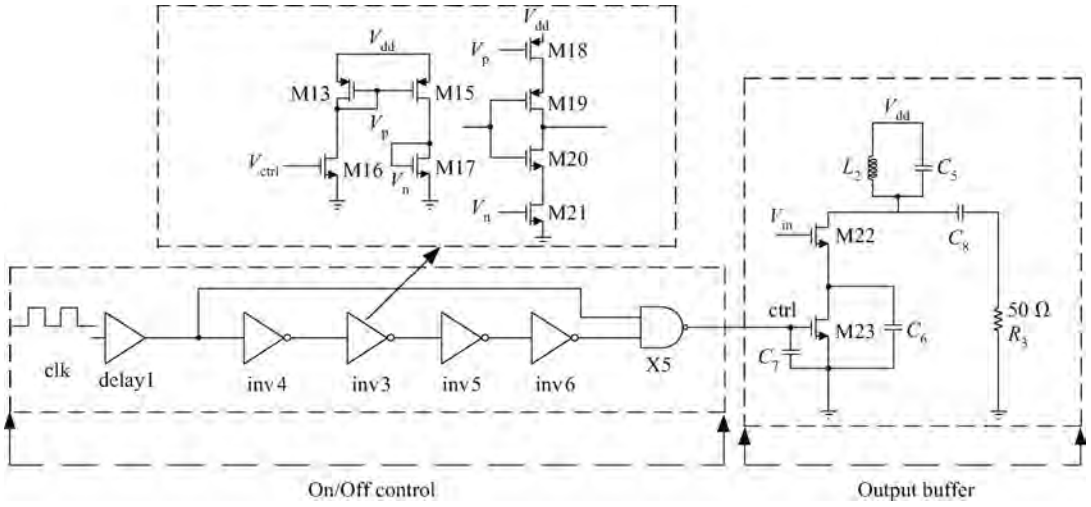

Fig. 7. The proposed output buffer and on/off control.

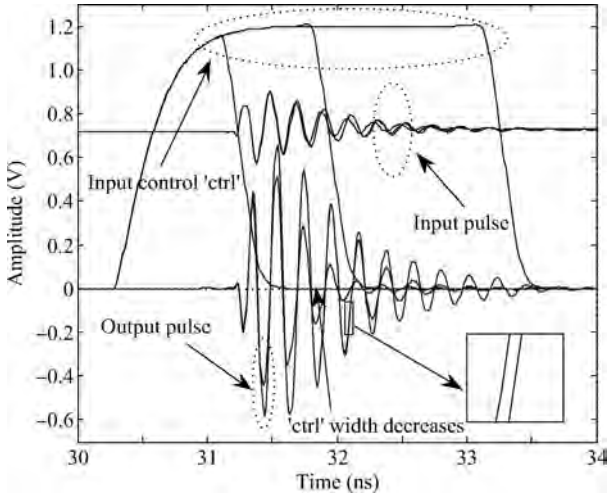

Fig. 8. Simulation of new output buffer at three different 'V_{ctrl}'.

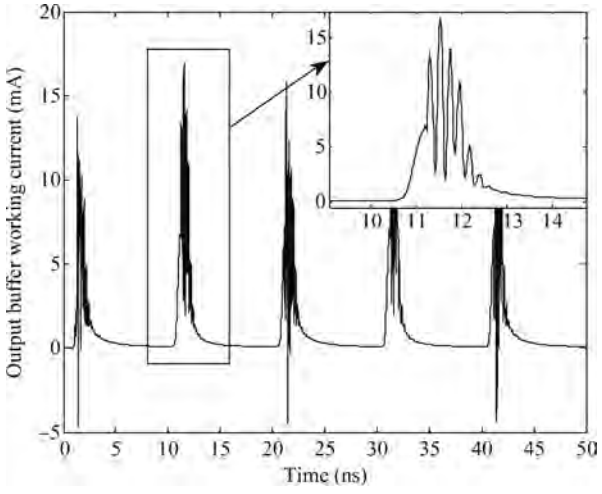

Fig. 9. Output buffer working current at a data rate of 100 MHz.

According to Eq. (3), Figure 6 proves that the bandwidth can be tuned by adjusting R. Observing Eq. (3), the tunable R can affect the value $|Z|$, so that output pulse amplitudes can be continuously adjustable.

This paper is based on the proposed tunable RLC pulsed shaping filter. Thus the pulse amplitude, width or bandwidth can be adjusted and the output pulse power spectral density (PSD) can strictly comply with the FCC spectral emission mask. In the third block of Fig. 2, transistor M12 is designed as an adjustable resistance; so the output pulse parameters can be controlled continuously. Inductor L_1, capacitors C_2, C_3, C_4 and transistor M12 are made up of a tunable RLC pulse shaping filter. Capacitors C_2, C_3, C_4 can be selected by switching M9–M11 on/off to compensate three different process corners, respectively. The LC network can lock the center frequency between 3 and 5 GHz.

2.4. Output buffer and on/off control

In pulsed UWB, the pulse width is nanosecond order and the transmitted duty ratio is very low. If the output buffer circuit can be cut off when there absents the pulse, the low power can be achieved. A proposed on/off control block is shown in the left dashed Fig. 7. The on/off control block produces a control signal 'ctrl', which switches the output buffer on/off. The inverter inv3 adopts the structure of a current-starved inverter[7]. The biasing circuit is also shown in the dashed box. The signal 'V_{ctrl}' can control the inverter delay time, which is proportional to the current.

A proposed output buffer block is shown in the right dashed Fig. 7. The main low power of the output buffer can be accomplished by switching M23 on/off. Considering the status that the pulse still stays on and the transistor M23 is switched off, capacitor C_6 can compensate for the time mismatch. To ensure the output buffer normal working at the biggest mismatch, the C_6 value must be large enough. As shown in Fig. 8, the simulation shows that the output pulse can go on when the input control ctrl is off. The M23 turn-on time can be designed as the same as the pulse width or shorter. As a result, the power consumption of the output buffer can be saved. Figure 9 is working current simulation of the output buffer at data rate of 100 MHz; it is obvious that the output buffer working current is saved a lot. Simulations indicate that the output buffer power consumption accounts for 85% of the total transmitter.

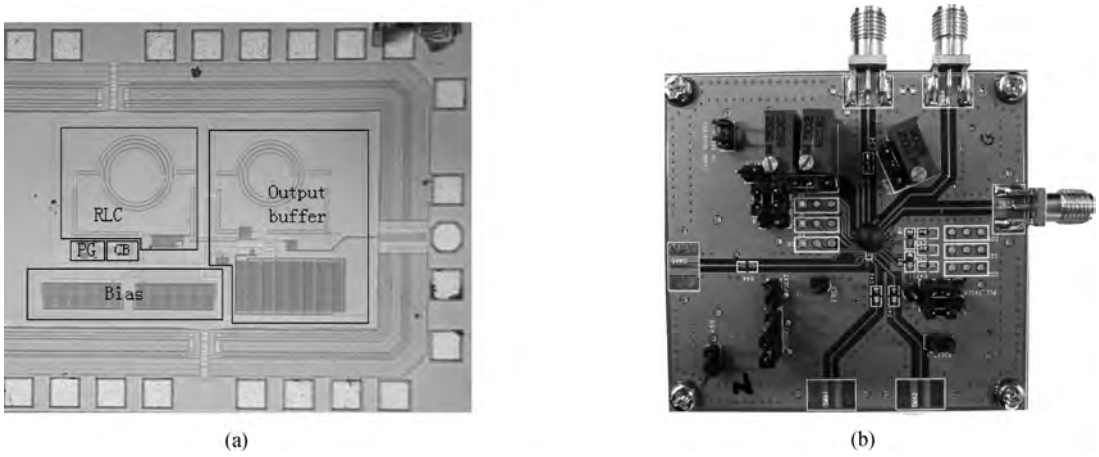

Fig. 10. (a) Die photomicrograph. (b) PCB of transmitter.

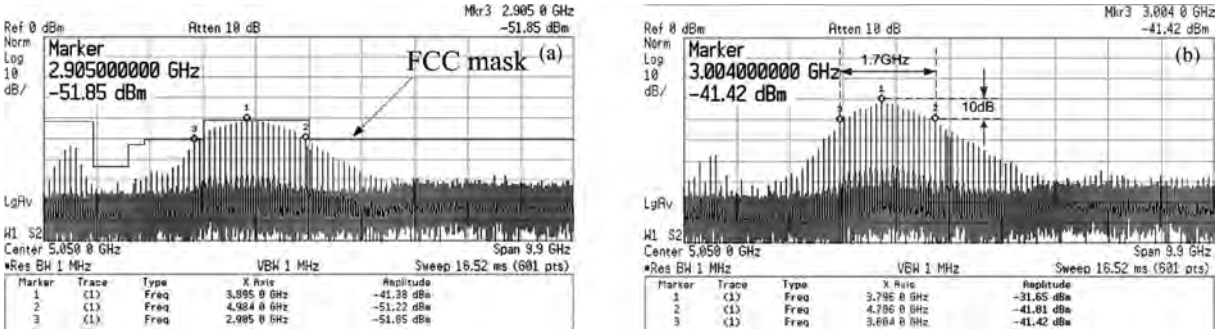

Fig. 11. PSD of (a) high and (b) low supply 'Res' at a data rate of 100 MHz.

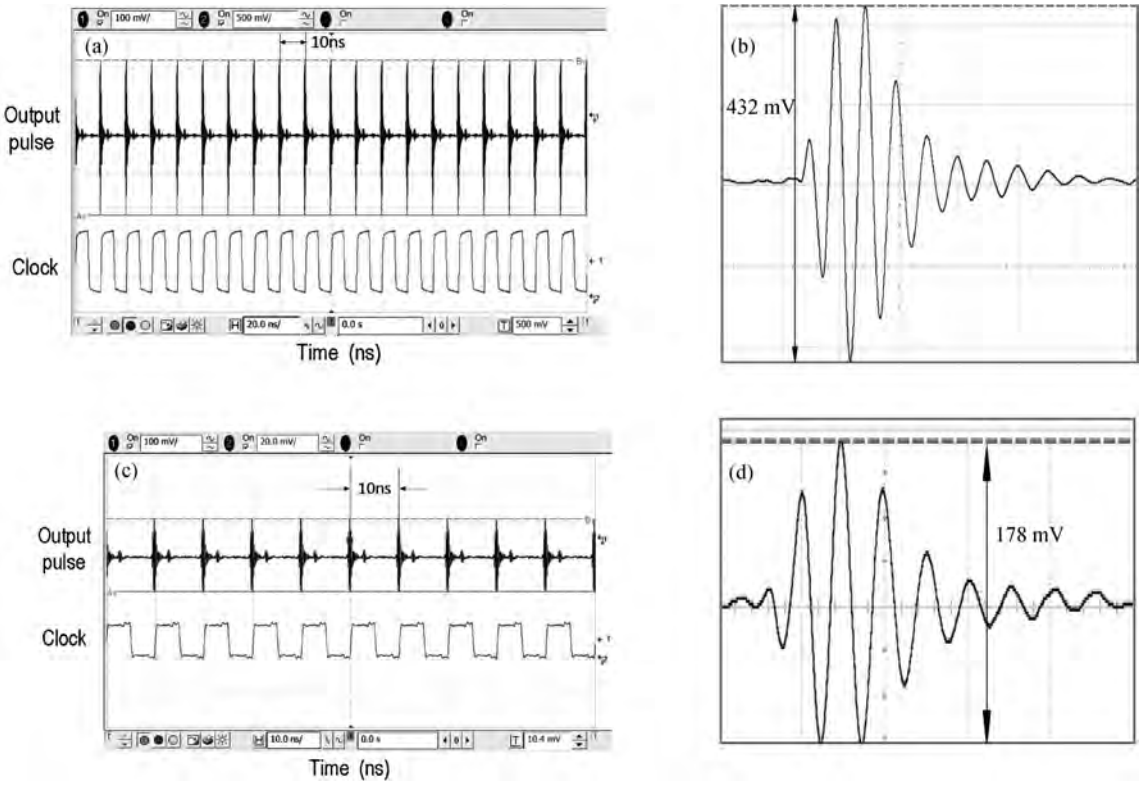

Fig. 12. Measured (a) positive pulses of maximum amplitude and (c) negative pulses of minimum amplitude at 100 MHz. (b), (d) Single corresponding enlarged pulses.

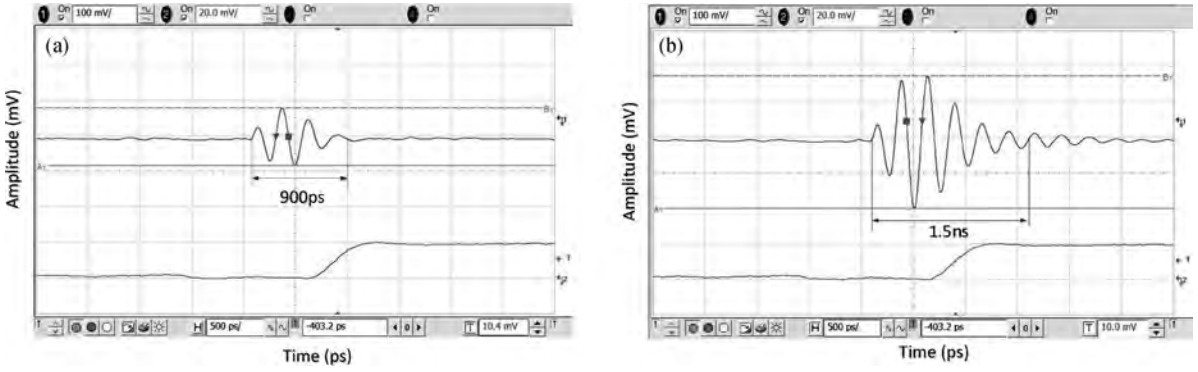

Fig. 13. (a) The minimal width pulse. (b) The maximal width pulse.

Table 1. Summary of transmitter performance and comparison.

Ref.	V_{pp} (mV)	Supply (V)	BW (–10 dB) (GHz)	Operation band (GHz)	CMOS (nm)	Power Cons. (mW)	Ep (pJ/pulse)	Area (mm^2)	Technique	Modulation
[5]	142	1.2	6.8	3–10	130	3.84 @ 100 MHz	38.4	0.54 (die)	Filter edge combination	OOK
[9]	90	1	0.6–1.4	3–6	65	NC @ 50 MHz	42.4	0.036 (core)	LO switch combination	BPSK
[10]*	60	1.8–2.2	2	6–10	180	NC @ 750 MHz	12*	0.045 (core)*	Filter edge combination	BPSK
[11]	165–710	1	0.5	3–5	90	4.36 @ 15.6 MHz	279.5	0.07 (core)	DCO combination	PPM+BPSK
This work	178–432	1.2	2	3–5	130	1.63 @ 100 MHz	16.3	0.76 (die)	Impulse pulse RLC filter	BPSK

*Do not include power amplifier.

Transistor M22, inductor L_2 and capacitor C_5 realize an ultra-wideband RF amplifier[8]. R_2 of 50 Ω is the input impedance of the antenna. Because the transistor M23 input 'ctrl' is a single peak pulse which is in possession of high frequency, capacitor C_7 is used to prevent the high frequency from coupling to the final output port.

3. Measurement results

The proposed pulsed UWB transmitter is implemented in SMIC 0.13 μm 1P8M CMOS technology with a 1.2 V supply. The output time domain and the PSD of the UWB transmitter are measured using an Agilent 12 GHz 40 GSample/s scope infiniium DSO92104A digital storage oscilloscope and an Agilent E4440A 3 Hz–26.5 GHz PSA series spectrum analyzer, respectively. The transmitter occupies chip areas of 0.8×0.95 mm^2 and the total power of the transmitter is 1.63 mW at a data rate of 100 MHz. The photograph of the chip and the test PCB are shown in Fig. 10.

The measured PSD at s transmitting data rate of 100 MHz is shown in Fig. 11. The center frequency is locked at about 3.9 GHz. The bandwidth of 10 dB in Fig. 11(a) is about 2 .1 GHz from 2.9 to 5 GHz, which strictly complies with a FCC spectral mask. Another bandwidth of 10 dB in Fig. 11(b) occupies 1.8 GHz from 3.0 to 4.8 GHz. The two PSDs correspond to the high and low supply of 'Res' (in Fig. 2), respectively. This proves that the bandwidth can be continuously changed by 'Res'.

The measured time domain waveform with min and max amplitudes is illustrated in Fig. 12, where the BPSK data rate is 100 MHz. Figure 12(a) shows a '1' stream. Figure 12(b) enlarges a single pulse of Fig. 12(a) where the pulse peak-to-peak is the max about 432 mV. Figure 12(c) shows a '0' stream. Figure 12(d) enlarges a single pulse of Fig. 12(c), where the pulse peak-to-peak is the minimum about 178 mV. The measured pulse waveform conforms to the theoretical analysis of Fig. 4.

The measured different width pulses are shown in Fig. 13. It is obvious that the pulse width can be continuously adjustable by changing the 'Res'. This also accords to the theoretical analysis expression (2).

A summary of the measured results and a comparison with previous papers is included in Table 1. The compared parameter Power Cons. represents the total power consumption of the transmitter at a pulse repetition rate. Another compared parameter Ep is given by

$$\mathrm{Ep} = \frac{\text{Total power consumption}}{\text{Pulse repetition rate}}.$$

4. Conclusion

A novel BPSK modulated pulsed UWB transmitter has been proposed for low-power and low-complexity. Due to the tunable RLC shaping filter, the transmitter parameters are continuously adjustable, including amplitude, pulse width, spectrum and bandwidth. The center frequency can be locked between 3 and 5 GHz and the PSD strictly complies with the FCC spectral emission mask. The proposed output buffer architec-

ture is employed so that the total power consumption can be saved significantly.

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