Characteristics and optimization of 4H-SiC MESFET with a novel p-type spacer layer incorporated with a field-plate structure based on improved trap models*

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Abstract: A novel structure of 4H-SiC MESFETs is proposed that focuses on surface trap suppression. Characteristics of the device have been investigated based on physical models for material properties and improved trap models. By comparing with the performance of the well-utilized buried-gate incorporated with a field-plate (BG-FP) structure, it is shown that the proposed structure improves device properties in comprehensive aspects. A p-type spacer layer introduced in the channel layer suppresses the surface trap effect and reduces the gate–drain capacitance (C_{gd}) under a large drain voltage. A p-type spacer layer incorporated with a field-plate improves the electric field distribution on the gate edge while the spacer layer induces less C_{gd} than a conventional FP. For microwave applications, 4H-SiC MESFET for the proposed structure has a larger gate-lag ratio in the saturation region due to better surface trap isolation from the conductive channel. For high power applications, the proposed structure is able to endure higher operating voltage as well. The maximum saturation current density of 460 mA/mm is yielded. Also, the gate-lag ratio under a drain voltage of 20 V is close to 90%. In addition, 5% and 17.8% improvements in f_T and f_{max} are obtained compared with a BG-FP MESFET in AC simulation, respectively. Parameters and dimensions of the proposed structure are optimized to make the best of the device for microwave applications and to provide a reference for device design.

Key words: 4H-SiC; MESFET; surface trap; p-type spacer layer; microwave application
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1. Introduction

There are increasing demands for microwave applications. Metal semiconductor field effect transistors (MESFETs) based on silicon carbide (SiC) have received increasing attention for their excellent properties, such as wide bandgap, high electron saturation drift velocity and high thermal conductivity[1]. However, there have been some reports revealing that SiC MESFETs suffer from a severe surface trapping problem that is fatal in microwave applications[2−4].

A lot of effort has been made to solve this problem. Various kinds of passivation material have been investigated to improve surface properties[5]. However, the surface traps are not removed from the surface fundamentally. A buried-gate approach was shown to result in less trapping, leading to less frequency dispersion and a reduction in current instability[6]. A buried-channel solution has been proved to give a favorable gate-lag ratio, resulting in improved microwave power performance[7]. However, the lightly doped spacer layer turns out to be n-type, which changes the designed parameters for the desired specification. A field-plate (FP) improves the electric field distribution by reducing the peak electric field at the gate edge, giving a higher operating voltage, and simulations have been made to identify the same effects on SiC MESFETs[8]. However, FP introduces extra gate–drain capacitance (C_{gd}), which works as feedback capacitance in AC output network and limits the MSG[9].

In this paper, a novel p-type spacer layer incorporated within a field-plate structure, which can overcome the hindrances mentioned above, is proposed. Studies on DC, AC, transient and breakdown characteristics based on applicable models were made and the results show that a 4H-SiC MESFET with the proposed structure has several advantages over the well recognized BG-FP structure. It is indicated that the proposed MESTET is a competitive candidate for microwave applications.

2. Device structure and physical models

Figure 1 shows a schematic cross-section of a 4H-SiC MESFET fabricated in the proposed structure; a p-type layer is introduced on the top of the n-type conductive channel layer, and two heavy-doped n^+ regions are formed on the p-type spacer by ion implantation for ohmic contact formation. Then a passivation layer is fabricated on the p-type layer to protect the active region of the device. This approach is similar to the introduction of the p-buffer layer on the substrate in earlier work[10]. The main function of the p-buffer layer is to shield the deep levels in the substrate. In the proposed structure, the conductive channel is isolated from surface traps by the insertion of

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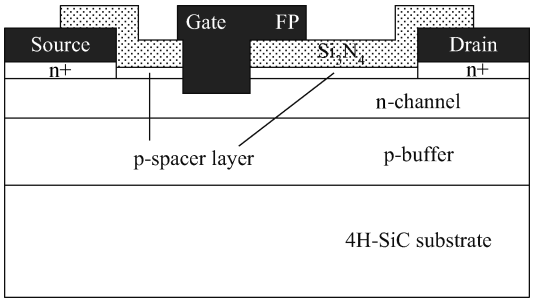

Fig. 1. Schematic cross-section of a 4H-SiC MESFET with the proposed p-type spacer layer.

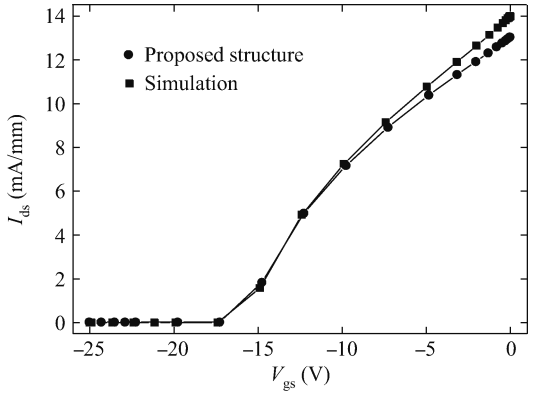

Fig. 2. Transfer characteristics of simulated BG-FP structure and proposed structure.

the p-type spacer layer.

The introduced p-type spacer layer has a thickness of 0.1 μm and a doping concentration of 3×10^{15} cm^{-3}, and the n-type channel used as the conductive channel for device operation has a thickness of 0.22 μm and a doping concentration of 3×10^{17} cm^{-3}. As conventional SiC MESFETs, a buffer layer with a thickness of 0.6 μm and a doping concentration of 5×10^{15} cm^{-3} is interspersed between the conductive channel and the substrate. To have a meaningful comparison, the channel thickness of the MESFET based on the BG-FP structure is also set at 0.22 μm, which ensures that both devices will have comparable pinch-off voltages. The other dimensions of two devices are as follows: gate length of the device L_g = 0.6 μm, gate–drain spacing L_{gd} = 1.5 μm and gate–source spacing L_{gs} = 0.6 μm.

A two dimensional simulator ISE TCAD is used in the simulation. To obtain accurate results, several basic physical models such as bandgap narrowing for bandgap, high field saturation for mobility of the carrier and incomplete ionization for carrier concentration are utilized, which precisely describe the material properties. Also, to make a simulated surface trap effect more comparable with experimental data, surface traps are assumed to exist along the SiC/SiO_2 interfaces. The density and capture cross section of the near interface trap (NIT) are set to 5.3×10^{12} cm^{-2} and 1×10^{-19} cm^2, while the density and capture cross section of the deep interface trap (DIT) are set to 1.2×10^{13} cm^{-2} and 1.4×10^{-15} cm^2 [11, 12]. Schottky barrier tunneling (SBT) and initial trap populating (ITP) are taken into account for transient investigation. Similar studies concerning

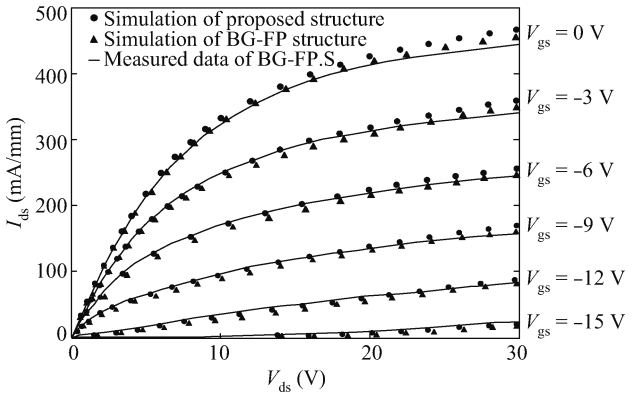

Fig. 3. I–V characteristics under different gate voltages for 4H-SiC MESFETs.

these mechanisms can be found elsewhere[13] and the accuracy of relevant models has been verified.

3. Results and discussion

Figure 2 depicts the transfer characteristics of proposed and BG-FP structures; devices with both structures have the same pinch off voltage (V_p) of –17 V. The parameters of the BG-FP MESFET for simulation are utilized as in the work of Ref. [14], and the measured pinch off voltage of the BG-FP MESFET is –18 V, which is comparable with our simulation and makes the results credible.

Figure 3 plots the drain current (I_{ds}) versus the drain–source voltage (V_{ds}) for devices with two structures, and the experimental data[14] of the BG-FP MESFET are included for comparison. The gate voltage (V_{gs}) was varied from 0 to –15 V in steps of –3 V. For meaningful comparison, the channel thickness, doping concentration, gate length and other parameters of the MESFETs with both structures are designed to be equal. The saturation drain current density (I_{dsat}) with V_{gs} = 0 V and V_{ds} = 30 V is about 460 mA/mm for the proposed MESFET, while it is around 440 mA/mm for the BG-FP MESFET. It is found that the saturation current (I_{sat}) of the proposed structure at V_{gs} = 0 V is about 4.5% larger than that of the BG-FP structure and is about 6.2% at V_{gs} = –9 V and 8.1% at V_{gs} = –12 V. In addition, under low V_{ds}, the difference in I_{ds} is not as obvious as that in the saturation region because the trapping effect becomes more serious under a larger gate–drain bias. For the proposed structure, there exits a depletion at the spacer/channel interface, since the doping concentration in the spacer layer is designed two orders of magnitude lower than that in the channel, and the depletion extends mainly to the lower doped p-type spacer layer, which has little negative effect on drain current. When the spacer layer is under the control of the biased gate voltage, the surface traps can be considered "removed", which leads to a larger drain current compared with the conventional BG-FP structure MESFET.

Figure 4 illustrates the I_{ds} dependency on the dimensions of the p-type spacer layer. To characterize the effect of the spacer, different doping concentrations and thicknesses are designed. The results show that when the doping concentration in the spacer is two orders of magnitude lower than that in the channel, the depletion caused by the p–n junction has little neg-

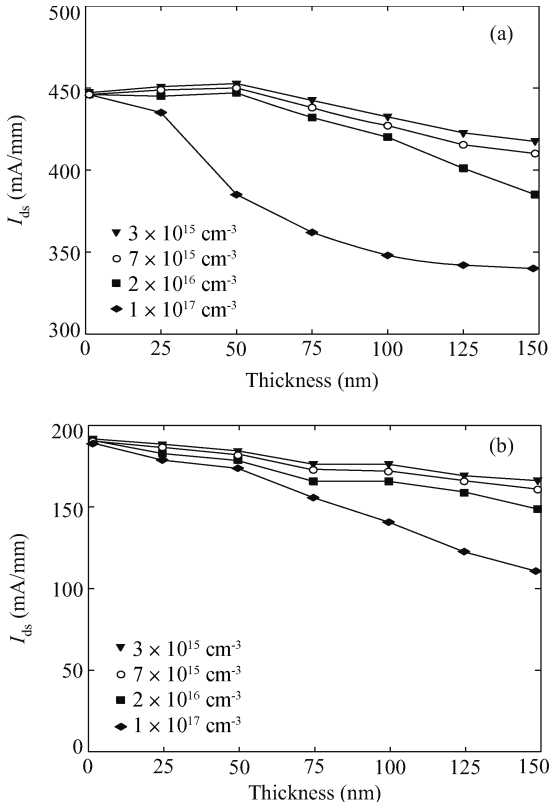

Fig. 4. Relationship between drain current and the dimensions of the p-type spacer layer under (a) $V_{gs} = 0$ V and (b) $V_{gs} = -9$ V.

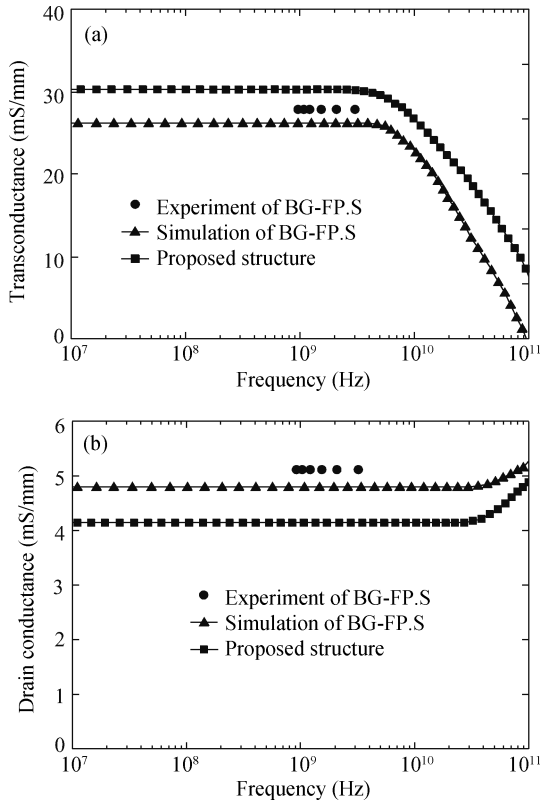

Fig. 6. Signal AC parameter curves versus frequency for (a) transconductance and (b) drain conductance.

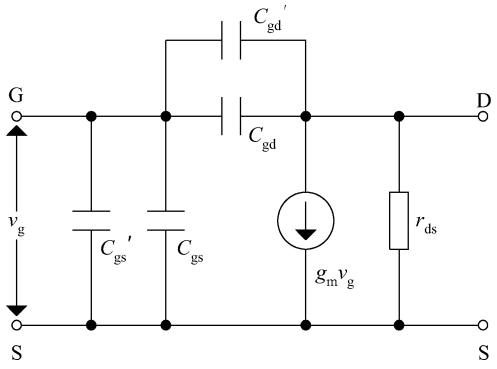

Fig. 5. AC equivalent circuit for a 4H-SiC MESFET with trap induced capacitance.

ative effect on I_{ds} in contrast with the surface traps, which results in an improvement in I_{ds}. As the doping concentration in the spacer increases, I_{ds} decreases as the depletion starts to extend to the channel region. When the doping concentration in the spacer becomes comparable with that in the channel, I_{ds} decays badly, as shown in Fig. 4(a). A similar situation can also be found in Fig. 4(b). However, deterioration of I_{ds} is not so severe, as shown in Fig. 4(a). In both cases, as the thickness of the spacer increases, the gate contact area to the spacer layer expands, thus more depletion region in the reverse-biased p–n junction is formed. Therefore, I_{ds} is reduced. To ensure that our proposed structure effectively improves the device properties, the p-type spacer layer is optimized to have a thickness of 50 nm and a doping concentration of 3×10^{15} cm^{-3}, and further studies are based on these dimensions.

Figure 5 shows the simplified small signal AC equivalent circuit for a 4H-SiC MESFET. As can be seen from the circuit, surface trap induced depletions are considered as extra capacitances on both sides of the gate.

The simulated small signal AC characteristics for both structures as a function of frequency at $V_{ds} = 60$ V and $V_{gs} = -17$ V are presented in Fig. 6. Figure 6(a) shows the simulated transconductance (g_m) curves versus frequency. It is obviously seen that g_m of a MESFET with the proposed structure is larger than that of a device with the BG-FP structure, which indicates that a MESFET with the proposed structure has better control on the drain current even at a frequency beyond the S band. Figure 6(b) shows the simulated drain conductance (g_d) curves versus frequency; in the saturation region, g_d is mainly determined by the effective channel length, for the BG-BF MESFET, the channel length is compressed by surface traps along the channel to the drain side, which means that it has a larger g_d than the proposed structure. Parameters for the BG-BF MESFET in AC simulation correspond with those in Ref. [15], unlike work in the DC simulation, L_g is set to 0.4 μm and the channel doping concentration is changed to 2.7×10^{17} cm^{-3}. Also, the experimental data are included for comparison.

Figures 7(a) and 7(b), respectively, show simulated gate–source capacitance (C_{gs}) and gate–drain capacitance (C_{gd}) curves versus frequency under the same bias condition. It can be seen that C_{gs} of the MESFET with the proposed structure is a bit larger than that of a device with a BG-FP structure, while C_{gd} of the device with the proposed structure is smaller than that of the device with a BG-FP structure in the whole fre-

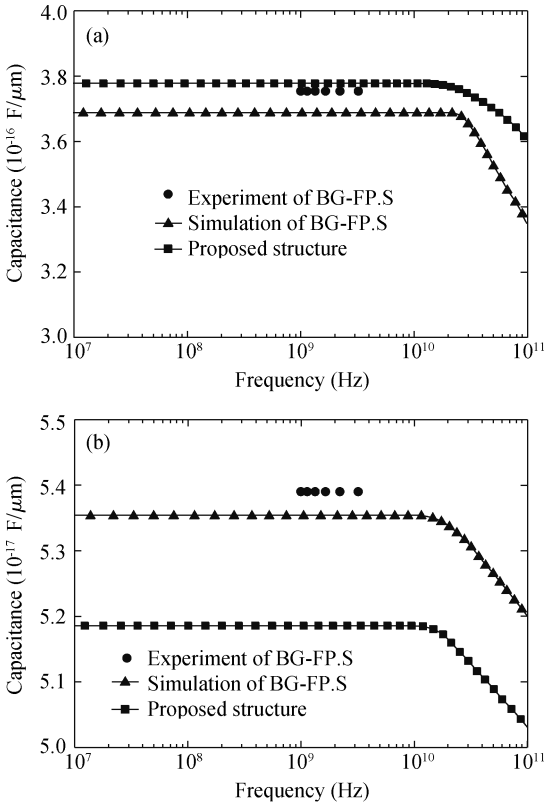

Fig. 7. Signal AC parameter curves versus frequency for (a) gate–source capacitance and (b) gate–drain capacitance.

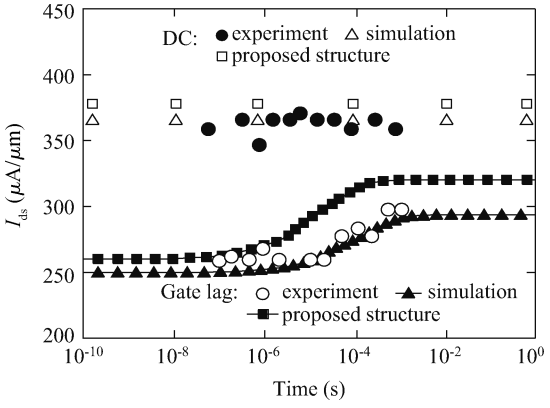

Fig. 8. Transient characteristics under $V_{ds} = 20$ V.

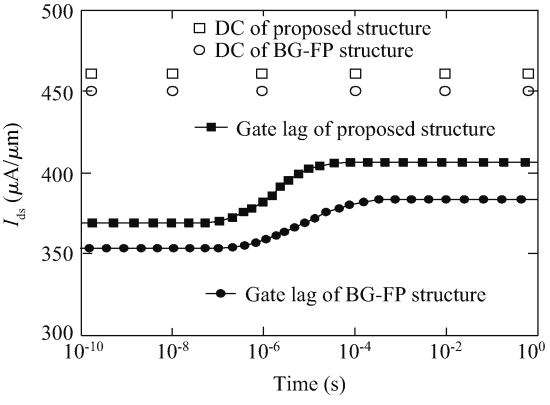

Fig. 9. Transient characteristics under $V_{ds} = 30$ V.

quency region (from 1 Hz to 100 GHz). On the drain side of the gate, since the electric field is much stronger than that on the source side, electrons are more likely to be ejected into surface traps. During the signal cycle, there is insufficient time for the trap states to be neutralized. Therefore the trap induced capacitance results in an addition to C_{gd}. For our proposed structure, the doping concentration in the spacer layer is designed to be two orders of magnitude lower than that in the channel, and the p-n junction depletion extends mainly to the lower doped p-type spacer layer. Compared to surface traps, spacer-induced depletion has a negligible effect on C_{gd}. Thus by isolating the surface traps, the proposed structure obtains a smaller C_{gd} compared with a BG-FP structure. On the other hand, a field-plate overlapped on the oxide plays a role that cannot be neglected in the C_{gd}, which may cause the deterioration of the output characteristics of MESFETs. For the proposed structure, an introduced p-type spacer can withstand part of the electric current brought by field field-plate, and the FP induced effect direct on the channel is mitigated. Therefore smaller FP induced depletion leads to smaller induced C_{gd}. In small signal and RF applications, the C_{gd} acts as a feedback capacitance at the output port, which limits the maximum stable gain (MSG). The MESFET with the proposed structure improves the degradation of the output drain current caused by C_{gd}. A smaller C_{gd} results from better suppression of surface traps and a smaller negative effect induced by the field-plate.

f_T and f_{max} in a small signal AC model for MESFETs obey the following two expressions,

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}, \tag{1}$$

$$f_{max} \leqslant f_T\sqrt{\frac{g_m}{g_d}}, \tag{2}$$

where g_m is the device transconductance, C_{gs} is the device gate–source capacitance, and g_d is the drain conductance. It can be calculated that the MESFET with the proposed structure has a $f_T = 11.1$ GHz and a $f_{max} = 28.5$ GHz, while those of a device with a BG-FP structure are 10.6 GHz and 24.2 GHz. There is a 5% improvement in f_T and a 17.8% improvement in f_{max}, respectively.

Figures 8 and 9 show the transient characteristics for MESFETs with two structures under different conditions. The gate voltages are stepped from the quiescent point to one specific final voltage while the drain current is simulated versus time. The gate lag simulation starts from pinch off $V_{gs} = -17$ V and $V_{ds} = 20$ V, to final voltage $V_{gs} = 0$ V and $V_{ds} = 20$ V. The result of a BG-FP MESFET fits the measured data well[13].

The gate-lag ratio is defined as the ratio of I_{ds} in transient mode (I_{dst}) and I_{ds} in quiescent mode (I_{dsq}), which indicates the trapping effect on the device during the microwave operation. As is revealed in Fig. 8, the value of I_{dst}/I_{dsq} is 88% for the proposed structure and 82% for the BG-FP structure.

The final voltage for the simulation shown in Fig. 9 is set to $V_{gs} = 0$ V and $V_{ds} = 30$ V to study the function of our proposed structure in high working conditions. The results show that the

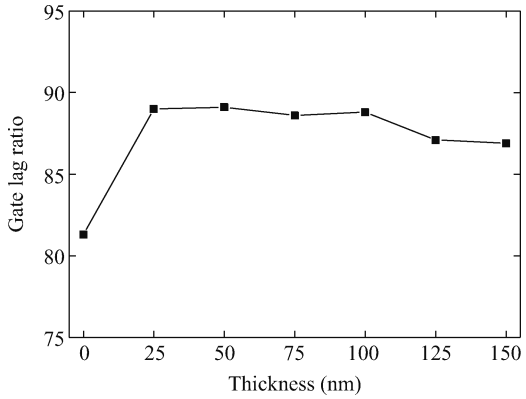

Fig. 10. Gate-lag ratio versus spacer thickness.

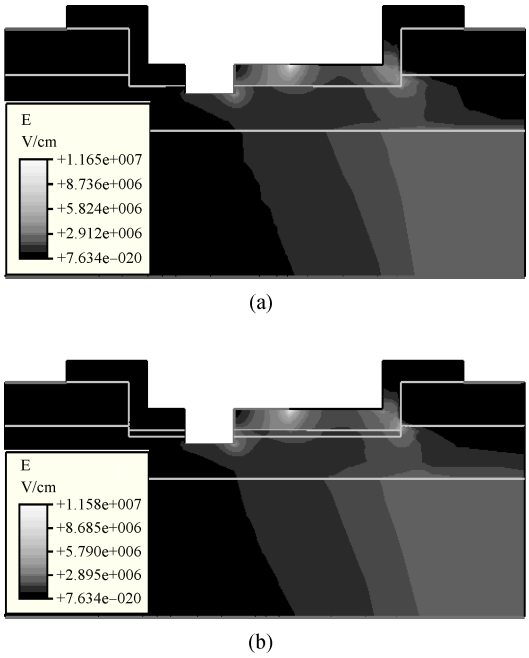

Fig. 11. 2-D electric field distribution simulated at V_{ds} over 200 V for (a) a BG-FP structure and (b) the proposed structure.

gate-lag ratio of both structures is somewhat decreased because the trapping problem is enhanced by the increase in drain voltage. Furthermore, the difference in I_{dst}/I_{dsq} is more obvious under a larger drain voltage for trapping phenomena and is more serious for a larger drive, where improvement brought by the proposed structure is proven. Figure 10 makes out the gate-lag ratio dependency on spacer thickness. The contact area between the Schottky gate and the p-type spacer layer increases with increasing spacer thickness, and equally the effective electrode area apply to the p–n junction is increased, which results in an addition to depletion in the p–n junction and causes a decrease in channel current. To obtain a favorable gate-lag ratio, the thickness of the spacer layer should not exceed a certain value for a MESFET with specific structural parameters.

For high power application, the power density is deduced from high output current and high working voltage, and the ability to endure as high a voltage as possible is significant to the performance of the device. For this consideration, the channel and the p-type spacer layer share the electrostatic potential.

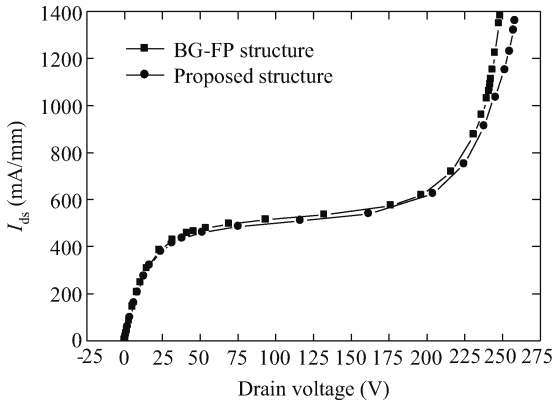

Fig. 12. Breakdown characteristics of a BG-FP structure and the proposed structure.

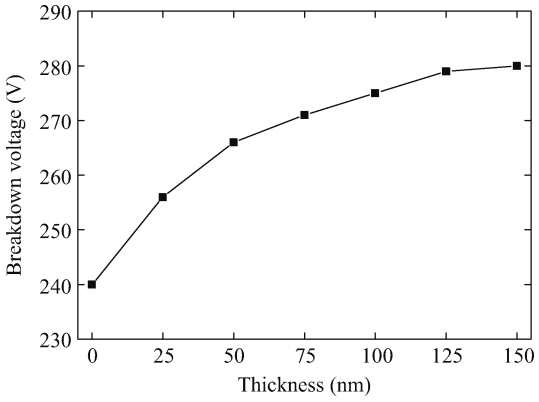

Fig. 13. Relationship between breakdown voltage and thickness of spacer.

Thus the electric field distribution is improved, especially at the drain side of the gate edge, as shown in Fig. 11.

The Thornber model[16] is utilized to characterize the ionization coefficients for breakdown simulation. Figure 12 shows the breakdown characteristics of a BG-FP structure and the proposed structure. Due to improved distribution of electric field, a MESFET with a P-type spacer layer and field-plate obtains a higher breakdown voltage. The maximum theoretical output power density for a Class A amplifier is given by[17]

$$P_{max} = \frac{I_{dsat}(V_b - V_{knee})}{8}, \tag{3}$$

where I_{dsat} is the saturation drain current density and V_{knee} is the knee voltage. According to Eq. (3), the maximum output power density of the proposed and conventional BG-FP MESFETs are about 11.2 W/mm and 9.5 W/mm, respectively.

Figure 13 illustrates the breakdown voltage dependency on spacer thickness. With the increase in thickness of the spacer layer, the breakdown voltage increases logarithmically. On condition that the desired output current is yielded, the thickness of the spacer should be designed to ensure as high a breakdown voltage as possible. In contrast, as discussed above, the thickness of the spacer layer should not exceed 100 nm to attain a large drain current. The favorable thickness of the spacer layer is optimized to be within the range from 50 to 100 nm.

4. Conclusion

A 4H-SiC MESFET with a p-type spacer layer incorporated into the field-plate structure has been proposed. By comparison with the well recognized BG-FP structure, it is revealed that this novel structure has a similar but more effective function than prior works in surface trap suppression by isolating the conductive channel from the surface trap induced depletion. Furthermore, spacer layer induced depletion has a less negative effect on the drain current than surface traps, and the decrease in C_{gd} leads to an increase in output drain current, especially in RF applications. In transient simulations, the proposed structure shows a favorable ratio of I_{dst}/I_{dsq} in the saturation region. Also, the proposed structure is proven to be applicable to high power applications. Moreover, the FP induced C_{gd} is somewhat reduced by a p-type spacer layer, which makes the proposed structure more competitive for microwave applications. The characteristics of the device depending on the parameters of the proposed structure have been discussed to provide a reference for device design.

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