Monolithically integrated enhancement/depletion-mode AlGaN/GaN HEMT D flip-flop using fluorine plasma treatment*

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Abstract: Depletion-mode and enhancement-mode AlGaN/GaN HEMTs using fluorine plasma treatment were integrated on one wafer. Direct-coupled FET logic circuits, such as an E/D HEMT inverter, NAND gate and D flip-flop, were fabricated on an AlGaN/GaN heterostructure. The D flip-flop and NAND gate are demonstrated in a GaN system for the first time. The dual-gate AlGaN/GaN E-HEMT substitutes two single-gate E-HEMTs for simplifying the NAND gate and shrinking the area, integrating with a conventional AlGaN/GaN D-HEMT and demonstrating a NAND gate. E/D-mode D flip-flop was fabricated by integrating the inverters and the NAND gate on the AlGaN/GaN heterostructure. At a supply voltage of 2 V, the E/D inverter shows an output logic swing of 1.7 V, a logic-low noise margin of 0.49 V and a logic-high noise margin of 0.83 V. The NAND gate and D flip-flop showed correct logic function demonstrating promising potential for GaN-based digital ICs.

Key words: AlGaN/GaN; fluorine plasma treatment; inverter; NAND gate; D flip-flop

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1. Introduction

AlGaN/GaN high electron mobility transistors (HEMT) are excellent candidates for integrated circuits used in elevated temperature and radiation environments owing to the wide bandgap[1−4]. They can work in high temperature environments, such as automotive, aviation, chemical reactor, and oil exploration systems, and hard radiation environments, such as space applications. Also, AlGaN/GaN 2DEG has a high electron mobility and it provides a semi-insulating substrate that produces a high switching current and lower parasitic capacitance, thus a higher operating speed is achievable in digital applications. Due to the lack of p-channel AlGaN/GaN HEMTs, a circuit configuration similar to that based on CMOS cannot be implemented yet. Using n-channel HEMTs, direct-coupled field-effect transistor (FET) logic (DCFL), as shown in Fig. 1, which features integrated enhancement/depletion-mode (E/D-mode) HEMTs, offers the simplest circuit configuration[5]. Recently, digital ICs based on integrated enhancement/depletion (E/D)-mode HEMTs have been demonstrated using a recess gate[3] and fluoride-plasma-treatment techniques[6].

In this paper, D flip-flop is demonstrated in a GaN system for the first time, and dual-gate enhancement-mode HEMTs are proposed to implement a NAND gate. The dual-gate AlGaN/GaN E-HEMT was integrated with conventional AlGaN/GaN D-HEMT to demonstrate a NAND gate. The fluorine plasma treatment enhancement-mode HEMTs had comparable characteristics to depletion-mode HEMTs. The detailed characteristics of the DCFL circuits, such as inverter and NAND gates fabricated by fluoride-based plasma treatment, were presented.

2. Device structure and fabrication

2.1. Circuit design

As shown in Fig. 1(a), the D-mode AlGaN/GaN HEMT with the gate connected to the source is used as a load device, and the E-mode AlGaN/GaN HEMT works as a drive device. The relative size of the two devices determines the output voltages, thus the inverter is ratioed. The ratio is $k = (W_E/L_E)/(W_D/L_D)$. In order to obtain satisfactory low output V_{OL}, an E-mode HEMT was designed with a gate width of 50 μm and a gate length of 0.8 μm, and a D-mode HEMT was designed with a gate width of 5 μm and a gate length of 1 μm, yielding a ratio of $k = 12.5$.

The NAND gate consists of one D-mode HEMT and two E-mode HEMTs, as shown in Fig. 1(b). We use one dual-gate device to implement the two E-mode HEMTs, which reduces the area. The dual-gate enhancement-mode HEMT structure is shown in Fig. 2. In order to produce the same V_{OL} as the inverter, the dual-gate E-mode HEMTs were designed with each gate width of 100 μm and the gate length of 0.8 μm, and the D-mode HEMT was designed to be the same size as the inverter.

The D flip-flop is widely used in digital circuits and systems for the storage of data. Figure 1(c) shows the circuit schematics of a negative edge-triggered D flip-flop. The D flip-flop consists of three inverters and eight NAND gates.

2.2. Circuit fabrication

The AlGaN/GaN HEMT layer was grown by metal organic chemical vapour deposition (MOCVD) on a sapphire substrate. The heterostructure consists of a nucleation layer, a 1-μm-thick

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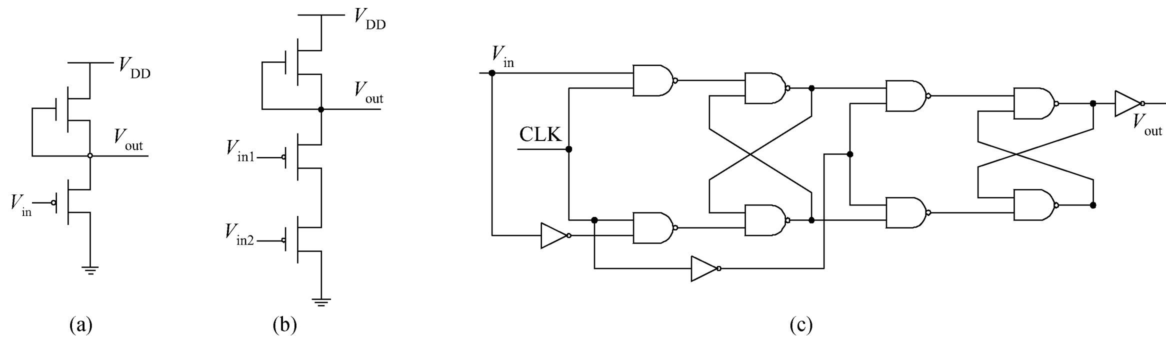

Fig. 1. DCFL circuit schematics of (a) an E/D inverter, (b) a NAND gate and (c) a D flip-flop.

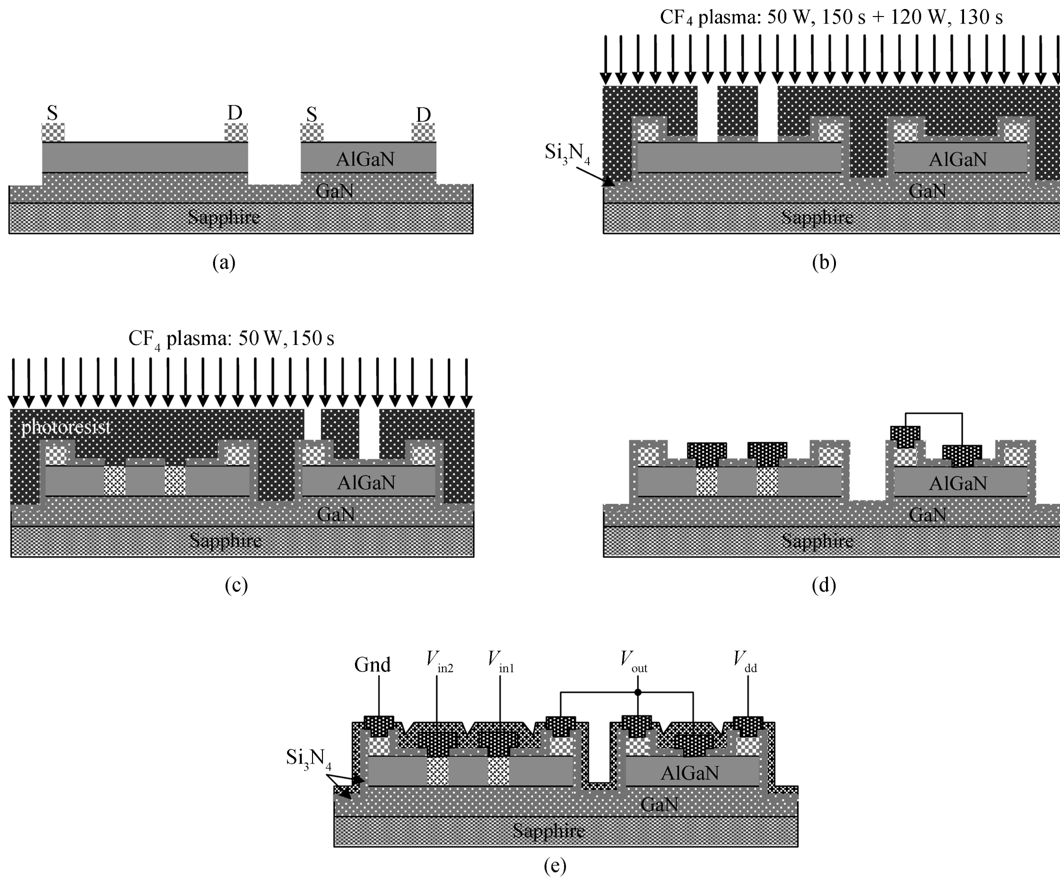

Fig. 2. Process flow of monolithic integration of dual-gate E-mode and D-mode HEMTs for a NAND. (a) Mesa etching and ohmic contacts formation. (b) E-mode HEMT gate definition and plasma treatment. (c) D-mode HEMT gate definition. (d) E/D-mode HEMT gate definition. (e) Interconnections.

GaN buffer layer, a 1.5-nm-thick AlN insert layer and an undoped 16-nm-thick AlGaN barrier layer. The AlN mole fraction of the AlGaN was 30%.

The monolithic integration process flow is shown in Fig. 2. After the formation of E/D-mode devices' mesas and source/drain ohmic contacts (Ti/Al/Ni/Au annealed at 870 ℃ for 30 s) [Fig. 2(a)], the 1st Si_3N_4 layer ($\sim$ 60 nm) was deposited on the sample by plasma enhanced chemical vapor deposition (PECVD). Then the E-mode gate windows with a 0.8 μm gate length were opened by photolithography, followed by CF_4 plasma treatment in a reactive ion etching (RIE) system, as shown in Fig. 2(b). This includes two steps: removal of the $Si_3N_4$with CF_4 plasma treatment of 50 W, 150 s, and incorporation of fluorine ions in the AlGaN with CF_4 plasma treatment of 120 W, 130 s. Figure 2(c) shows that the D-mode device gate windows with 1 μm gate length were opened by removing the Si_3N_4 with CF_4 plasma treatment of 50 W, 150 s. Subsequently, the E/D-mode device gate electrodes and the 1st interconnects are formed simultaneously [Fig. 2(d)]. The gate electrodes' top length is 1.2 μm for the E-mode device and 1.4 μm for the D/mode device to ensure that the gate electrode covers the entire plasma treatment gate region, leading to a T-gate configuration. The 2nd Si_3N_4 layer ($\sim$ 200 nm) is deposited by PECVD, and after the Si_3N_4 layer is removed from the source and drain ohmic contact regions, the 2nd interconnects are formed (Fig. 2(e)).

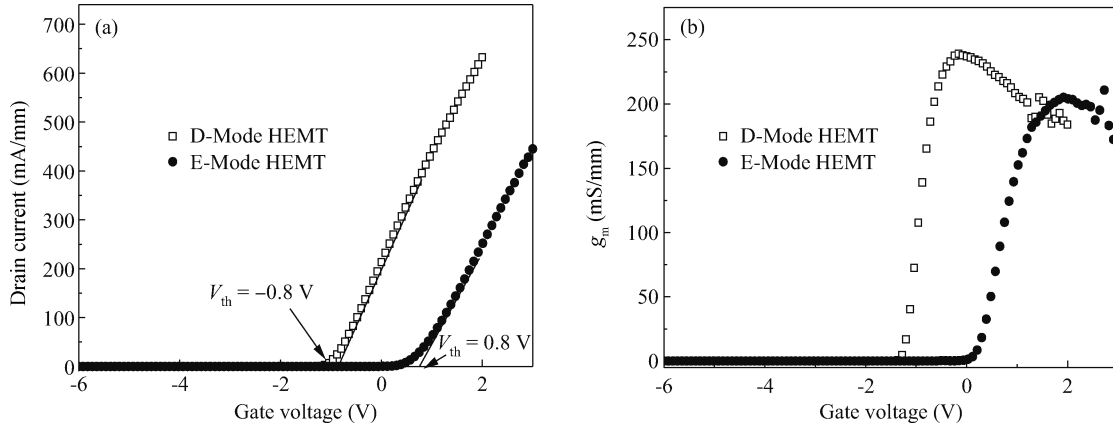

Fig. 3. (a) Transfer characteristics and (b) g_m characteristics of the E/D-mode HEMTs.

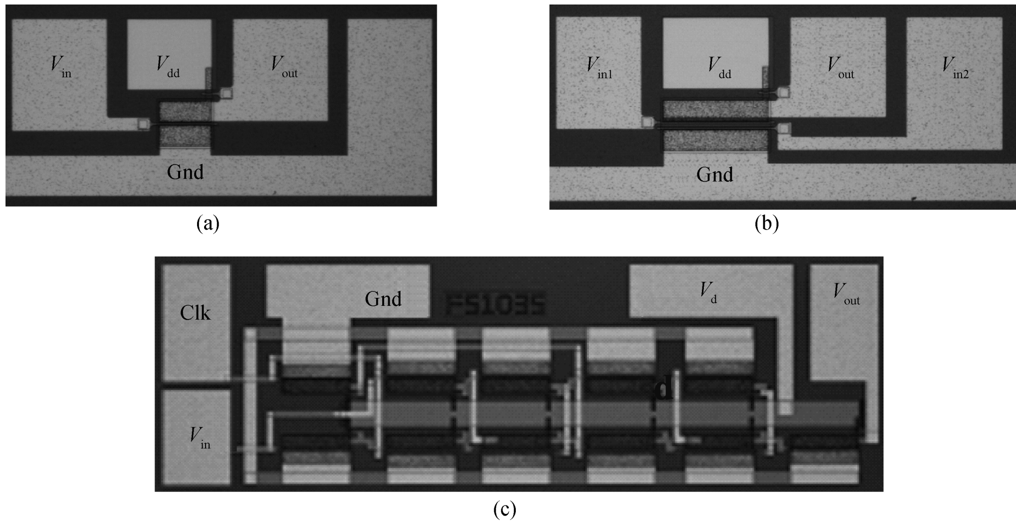

Fig. 4. Micrograph of (a) an inverter, (b) a NAND gate and (c) a D flip-flop.

3. Device and circuit characterization

3.1. Characteristics of discrete E/D-mode HEMTs

DC current–voltage (I–V) characteristics of discrete devices were measured by an Agilent B1500A parameter analyzer. Figure 3 shows the transfer characteristics of the E/D-mode HEMTs. The threshold voltage and peak transconductance are 0.8 V and 226 mS/mm for the E-mode HEMT, and –0.8 V and 219 mS/mm for the D-mode HEMT. The fluorine plasma treatment shifts the threshold voltage of the device due to two factors. First, CF_4 etches the AlGaN at a slow rate, with the CF_4 treatment condition of 150 W, 150 s, 4 nm thick recess being formed[7]. The depletion effect of the gate on the 2DEG is improved for a thinner AlGaN barrier. Second, the fluorine ions have a strong electronegativity and are negatively charged, effectively depleting the 2DEG in the channel. As a result, the threshold voltage can be shifted to positive values. The higher peak transconductance of the E-mode HEMT than that of the E-mode HEMT is due to the small gate length of the E-mode device. The threshold voltage of –0.8 V for the D-mode device is higher than the results reported previously, because the AlGaN barrier layer of 16 nm is thinner than that of the conventional heterostructure. The maximum current densities are 732 mA/mm and 512 mA/mm for the D-mode and E-mode devices, respectively.

3.2. Inverter

Figure 4(a) shows a fabricated inverter. Figure 5 shows the measured static voltage transfer curve of an inverter at a supply voltage of 2 V. High and low output logic levels (V_{OH} and V_{OL}) are 1.8 V and 0.1 V, respectively. The output logic swing defined as $V_{OH} - V_{OL}$ is 1.7 V. The static noise margins are 0.49 V and 0.83 V for the logic-low noise margin (NM_L) and the logic-high noise margin (NM_H), respectively. Figure 6 shows the transient voltage transfer curve of the inverter at the supply voltage of 2 V. The results show that the inverter works properly.

3.3. NAND gate

Figure 4(b) shows a fabricated NAND gate. As shown in Fig. 1(b), the NAND gate consists of a D-mode HEMT and an E-mode HEMT with two E-mode gates. Figure 7 shows the measured transient voltage transfer curve of a NAND gate at a supply voltage of 2 V. The output voltage turns low level only when the two input signals are both at high level, which is correct according to the regulation. The high and low output logic levels (V_{OH} and V_{OL}) are 1.9 V and 0.16 V, respectively.

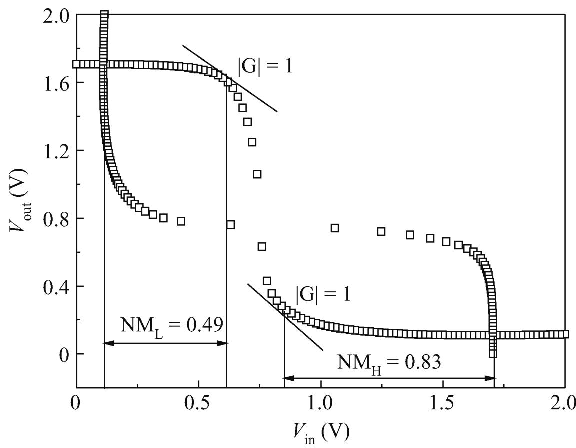

Fig. 5. The measured static voltage transfer curve of an inverter at a supply voltage of 2 V.

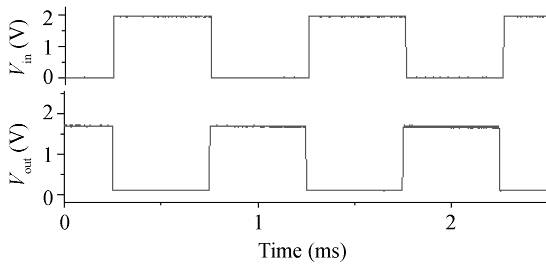

Fig. 6. Transient voltages transfer curve of an inverter.

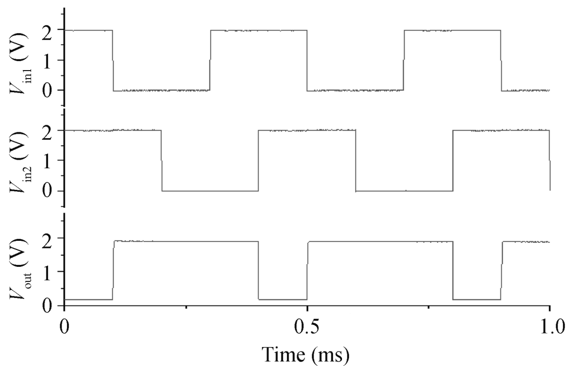

Fig. 7. Transient voltages transfer curve of a NAND gate.

3.4. D flip-flop

Figure 4(c) shows a fabricated D flip-flop. As shown in Fig. 1(c), the D flip-flop includes three inverters and eight NAND gates. Figure 8 shows the measured transient voltages of a D flip-flop at a supply voltage of 3 V and at the clock frequency of 500 Hz. The input signal transfers to the output when the clock is at the negative edge, and the output signal keeps constant at any other condition. The results show proper functions. The high and low output logic levels (V_{OH} and V_{OL}) are 2.7 V and 0.5 V, respectively.

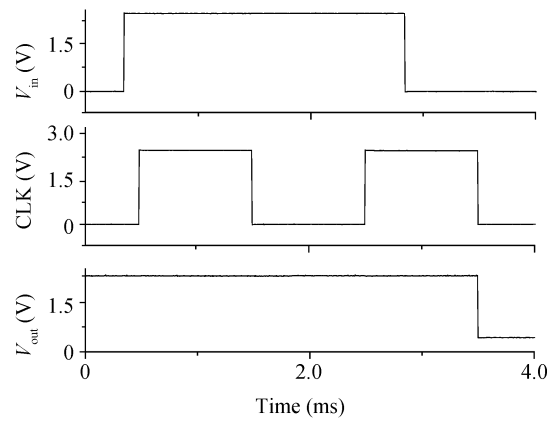

Fig. 8. Transient voltages transfer curve of a negative edge-triggered D flip-flop.

4. Summary

We have successfully demonstrated a D flip-flop integrated by E/D-mode HEMTs in the GaN material system based on the technique of fabricating a high-performance E-mode HEMT using fluoride-based plasma treatment. The D flip-flop consists of three inverters and eight NAND gates. The inverter consists of a D-mode HEMT and an E-mode HEMT, and the NAND gate consists of a D-mode HEMT and an E-mode HEMT with two E-mode gates. The static noise margins of the inverter are 0.49 V and 0.83 V for the logic-low noise margin (NM_L) and logic-high noise margin (NM_H), respectively. All circuits show proper functions.

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