Gate current modeling and optimal design of nanoscale non-overlapped gate to source/drain MOSFET

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Abstract: A novel nanoscale MOSFET with a source/drain-to-gate non-overlapped and high-k spacer structure has been demonstrated to reduce the gate leakage current for the first time. The gate leakage behaviour of the novel MOSFET structure has been investigated with the help of a compact analytical model and Sentaurus simulation. A fringing gate electric field through the dielectric spacer induces an inversion layer in the non-overlap region to act as an extended S/D (source/drain) region. It is found that an optimal source/drain-to-gate non-overlapped and high-k spacer structure has reduced the gate leakage current to a great extent as compared to those of an overlapped structure. Further, the proposed structure had improved off current, subthreshold slope and drain induced barrier lowering (DIBL) characteristics. It is concluded that this structure solves the problem of high leakage current without introducing extra series resistance.

Key words: gate tunneling current; analytical model; spacer dielectrics; DIBL; subthreshold slope
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1. Introduction

Leakage power has recently been recognized as a major challenge in the electronics industry. The desire to improve device performance has resulted in aggressive scaling of gate oxide thickness to below 2 nm. At such oxide thicknesses, there occurs an increased probability of tunneling of charge carriers through the gate oxide[1]. This has resulted in an alarming increase in gate leakage current. Gate leakage is predicted to increase at a rate of more than 500X per technology generation, while sub-threshold leakage increases by around 5X for each technology generation[2]. Thus, the reduction of gate leakage power dissipation is a primary concern for current research in the field of integrated circuits, especially for low power battery-operated portable applications[3].

Numerous effective techniques for controlling gate leakage have been proposed in the past. The work in Ref. [4] presented an approach to reduce $I_{\rm sub}$, but not $I_{\rm gate}$. The impact of $I_{\rm gate}$ on delay was discussed in Ref. [1], but its impact on leakage power was not addressed. In Ref. [5], the authors presented circuit-level techniques for gate leakage minimization. In each of these reports, extensive SPICE simulations were performed to obtain estimates of gate leakage. In Ref. [6], the authors addressed various leakage mechanisms, including gate leakage, and they presented a circuit level technique to reduce the leakage. However, this can be extremely time-consuming, especially for large circuits. In Ref. [7], the authors examined the interaction between $I_{\rm gate}$ and $I_{\rm sub}$, and their state dependencies. This work applied pin reordering to minimize $I_{\rm gate}$. In Ref. [8], Lee *et al.* developed a method for analyzing gate oxide leakage current in logic gates and suggested pin reordering to reduce it. Sultania *et al.*, in Ref. [9], developed an algorithm to optimize the total leakage power by assigning dual $T_{\rm ox}$ values to transistors. In Ref. [10], Sirisantana and Roy used multiple channel lengths and multiple gate oxide thickness to reduce leakage. Mohanty *et al.*[11] presented analytical models and a data path scheduling algorithm for the reduction of gate leakage current. In Ref. [12], a conventional offset gated MOSFET structure has been widely used to reduce subthreshold leakage but it does not address the issue of gate leakage reduction. Thus, the general problems of gate leakage reduction techniques are the need for additional devices (e.g. sleep transistors) and the reduction of only one component of leakage. Moreover, transistor level approaches are not applicable to standard cell designs and require a long calculation time. Further, gate level DVT-/DTOCMOS methods do not offer the best possible solution as the number of gate types limits the improvement.

To solve this problem, we propose a novel source/drain-to-gate non-overlap nano CMOS device structure for the first time to reduce the gate leakage current effectively because gate leakage current through the source/drain overlap region has been identified as the principal source of power dissipation in VLSI chips, especially in the sub-1-V range[13]. By adopting high-k dielectric spacers, we can induce a low resistance inversion layer as a S/D extension region in the non-overlap region and report various results regarding the proposed structure. An effective and compact model has been developed to analyze the gate tunneling current of gate to source/drain non-overlap N-MOSFET by considering the NSE (nano scale effect) effects that are difficult to ignore in the nano scale regime. The NSE effects include (1) the non-uniform dopant profile in the poly-gate in the vertical direction due to low energy ion implantation, (2) an additional depletion layer at the gate edges due to the gate length scaling down, and (3) a gate oxide barrier lowering due to image charges across the Si/SiO_2 interface. We also

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adopted advanced physical models in the simulation (Sentaurus simulator) to see other device characteristics, such as DIBL (drain induced barrier lowering), SS (subthreshold slope), on current and off current.

2. Theoretical gate current model

Modeling of the direct tunneling current analytically has been largely based on the WKB approximation[14]. The discrepancies that were presented in the original WKB approximation[14] have been rectified in Ref. [15] by introducing a few adjusting parameters. In our work, we adopt this model to evaluate the direct tunneling current from the channel and overlap region in the nano scale regime where poly gate dopant non-uniformity, gate length effects and gate oxide barrier lowering due to image charges across the Si/SiO_2 interface cannot be ignored. This model is more consistent and covers the entire gate bias range. The robustness of the model has been verified with Sentaurus simulation data. Because of the non overlap region between the gate-to-source and gate-to-drain, the edge direct tunneling current is absent and hence the total gate leakage current is given by

$$I_g = I_{gc} = J_{ch} L_g, \tag{1}$$

where L_g is the total gate length. The channel current density (J_{ch}) is modified for non-overlap MOSFET by using the current density in Ref. [15].

$$J_{(ch)} = A C_{F(ch)} T_{WKB(ch)}, \tag{2}$$

where $A = \frac{q^3}{8\pi\phi_{b_eff}\varepsilon_{ox}}$ and $C_{F(ch)}$ is the correction term incorporated in Ref. [15] and $T_{WKB(ch)}$ is the modified WKB transmission probability given as follows,

$$C_{(ch)} = \exp\left[\frac{20}{\phi_{b_eff}}\left(\frac{|V_{ox(ch)}| - \phi_{b_eff}}{\phi_{b_eff}} + 1\right)^{\alpha_{(ch)}} \times \left(1 - \frac{|V_{ox(ch)}|}{\phi_{b_eff}}\right)\right]\frac{V_g}{T_{ox}} N_{DTC(ch)}, \tag{3}$$

$$T_{WKB(ch)} = \exp\frac{-8\pi\sqrt{2m_{ox}}\phi_{b_eff}^{3/2}\left[1 - \left(1 - \frac{|V_{ox(ch)}|}{\phi_{b_eff}}\right)\right]^{3/2}}{3hq|E_{ox(ch)}|}, \tag{4}$$

$$N_{DTC(ch)} = \begin{cases} \frac{\varepsilon_{ox}}{t_{ox}} n_{acc} v_t \ln\left[1 + \exp\left(-\frac{V_g - V_{FB}}{n_{acc} v_t}\right)\right], & V_g < 0, \\ \frac{\varepsilon_{ox}}{t_{ox}} n_{inv} v_t \ln\left[1 + \exp\left(-\frac{V_g - V_{th}}{n_{inv} v_t}\right)\right], & V_g > 0, \end{cases} \tag{5}$$

where $\alpha_{(ch)}$ is the fitting parameter for channel tunneling and in this scheme, the value of $\alpha_{(ch)}$ for the channel region has been used as 0.73 to match the overall best fit with the Sentaurus simulation. T_{ox} refers to the physical oxide thickness and effective mass of the carrier in the oxide has been used as $0.40m_o$ throughout this work. The n_{inv} and n_{acc} are the swing parameters, V_{FB} represents the flat band voltage, $N_{DTC(ch)}$ denotes the density of carrier in the channel region depending upon the MOSFET biasing condition, and V_{ge} is the effective gate voltage excluding poly gate non-uniformity and gate length effect and is equal to $V_g - V_{poly}$, where V_{poly} is the voltage drop due to a poly depletion layer in the poly-Si gate. The default values of n_{inv} and n_{acc} are S/v_t (S is the sub threshold swing and v_t is the thermal voltage, equaling kT/q) and 1, respectively. ϕ_b is the actual barrier height of the gate insulator, i.e. the gate dielectric, and ϕ_{b_eff} is the effective barrier height, given as

$$\phi_{b_eff} = \phi_b - \Delta\phi, \tag{6}$$

$$\Delta\phi = \sqrt{\frac{qE_{gi}}{4\pi\varepsilon_{gi}}} = \sqrt{\frac{qV_{gi}}{4\pi\varepsilon_{gi}T_{gi}}} = \left(\frac{2q^3 N_{eff}\phi_{b_eff}}{16\pi^2\varepsilon_{gi}^3}\right)^{1/4}. \tag{7}$$

$\Delta\phi$ is the reduction in the barrier height at the high-k/Si interface from ϕ_b so that the barrier height becomes ϕ_{b_eff}. This reduction in barrier height is due to image charges across the interface. It is of great interest since it modulates the gate tunneling current. The voltage across the gate oxide for different regions of operation is

$$V_{ox} = \begin{cases} V_g - \phi_s - V_{FB}, & V_g > 0, \\ V_{ge} - \phi_s - V_{FB}, & V_g < 0, \end{cases} \tag{8}$$

where ϕ_s is the surface band bending of the substrate and is calculated for the channel region, depending upon the biasing condition of the MOSFET including the poly non-uniformity, gate length effects and image force barrier lowering. The accurate surface potential expressions for the channel in weak inversion/depletion, strong inversion and in accumulation can be taken from Ref. [16]. The gate effective voltage, including the effect of nonuniform dopant distribution in the gate, is derived as

$$V_{ge} = (V_{FB} + \phi_{so} - \Delta V_{p1} - \Delta V_{p2}) + \frac{q\varepsilon_{si}N_{poly}T_{gi}^2}{\varepsilon_{gi}^2} \times \left[\sqrt{1 + \frac{2\varepsilon_{gi}^2(V_g - V_{FB} - \phi_{so})}{q\varepsilon_{si}N_{poly}T_{gi}^2}} - 1\right]. \tag{9}$$

By taking the quantization effect into account, ϕ_{so} is given as[18]

$$\phi_{so} = 2\phi_s + \Delta\phi_s^{QM} - V_{BS}, \tag{10}$$

where $\Delta\phi_s^{QM}$ can be taken from Ref. [16]. Equation (9) includes the non uniformity in the gate dopant profile through a term ΔV_{p1} and fringing field effect (i.e. a gate length effect) through a term ΔV_{p2}. The potential drop ΔV_{p1} due to the non uniform dopant profile in the poly Si gate, caused by low energy implantation, is given by

$$\Delta V_{p1} = \frac{kT}{q}\ln\frac{N_{poly_top}}{N_{poly_bottom}}. \tag{11}$$

N_{poly_top} and N_{poly_bottom} are the doping concentration at the top and bottom of the polysilicon gate. The potential drop ΔV_{p2} due to the gate length effect, caused by very short gate lengths, is given as

$$\Delta V_{p2} \approx \frac{\Delta Q}{C_d} = \frac{2qAN_d}{L_g C_d} \quad (\text{V/cm}), \tag{12}$$

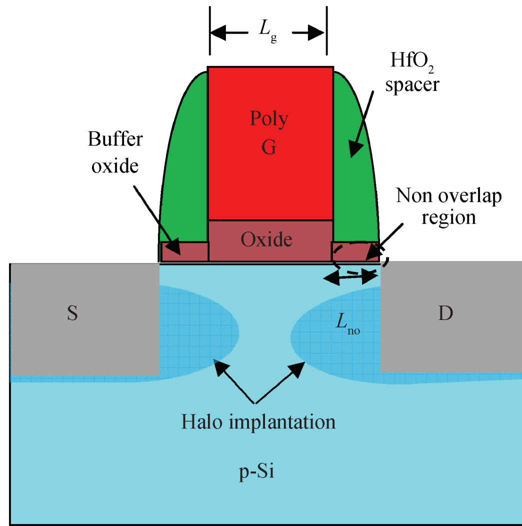

Fig. 1. Schematic cross-section of proposed N-MOSFET.

$$C_d = \delta \frac{\varepsilon_{ox}}{\pi} \ln \frac{3 - \cos \pi \dfrac{T_F - T_{ox}}{T_F}}{1 + \pi \dfrac{T_F - T_{ox}}{T_F}}, \tag{13}$$

where A denotes the triangular area of the additional charge, L_g is the gate length, C_d is the depletion capacitance in the sidewalls[18], ε_{ox} is the permittivity of the gate oxide, T_F is the thickness of the field oxide, T_{ox} is the thickness of the gate oxide and δ is the fitting parameter equal to 0.95 normally.

3. Device design

The N-MOSFET device cross-section with gate to source/drain non-overlap, designed for the analysis of the gate tunneling current characteristics, is shown in Fig. 1. The MOSFET has an n^+ poly-Si gate of physical gate length (L_g) 35 nm, gate oxide of 1.0 nm, and buffer oxide of 1.0 nm under high-k spacer. The buffer oxide is used to minimize the stress between the spacer and the substrate. The HfO_2, high-k dielectric, is used as a spacer after optimization. Here L_{no} represents the non-overlap length between the gate and the source/drain. The source/drain extension regions are created with the help of a fringing gate electric field by inducing an inversion layer in the non overlap region. The halo doping around the S/D also reduces short-channel effects, such as the punch-through current, DIBL, and threshold voltage roll-off, for different non-overlap lengths.

4. Simulation set up

Figure 2 shows the Sentaurus simulator schematic N-MOSFET, which has a non-overlapped gate to the S/D (source/drain) region. The doping of the silicon S/D region is assumed to be very high, 1×10^{20} cm^{-3}, which is close to the solid solubility limit and introduces negligible silicon resistance. The dimension of the silicon S/D region is taken as 40 nm long and 20 nm high. This gives a large contact area resulting in a small contact resistance. The doping concentration of the acceptors in the silicon channel region is assumed to

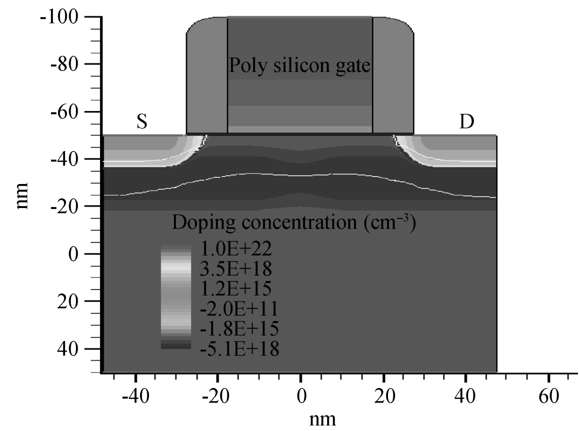

Fig. 2. Schematic cross-section of Sentaurus simulator image of 35 nm gate to S/D non overlapped NMOSFET.

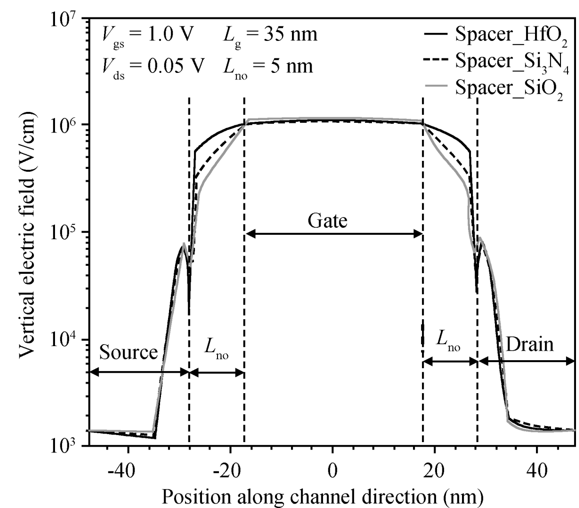

Fig. 3. Vertical electric field along channel for different spacers in the non overlap region.

be graded due to the diffusion of dopant ions from the heavily doped S/D region with a peak value of 1×10^{18} cm^{-3} and 1×10^{17} cm^{-3} near the channel. The poly-silicon doping has been taken to be 1×10^{22} cm^{-3} at the top and 1×10^{20} cm^{-3} at the bottom of the polysilicon gate, i.e. the interface of oxide and silicon. The MOSFET was designed to have V_{th} of 0.23 V. We determined V_{th} by using a linear extrapolation of the linear portion of the I_{ds}–V_{gs} curve at low drain voltages. The operating voltage for the devices is 1 V. The simulation study has been conducted in two dimensions, hence all of the results are in the units of per unit channel width.

The simulation of the device is performed by using the Sentaurus design suite[19], with drift–diffusion, density gradient quantum correction and the advanced physical model being turned on.

Figure 3 shows the simulated vertical electric field along the channel direction for different spacers in the non-overlap region for the non-overlap length of 5 nm. The vertical electric field is plotted for three different spacers such as HfO_2 (k = 22), Si_3N_4 (k = 7.5) and SiO_2 (k = 3.9). It is clear from Fig. 3 that the magnitude of the vertical electric field increases with an increase in the dielectric constant of the spacer. The verti-

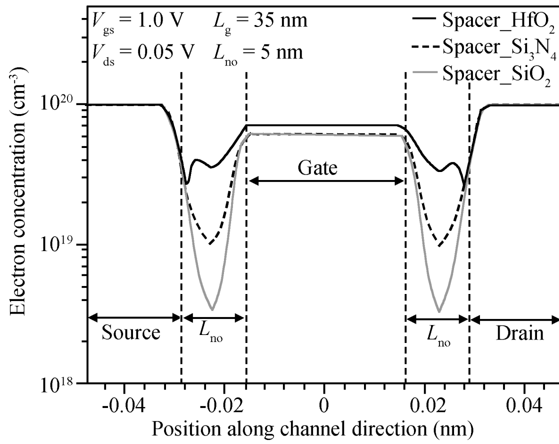

Fig. 4. Electron concentration along the channel for different spacers in the non overlap region.

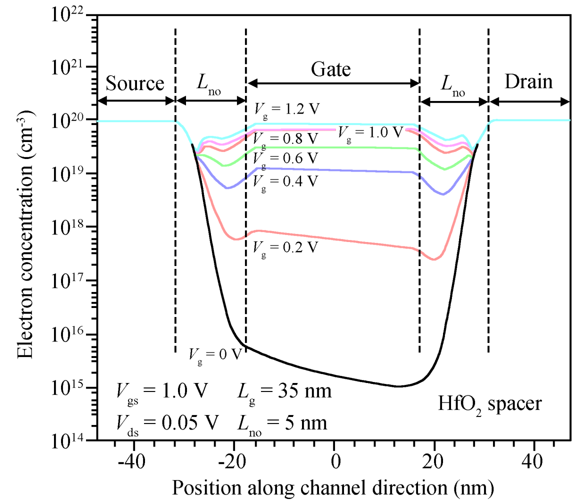

Fig. 5. Electron concentration along the channel under a HfO_2 spacer for different V_{gs} from 0.0 to 1.0 V with a 0.2 V step and at V_{ds} of 0.05 V.

cal electric filed is responsible for inducing an inversion layer in the non-overlap region. The results show that an approximately three times higher vertical electric field is obtained in the non-overlap region under a HfO_2 high-k spacer compared to the oxide spacer. This implies that the on-state current of the high-k spacer non-overlapped gate to the S/D MOSFET can be significantly larger than that of the oxide spacer MOSFET. This guides the use of a compatible high-k spacer to induce the sufficient inversion layer in the non-overlap region. It also shows that the vertical electric field magnitude decreases significantly with the distance of non overlap region from the gate edge, thereby limiting the non-overlap length (L_{no}).

Figure 4 plots the electron concentration along the channel for such as HfO_2 ($k = 22$), Si_3N_4 ($k = 7.5$) and SiO_2 ($k = 3.9$) in the non overlap region. The electron concentration below the spacer increases as the dielectric constant of the spacer material increases. This is due to the fact that the electron concentration under the spacer strongly depends on the intensity of the vertical fringing field, which is obvious from Fig. 3. At $V_{gs} = 1.0$ V, an electron concentration of more than 3×10^{19} cm^{-3} is induced under the spacer, which can act as an extended S/D region.

Figure 5 represents the variation in electron concentration along the channel direction for different V_{gs} from 0.0 to 1.2 V with a 0.2 V step and at V_{ds} of 0.05 V. It is observed from Fig. 5 that the electron concentration below the spacer increases as the gate bias increases. This figure shows that the gate bias controls the inversion layer effectively by the gate fringing field.

Thus, a reasonable amount of electron concentration was induced for the HfO_2 spacer with L_{no} less than 8 nm. L_{no} was also optimized with DIBL and the subthreshold slope (SS) (as shown in Fig. 9) and was found to be 5 nm.

5. Results and discussion

Computations have been carried out for an n-channel nanoscale non overlapped gate to S/D MOSFET to estimate the gate tunneling current. This model is computationally efficient and easy to realize.

A comparison between the simulated data and the model value for gate tunneling current is presented in Fig. 6. The figure shows the gate tunneling current versus gate bias for a non overlapped gate to S/D MOSFET with a HfO_2 spacer above the non-overlap region at an equivalent oxide thickness (EOT) of 1 nm and non-overlap length of 5 nm. It is shown in Fig. 6 that the result calculated by our model has better agreement with the simulated results certifying the high accuracy of the proposed analytical modelling.

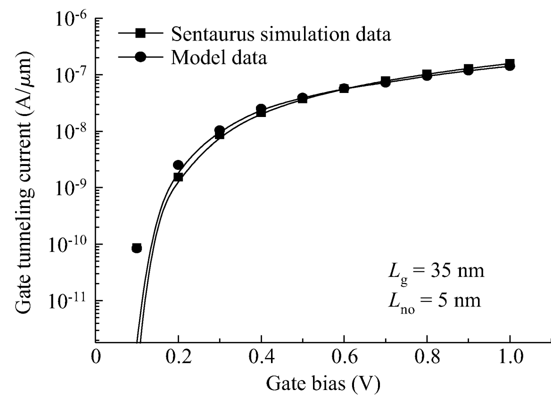

Fig. 6. Comparison of analytical model data with Sentaurus simulated data for a HfO_2 based high-k spacer MOSFET with equivalent oxide thickness (EOT) of 1.0 nm, physical gate length of $L_g = 35$ nm and S/D to gate non overlap length of $L_{no} = 5$ nm.

Figure 7 shows the variation in the gate tunneling current with gate bias for different non overlap lengths with a HfO_2 spacer above the non overlap region at an EOT of 1.0 nm. It is observed that the gate leakage current decreases significantly with a non overlap structure as compared to an overlapped structure, especially in the low gate bias range. At low gate bias, the formation of the channel just starts to begin so that the gate leakage current is mainly due to carrier tunneling through the gate to the S/D overlap region. The gate to S/D overlap region is absent in our designed MOSFET, so the gate tunneling (leakage) current is reduced to a greater extent. However, at a higher gate bias range, the gate tunneling (leakage) current is mainly due to the carrier tunneling through the channel region to the gate. Due to this region, the gate tunneling current is almost the same for an overlapped gate to S/D

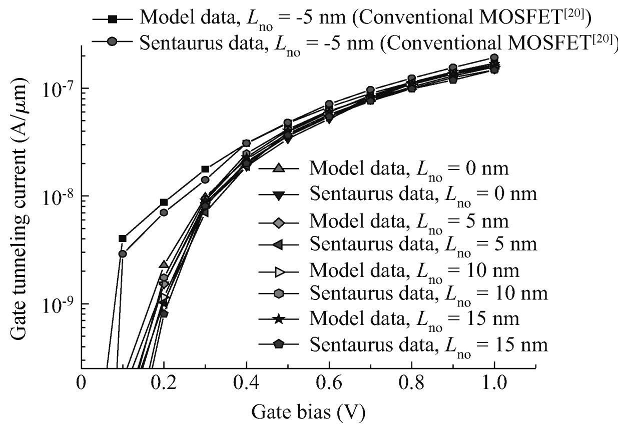

Fig. 7. Gate tunneling current versus gate bias for different gates to S/D non overlap length with EOT of 1.0 nm

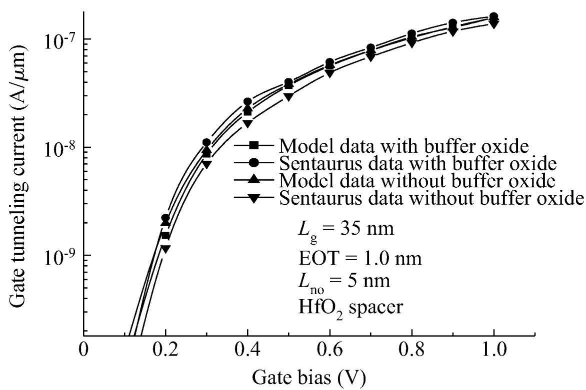

Fig. 8. Gate tunneling current versus gate bias with and without buffer oxide.

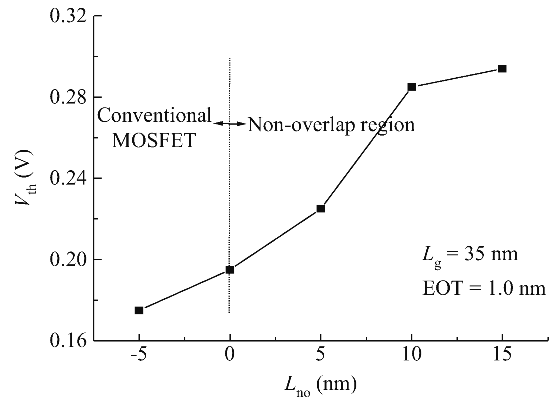

Fig. 9. Sentaurus simulation of threshold voltage versus non-overlap length with EOT of 1.0 nm.

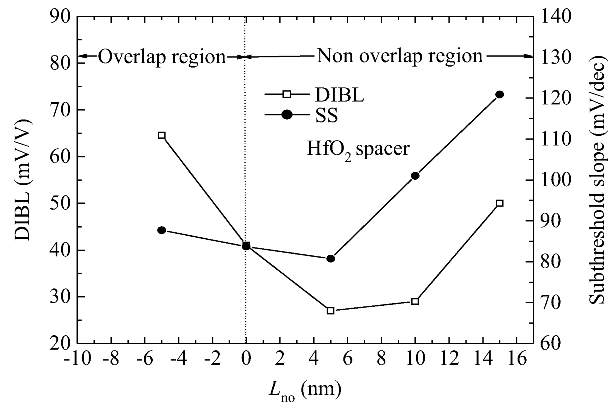

Fig. 10. Sentaurus simulation of DIBL, SS versus gate to S/D non overlap length of a NMOSFET with EOT of 1.0 nm.

MOSFET structure and non-overlapped gate to S/D MOSFET structure. However, marginal anomalous behavior in the case of $L_{no} = 15$ nm is observed. This may be due to the fact that as L_{no} increases beyond 10 nm, the barrier peak decreases (Figs. 4 and 5), as observed in the electron concentration profile due to which career tunneling increases slightly.

Figure 8 plots the gate tunneling current versus gate bias with and without a buffer oxide layer. It is observed that the gate leakage current increases without buffer oxide (SiO_2) because without buffer oxide the vertical E-field of the region is slightly enhanced.

Figure 9 plots the threshold voltage versus non-overlap length. It is observed that as the non overlap region increases, the channel area to be depleted by the vertical and fringing electric field from the gate widens, thereby increasing the threshold voltage. However, for L_{no} larger than 10 nm, the threshold voltage variation decreases due to an increase in metallurgical channel length.

Figure 10 shows the variation in DIBL and SS with a gate to S/D non overlap length of a NMOSFET. The DIBL effect is defined as the change in the threshold voltage ΔV_{th} divided by the change in the drain voltage ΔV_{ds}. It is observed in Fig. 10 that the drain induced barrier lowering (DIBL) is maximal for the overlapped gate to S/D MOSFET structure. This is due to the fact that the effect of the fringing field on the channel is maximal. Due to this decrease in gate control, the drain electrode is tightly coupled to the channel and the lateral electric field from the drain reaches a greater distance into the channel. Consequently, this electrically closer proximity of the drain to the source gives rise to higher drain-induced barrier lowering (DIBL) in the overlapped gate to S/D MOSFET structure. In the non-overlapped gate to S/D MOSFET structure, DIBL improves as the gate to S/D non overlap length (L_{no}) increases up to 5.0 nm because the lateral electric field from the drain reaches a shorter distance into the channel. This is due to an increase in the metallurgical gate length as compared with the conventional MOSFET structure in the same physical gate length. For L_{no} larger than 5 nm, DIBL degrades due to poor turn-on characteristics. The poor turn-on characteristics at low V_{ds} (0.05 V) are degraded by the barrier peaks under a HfO_2 spacer (shown in Fig. 4).

Figure 10 also shows that the subthreshold characteristics improve for the non overlapped gate to S/D MOSFET structure from L_{no} of about 0 to 5 nm as compared to the overlapped gate to S/D MOSFET structure. This represents one of the positive aspects of the non overlapped gate to S/D MOSFET structure. For L_{no} larger than 5 nm, SS degrades because the channel area to be depleted by the vertical and fringing electric field from the gate becomes wide, thereby increasing the depletion capacitance in the subthreshold equation. This increased depletion capacitance, in turn, degrades the SS. The result indicates that a non overlapped gate to S/D non NMOSFET with L_{no} of 5 nm is reasonable to achieve a very small DIBL of 27 mV/V

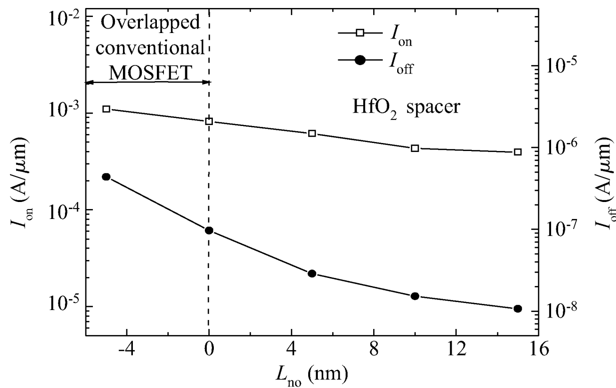

Fig. 11. Sentaurus simulation of on and off current versus gate to S/D non overlap length of a NMOSFET with EOT of 1.0 nm.

and a subthreshold slope of 80.75 mV/dec, and it is capable of suppressing the SCE.

The effect of non overlap length on both off and on current is plotted in Fig. 11. The on current defines the drain current when both the gate and the drain of the device are held at V_{DD} with the source being grounded. The off current defines the drain leakage current when the gate of the device is at low voltage below threshold voltage and the drain of the device is at high voltage (V_{DD}) with the source being grounded. It is observed in Fig. 11 that the on current slightly degrades with increasing non-overlap length due to increasing threshold voltage (V_{th}) and increasing source and drain series resistances with non overlap length. The off current decreases due to increasing threshold voltage and improved SS, thereby resulting in reduced subthreshhold leakage. The decrement in off current is more as compared to the decrement in on current, which in turn results in an enhanced I_{on}/I_{off} ratio greater than 3×10^4 at L_{no} of 5 nm.

6. Conclusion

In this work, we have extended the compact analytical gate current model to include the nano scale effect (NSE) for a new 35 nm non-overlapped gate to S/D non NMOSFET structure. It is found that with a fixed metallurgical gate length of 35 nm, the non-overlap gate to S/D MOSFET structure has shown a smaller gate tunneling current compared to the overlapped gate to S/D MOSFET structure. The gate tunneling current also deceases slightly with non-overlap length. It was found that the gate to channel control ability of the non-overlapped MOSFET structure can be significantly enhanced by using a high-k HfO_2 spacer. It is also shown that the source/drain non-overlap length of the nano device under consideration has been optimized with regard to the DIBL, SS and I_{on}/I_{off} current of the device. Based on these results, we conclude that the non-overlapped gate to S/D non-overlapped NMOSFET structure with L_{no} of around 5 nm is reasonable to reduce the gate tunneling current to a greater extent in addition to suppressing the SCE.

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