A 3 A sink/source current fast transient response low-dropout G_m driven linear regulator*

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Abstract: A 3 A sink/source G_m-driven CMOS low-dropout regulator (LDO), specially designed for low input voltage and low cost, is presented by utilizing the structure of a current mirror G_m (transconductance) driving technique, which provides high stability as well as a fast load transient response. The proposed LDO was fabricated by a 0.5 μm standard CMOS process, and the die size is as small as 1.0 mm^2. The proposed LDO dissipates 220 μA of quiescent current in no-load conditions and is able to deliver up to 3 A of load current. The measured results show that the output voltage can be resumed within 2 μs with a less than 1 mV overshoot and undershoot in the output current step from –1.8 to 1.8 A with a 0.1 μs rising and falling time at three 10 μF ceramic capacitors.

Key words: sink/source; linear regulator; load transient response; low-dropout
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1. Introduction

The phenomenal growth in mobile, PDA, battery-operated devices and other complicated portable, noise-sensitive equipment that need a high precision supply voltage, large output current and fast transient response has fueled the growth of the low-dropout regulator (LDO) due to its many advantages[1−3]. However, as the increasing large range output current and the increased system gain, the conventional compensation method cannot guarantee the system stability and achieve a fast load transient response. The bandwidth should be increased to obtain a fast load transient response while the gain of the LDO is reduced. In that case, the precision of the output voltage will be reduced[4, 5]. So the precision of the output voltage and the transient response are tradeoffs with LDO stability.

The common method to solve the above problems is to insert an additional buffer stage between the gain stage and the transfer transistors to push the parasitic poles at the gate of transfer transistors to a high frequency. This also increases the drive signal slew rate with a sacrifice of power consumption. The adaptive Miller compensation in Ref. [4] can solve the correlated tradeoffs in stability and precision with the decline of the load transient response, but the compensated zero will disappear when the LDO operates in a large output current and a low power supply condition.

According to the above analysis, it is desirable to have a LDO that is stable in the full output current range and has a fast load transient response. Based on the widely used architecture of the current mirror, a stable and fast load transient response LDO specially designed for low input voltage, low-cost and low-noise systems is implemented by pushing the pole generated at the gate of transfer transistors to high frequency, which eliminates the effect of the non-dominant pole with the method of reducing the impedance of the error amplifier. The LDO is designed as G_m driven. The voltage drop between the reference input and the output regulator is determined by the transconductance and output current of the device. The G_m of the LDO changes with respect to the output current in order to conserve the quiescent current. Both a fast load transient response and a high precision output voltage are achieved. The class AB output stage makes it possible to sink and source a maximum 3 A output current. Moreover, a novel quiescent current control circuit is presented in this paper that perfectly controls the quiescent current of the class AB output stage.

2. Circuit design

2.1. Architecture of the proposed LDO

Figure 1 shows the diagram and off chip components of the proposed LDO. The block of COMP together with Mirror 1 comprises the G_m driven of gmH when the LDO source current. Similarly, the G_m driven section of sink current gmL comes from the block of COMP and Mirror 2. The proposed LDO regulator is a single pole system. Based on two current adders, the block IQ_Control perfectly controls the quiescent current of the class AB output stage.

2.2. Stability of the proposed LDO

Only one low-frequency pole has to be taken into consideration when the frequency response of the LDO's open loop transfer function is evaluated. The low frequency pole lies at the output node VOUT because the large off-chip capacitor C_L of about 30 μF is attached at the output node to obtain a good

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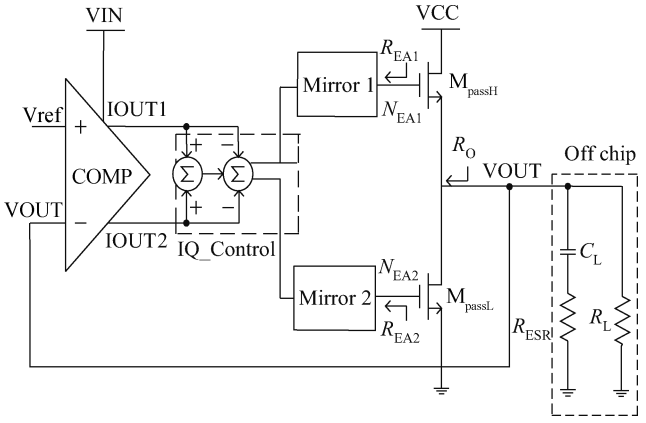

Fig. 1. Structure of the proposed LDO.

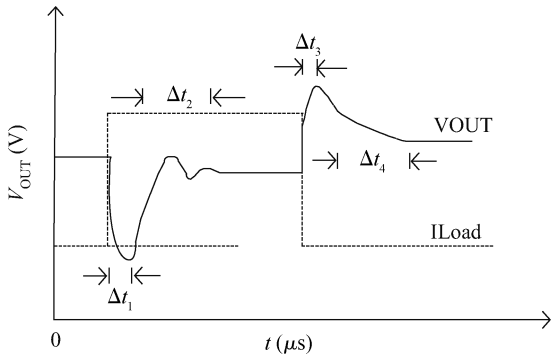

Fig. 2. Load transient response for a typical LDO.

transient response. The other traditional low-frequency pole at the output nodes N_{EA1} and N_{EA2} is pushed to high frequency according to the error amplifier's low output impedance in the full output current range. The distance between the two poles is now large enough to guarantee only one pole in the unity gain bandwidth. The unity gain bandwidth for the voltage loop is determined by the output capacitance, as a result of the bandwidth nature of the G_m, which is given by

$$\mathrm{GBW} = \frac{G_m}{2\pi C_L}. \tag{1}$$

If the internal poles of the error amplifier are ignored, the loop transfer function of the proposed LDO can be expressed as

$$H(s) = \frac{A_0\left(1+\dfrac{s}{\omega_z}\right)}{\left(1+\dfrac{s}{\omega_{P1}}\right)\left(1+\dfrac{s}{\omega_{P2}}\right)}, \tag{2}$$

where A_0 is the DC loop gain, which is given by

$$A_0 = G_m(R_O // R_L), \tag{3}$$

where G_m and R_O are the transconductance and output impedance of the proposed LDO, respectively.

The poles and zero of $H(s)$ can be expressed as

$$P_1 \cong \frac{1}{2\pi(R_O // R_L)C_L}, \tag{4}$$

$$P_2 = \frac{1}{2\pi R_{EA1(2)} C_{OH(L)}}, \tag{5}$$

$$Z_1 = \frac{1}{2\pi R_{ESR} C_L}, \tag{6}$$

where C_{OH} (C_{OL}) is the equivalent capacitance of the error amplifier while $R_{EA1(2)}$ is its output impedance when the LDO source (sink) current. R_{ESR} is the equivalent series resistance (ESR) of the off-chip capacitor. With P_2 and Z_1 far away from the unit-gain bandwidth, the proposed LDO is designed as a single pole system no matter what the output current is.

2.3. Load transient response of the proposed LDO

The response time and maximum allowable output voltage change for a full range transient load-current step are important specifications of LDOs. Figure 2 shows the typical load transient response waveforms of an output current step, where Δt_1 and Δt_3 represent the response times while Δt_2 and Δt_4 are the setting times. The expression of Δt_1 is given by

$$\Delta t_1 \approx \frac{1}{\mathrm{BW_{cl}}} + t_{sr} = \frac{1}{\mathrm{BW_{cl}}} + C_{pass}\frac{\Delta v}{I_{sr}}, \tag{7}$$

where $\mathrm{BW_{cl}}$ is the closed-loop bandwidth of the system, C_{pass} is the parasitic capacitance of the pass transistors $\mathrm{M_{passH}}$ ($\mathrm{M_{passL}}$), t_{sr} is the slew rate time associated with C_{pass}, I_{sr} is the slew rate limited current, and ΔV is the output voltage variation at C_{pass}.

Δt_3 is also inversely proportional to the closed-loop bandwidth, but it does not put pressure on the current restrictions. As predicted by Eq. (7), Δt_1 and Δt_3 can be improved by increasing the closed-loop bandwidth and slew rate current. The setting time Δt_2 is dependent on the phase margin of the open-loop frequency response while Δt_4 is determined by the feedback resistors' current. Because the proposed LDO is a single pole G_m driven LDO and the slew rate current is not limited, the fast load transient response can be achieved.

3. Circuit realization

3.1. Detailed stability analysis

The corresponding schematic diagram of Fig. 1 is illustrated in Fig. 3. Based on the above described architecture of the current mirror, the gain of the LDO when the source (sink) current is

$$A_0 = K g_{m1(2)} \times (R_O // R_L), \tag{8}$$

where

$$R_O = \frac{1}{g_{mMpassH}} // r_{ds\_MpassH} = \frac{1}{\sqrt{2\mu_p C_{ox}\left(\dfrac{W}{L}\right) I_O} + \lambda I_O}, \tag{9}$$

or

$$R_O = r_{ds\_MpassL} = \frac{1}{\lambda I_O}. \tag{10}$$

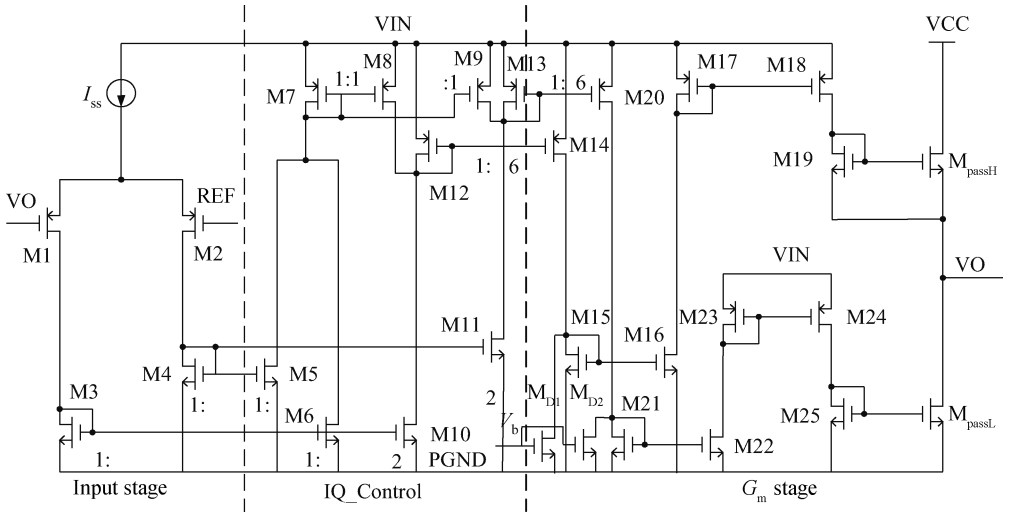

Fig. 3. Schemetic view of the proposed LDO.

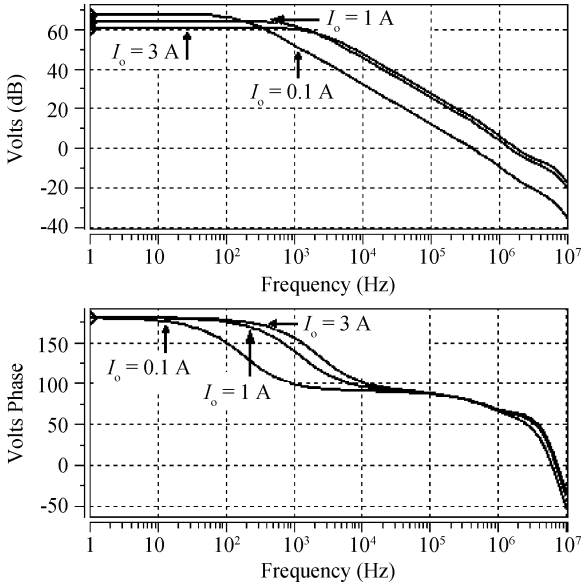

Fig. 4. Simulated bold plots for different load conditions.

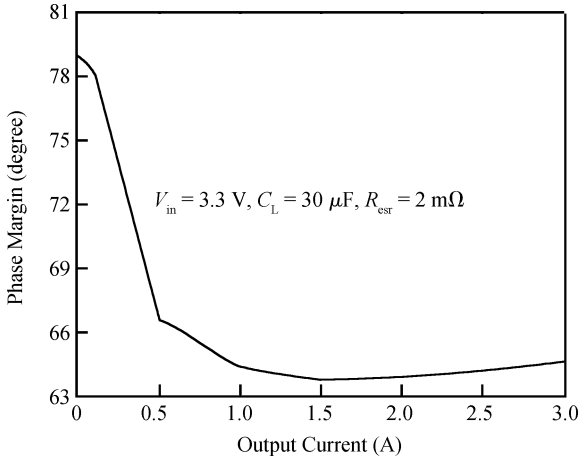

Fig. 5. Phase margin versus output current.

When the source (sink) current, K is the ratio factor of the current mirror from M3 (M4) across M10 (M11) to M_{passH} (M_{passL}), and $g_{m1(2)}$ is the transconductance of M1 (M2).

The poles of the circuit are

$$P_1 \cong \frac{1}{2\pi(R_O // R_L)C_L}, \tag{11}$$

$$P_2 = \frac{1}{2\pi R_{EA1(2)}C_{OH(L)}} = \frac{\sqrt{2\alpha(\beta)\mu_n C_{ox}\left(\frac{W}{L}\right)I_O}}{2\pi C_{OH(L)}}, \tag{12}$$

where $\alpha(\beta)$ is the reciprocal of the ratio factor of the current mirror from M19 (M25) to M_{passH} (M_{passL}). So the distance between P_1 and P_2 can be properly set through the value of α to guarantee that there is only one pole in the unity gain bandwidth. The simulated bold plots for different output current conditions are shown in Fig. 4, and the phase margin at different output currents is shown in Fig. 5. The results show that the phase margin of the proposed LDO is more than 60° in the worst case and is absolutely stable at any time.

3.2. Detailed load transient response analysis

The architecture of the current mirror achieves low output impedance for the error amplifier, which improves the speed to charging and discharging the parasitic capacitors at the gate of the pass element M_{passH} (M_{passL}). The slew rate limit current, $I_{sr} = K\alpha(\beta)\, g_{m1(2)}\, |V_{OUT} - V_{REF}|$, follows the output current. Now the response time can be calculated by

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{12\pi C_L}{K g_{m1(2)}} + \frac{C_{pass}}{K\alpha(\beta) g_{m1}}. \tag{13}$$

3.3. Realization of quiescent current control circuits

The circuit, namely IQ_Control, perfectly controls the quiescent current of the class AB output stage that changes with the mismatch of the devices and inherent process drift. Assuming that the current flow through input pairs M1 and M2 is I_{M1}

Table 1. Performance summary and comparison of different fast load transient LDOs.

Parameter	Ref. [7]	Ref. [8]	Ref. [9]	Ref. [10]	This work
Process (μm)	0.09	0.5	0.5	0.35	0.5
V_{in} (V)	1.2	—	2.2–5.5	1.2	2.4–6
V_{out} (V)	0.9	1.8	1.6	1	0.6–1.3
Dropout voltage (mV)	300	650	200	200	350
$I_{loadmax}$ (A)	0.1	3	0.2	0.1	3
I_Q @ no load (μA)	6000	1000	2.3	100	220
C_{out} (μF)	0.0006	4.7	1	—	30
ΔV_{out} (mV)	90	180	53	—	30
T_R (μs)	0.00054	0.282	0.275	2.8	0.25

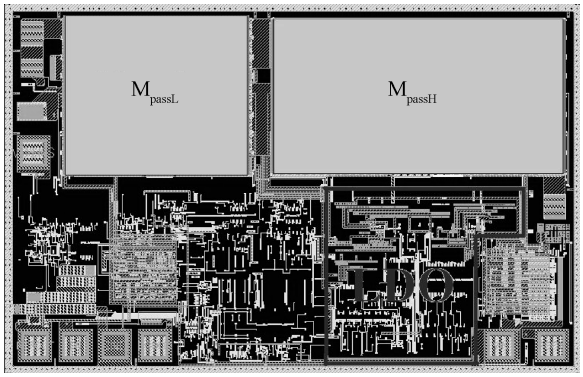

Fig. 6. Layout of the proposed LDO.

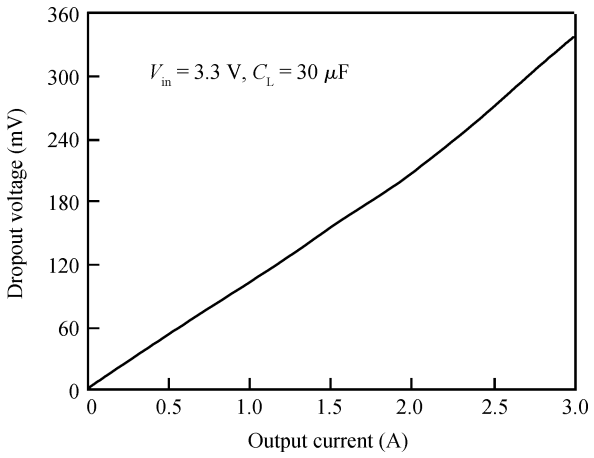

Fig. 7. Dropout voltage versus output current.

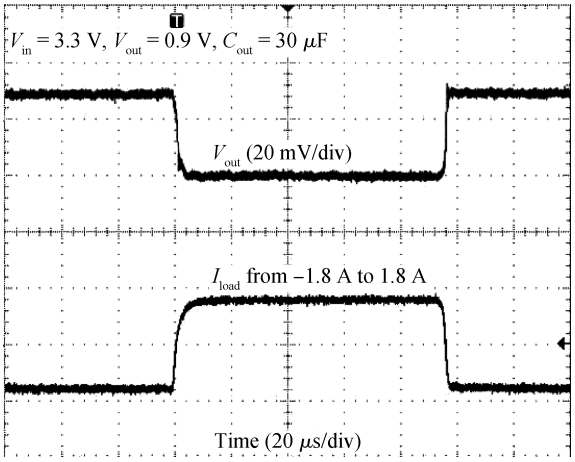

Fig. 8. Measured load transient response.

$= 0.5I_{ss} + I'$, $I_{M2} = 0.5I_{ss} - I'$, it can be derived that $I_{M7} = I_{M5} + I_{M6} = 2(I_{M1} + I_{M2}) = I_{ss}$, $I_{M12} = I_{M10} - I_{M8} = 2I'$, $I_{M13} = I_{M11} - I_{M9} = -2I'$. The value I', which represents the current difference between input pairs, is very small. The current though MD1 and MD2 is $0.25I_{ss}$, which can guarantee the transistors M15 and M21 in the cut-off region that the current through M_{passH} and M_{passL} is zero.

4. Test results

The proposed LDO shown in Fig. 3 was fabricated by standard double-poly trinal-metal 0.5 μm CMOS technology. It can be used in a memory termination regulator for DDR, DDR2 and DDR3. The layout of the proposed LDO is shown in Fig. 6, and the die area is 1 mm^2. The quiescent current is 220 μA at no-load and 0.9 V output voltage conditions, and the maximum output current is 3 A with a dropout voltage of 350 mV. Moreover, the measured dropout voltage at different output currents is shown in Fig. 7.

The measured load transient response of the proposed LDO is shown in Fig. 8. This shows that the proposed LDO can respond quickly within 1us and recover to the preset output voltage within 2 μs with three 10 μF ceramic output capacitors that the ESR should be less than 10 mΩ. Moreover, the fast response time is beneficial to reduce overshoot and undershoot voltage, and a less than 1 mV deviation is recorded with the output current switching between –1.8 and 1.8 A. According to Ref. [7], the response time, T_R, is given as

$$T_R = \frac{C_L \Delta V_{OUT}}{I_{LOAD}(\max)} = \frac{30\,\mu\text{F} \times 30\,\text{mV}}{3.6\,\text{A}} = 0.25\,\mu\text{s}. \quad (14)$$

The measured line transient response of the proposed LDO with an input voltage of 3 to 5 V is shown in Fig. 9. This shows that both the overshoot and the undershoot are less than 16 mV, and the output voltage can recover to the preset voltage within 3 μs.

The LDO's main performances are summarized in Table 1 and compared with recently published fast load transient response LDOs[7–10]. The response time of Refs. [7, 8] is smaller than the proposed LDO, while the quiescent is much larger. References [9, 10] consume ultra low power with very slow response time. Both low power consumption and a fast response are achieved in the proposed LDO.

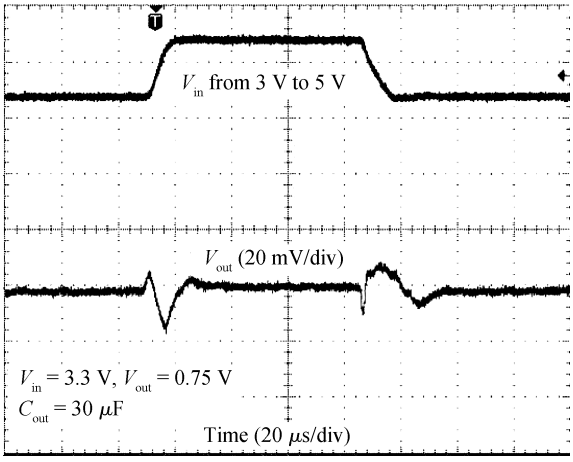

Fig. 9. Measured line transient response.

5. Conclusion

By eliminating the pole at the gate of pass transistors with the architecture of current mirrors, a novel LDO with a maximum 3 A output current and fast load transient response is implemented. Both sink and source currents are achieved with the class AB output architecture. The LDO achieves the stability in full output current range with a wide bandwidth, and only requires a minimum capacitance of 20 μF. The fabricated IC achieves a very fast response time with less than 1 mV overshoot and undershoot within a 1 μs response time.

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