# High-precision high-sensitivity clock recovery circuit for a mobile payment application*

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**Abstract:** This paper presents a fully integrated carrier clock recovery circuit for a mobile payment application. The architecture is based on a sampling-detection module and a charge pump phase locked loop. Compared with clock recovery in conventional 13.56 MHz transponders, this circuit can recover a high-precision consecutive carrier clock from the on/off keying (OOK) signal sent by interrogators. Fabricated by a SMIC 0.18-$\mu$m EEPROM CMOS process, this chip works from a single power supply as low as 1.5 V. Measurement results show that this circuit provides 0.34% frequency deviation and 8 mV sensitivity.

**Key words:** clock recovery; mobile payment; PLL; OOK; RFID
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## 1. Introduction

Mobile payment is a new and rapidly adopting alternative payment method. Currently, there are four primary models for mobile payment: short message service (SMS) payment, direct mobile billing, mobile web payment and contactless near field communication payment. The "RFID on subscriber identity module (SIM) card" model has been considered as one of the most promising solutions among contactless near field communication payment. In this solution, the RFID tag chip and antenna are integrated into the SIM card and powered by phone battery, which allows potential users to keep their existing handsets and only change the SIM card in order to use the payment function. However, because the RF signal is maximally attenuated to several mV by the shielding effect of equipment shells, the envelope detector used in most HF RFID system fails in this application. A coherent detector is adopted due to its high demodulation sensitivity. A consecutive local clock for the mixer in a coherent detector is necessary. However, limited by the size of the SIM card, an extra device, such as a crystal, is avoided. Therefore, a critical task in such a detector is the recovery of the carrier clock embedded in the OOK data stream, which takes place using the modulation principle of 100% ASK of the RF operating field to create a "pause"[1].

There have been several papers published regarding clock recovery in a 13.56 MHz RFID transponder[2−5]. However, the solutions[2−4] only provide a discontinuous clock because of the "pause" generated by OOK modulation in the carrier. Although Reference [5] can provide the consecutive clock, low sensitivity to OOK signal leads to high frequency deviation, which increases the probability of error demodulation. In particular, under the mobile payment application, it tends to fail due to the weak OOK signal.

This paper presents a new topology of consecutive clock recovery (CR) with a sampling phase frequency detector (PFD) suitable for use in a phase-locked loop (PLL) clock recovery system in low-voltage CMOS technology. High sensitivity is achieved through the sampling structure, which ensures little frequency deviation. The system architecture and detailed analysis of the system for mobile payment are given. Circuit implementation and measurement results are also shown.

## 2. System design

### 2.1. Architecture of clock recovery circuit

Figure 1 shows the block diagram of the CR circuit, which includes a sampling circuit, lock detector and charge-pump phase-locked loop (CP-PLL). The first part of the topology is a conventional CP-PLL marked by a dashed dotted line in Fig. 1. A ring-oscillator is preferred in the MHz band rather than an LC tank due to the unacceptable area consumption and low quality factors of on-chip inductors. A two-order loop filter with high proportional capacitance is adopted. The structure of the auxiliary switch is used in the charge pump, which expands the charge pump current when the PLL is in the tracking state. This effectively reduces the setup time of the PLL.

As marked with a dashed line in Fig. 1, the second part of the topology is a sampling-detection loop, which is mainly composed of a lock detector and a sampling circuit. The loop action can be expressed as follows. (1) Before "pause" appears, the PLL freely tracks the comparator clock. Meanwhile, the VCO clock samples the comparator clock and the lock detector detects the difference between the UP and DOWN signals. If the lock detector judges that the recovered clock is identical to the comparator clock, the detector gives a valid LOCKD signal. Then the sampling result is sent to the ENABLE signal. Otherwise, ENABLE is set to "1". Different ENABLE values decide whether the PFD should be locked. (2) When "pause" occurs, if the recovered clock is identical to the comparator clock, the sampling circuit will find the "pause" and the corresponding

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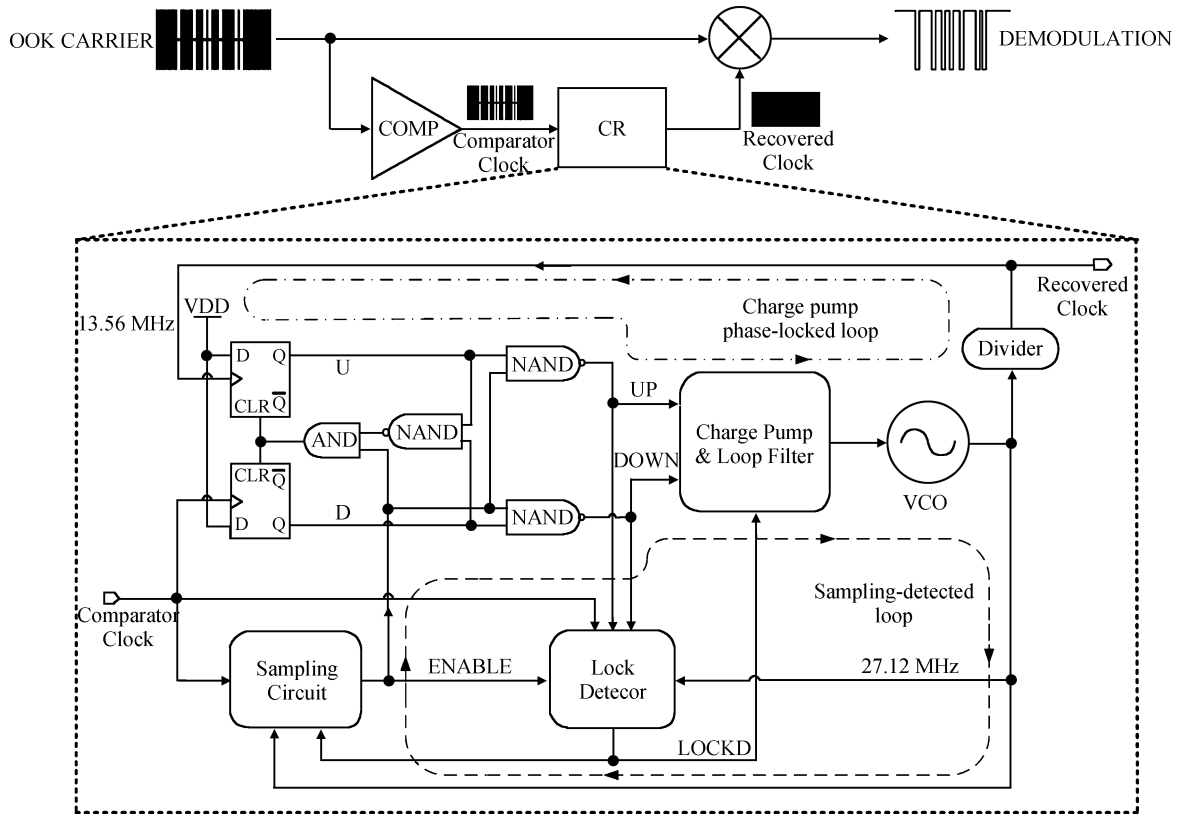


Fig. 1. Architecture of carrier-clock recovery circuit.

sampling result will lock the PFD by resetting the ENABLE to "0". Then the PLL enters the maintaining state. However, if the recovered clock is not identical to the comparator clock, the PLL will remain in tracking state until the two clocks are identical whether "pause" occurs or not. (3) After "pause" disappears, the lock detector redetects the consistency between the recovered clock and the comparator clock. If the UP differs from the DOWN, the lock detector will reset the lock instruction and the PLL will freely track the comparator clock until the two clocks are identical again. Otherwise, the loop waits for the next "pause" and the loop action does again.

### 2.2. Design consideration

As shown above, the PLL loop is necessary in the CR circuit, which can efficiently ensure stability and accurate lock with a low cost in this payment application. However, some properties of the input data need to be analyzed before the design of the clock recovery circuits. On the one hand, the "pause" embedded in the RF carrier makes the PLL lose reference frequency intermittently. If the PFD continuously detects the phase and frequency during the "pause", the VCO frequency will drift. Therefore, how to locate the "pause" is critical to prevent the PFD action during "pause". On the other hand, ripple often takes place at the beginning of "pause" due to the power oscillation on the antenna with different impedance at the proximity coupling device (PCD). The ripple makes the comparator clock vary sharply, which induces a high reference clock deviation for the PLL. A high sensitivity "pause" instruction circuit with high immunity to variation of the reference clock is necessary to eliminate the effect of the ripple.

Furthermore, in most PLL designs, the consideration of circuit parameters and architecture is important to the output frequency precision. Firstly, minimizing the charge pump current is helpful to increase the precision of the recovered clock because weak current leakage in the charge pump switches may happen, which affects the control voltage of the VCO. Secondly, a narrow loop bandwidth and a low voltage-control gain ($K_{VCO}$) can maximally maintain the VCO clock during "pause". Thirdly, jitter produced by the oscillator can be suppressed by the use of large voltage swings and careful design with phase noise concerned. In this work, the oscillator is designed for differential configuration so as to minimize the effect of supply and common-mode noise. Finally, a divider isolates the oscillator from the interference coupled through the PFD.

## 3. Circuit implementation

### 3.1. PFD and sampling circuit

A three-state PFD is widely used because it not only has a linear range of $\pm 2\pi$ radians but also acts as both phase detector and frequency detector. As shown in Fig. 1, a modified double D flip-flop PFD is implemented in this design. To prevent the PFD from operation during "pause", an ENABLE signal is added for the PFD locker.

In this paper, multiple-sample technology is used to confirm the "pause". Figure 2 shows the multiple-sample circuit, in which the comparator clock (REF) is sampled by the VCO clock (CLK). If the comparator clock deviates from the recovered clock (CLK/2) when "pause" occurs, the sampling circuit

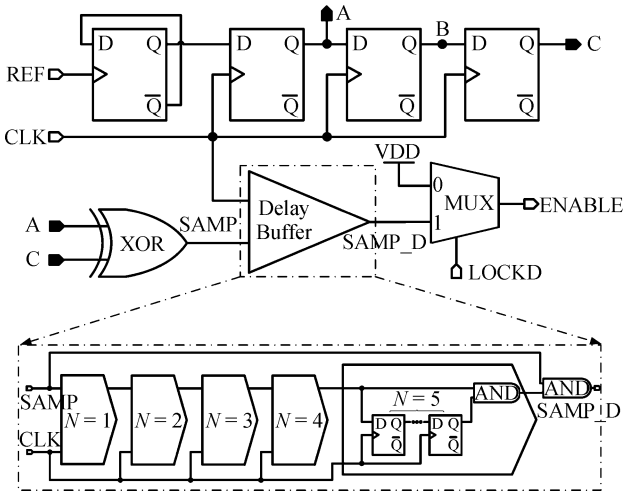


Fig. 2. Detailed block of two times frequency sampling circuit.

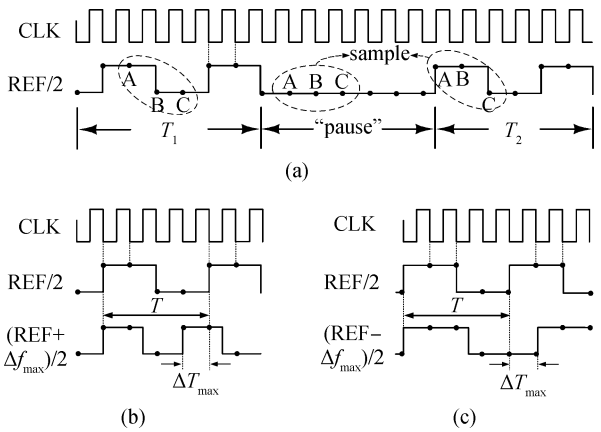


Fig. 3. (a) Sample waveform. (b) Maximal varying frequency. (c) Minimal varying frequency.

will send a valid ENABLE signal to lock the PFD. The principle of the sampling circuit can be expressed as SAMP = A ⊕ C. As shown in Fig. 3(a), if the XOR result between A point and C point is "1", the sampling circuit will not regard the appearance of "pause". Otherwise, the sampling circuit deems the "pause" occurs, the PFD will be locked.

The sampling accuracy can be obtained according to Figs. 2(b) and 2(c). The maximal quantity of period-varying ($\Delta T_{\max}$) is a quarter of a period. Therefore, the sampling accuracy can be expressed as Eq. (1) under 2× carrier clock sampling. Extending to $N$ multiple sampling rates, the sampling accuracy is expressed as Eq. (2).

$$S^2_{\text{accuracy}} = 1 - \frac{\Delta T_{\max}}{T} = 75\%, \tag{1}$$

$$S^N_{\text{accuracy}} = 1 - \frac{1}{2N}. \tag{2}$$

According to Eq. (2), the higher the sampling frequency, the better the sampling accuracy can be achieved. Therefore, two methods can be employed to improve the sampling accuracy: (1) increasing the sampling frequency to 4×, 8× or even more; and (2) reducing the REF to REF/4, REF/8 or even lower. The former method increases the VCO power dissipation, while the latter increases the response time of the sampling circuit, which reduces the system sensitivity. A tradeoff between power dissipation and system sensitivity has to be taken into account. Actually, because REF changes sharply when "pause" appears so that it is far faster than the variation of the VCO clock, the sampling accuracy under a 2× carrier clock is enough in this design.

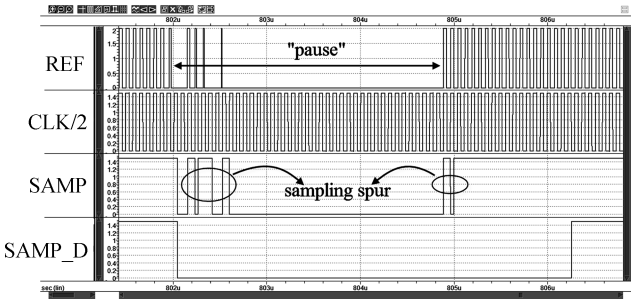


Fig. 4. Simulation result of spur elimination during a 3 $\mu$s "pause".

Except for the sampling logic, a delay buffer is added to remove the sampling spur induced by the ripple and interference during "pause". Otherwise, the spur will lead to an unintended action of the PFD, which makes the recovered clock drift slowly. As shown in Fig. 2, a five-stage delay is enough to eliminate the sampling spurs in the actual application. A simulation result of spur elimination during a single "pause" is shown in Fig. 4.

### 3.2. Lock detector

Figure 5 shows the lock detector circuit, which detects the state of the PLL by comparing the voltage on $C_2$ ($V_P$) with a standard bias voltage on $C_3$ ($V_N$). The $V_P$ can vary with the charge of PM1 or discharge of NM1, so a different lock instruction can be derived from the comparison result. The action of the detector can be expressed as follows. (1) When the chip is power down, LOCKD is reset to "0" and ENABLE is set to "1". Once the chip is powered on, LOCKD will be updated continuously according to the comparison result. The PLL will keep tracking the comparator clock freely until LOCKD overturns. (2) When LOCKD overturns, ENABLE is linked to the sampling result. If "pause" occurs, the PLL will enter the maintaining state. However, if a large frequency deviation occurs, the lock detector will overturn again and force the PLL to enter the tracking state whether or not the "pause" exits.

### 3.3. Charge pump and loop filter

Charge pump converts the digital signal to an analog voltage to control the frequency of the VCO. It is also the main block causing reference spurs due to the current leakage, current mismatch and timing mismatch. In this design, current leakage is critical for the recovered clock precision, so a 1 $\mu$A charge pump current is employed for lower current leakage. However, the low current increases the response time of the PLL. Additional charge pump current (3 $\mu$A) needs to be added for the quick locking at the stage of power on and tracking state. As shown in Fig. 6, the additional switches T3 and T4 are controlled by LOCKD, which is only valid in the PLL

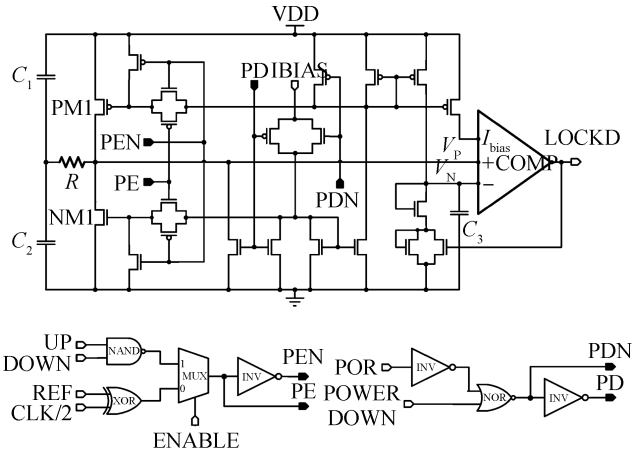


Fig. 5. Schematic of lock detector.

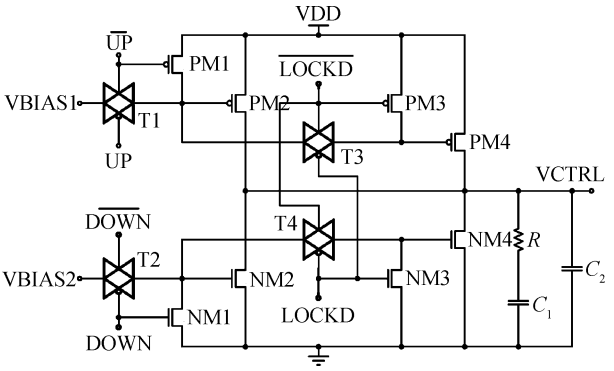


Fig. 6. Circuit of charge pump and loop filter.

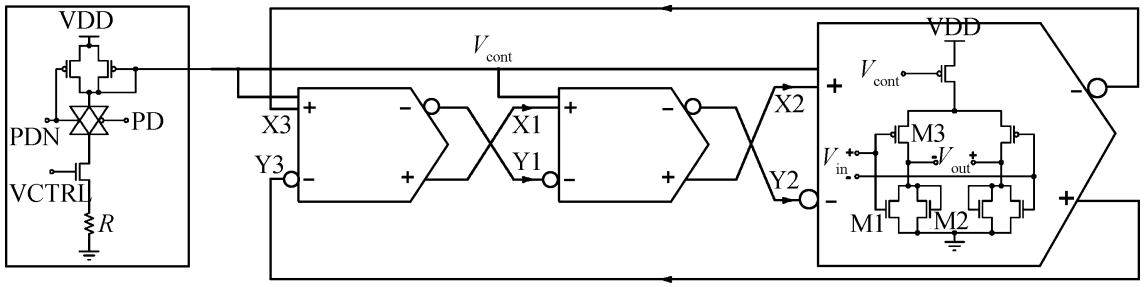


Fig. 7. Three-stage ring-oscillator: including input stage and three DCSL units.

tracking state. A two-order loop filter is adopted for high Q of bandwidth. A large $C_1$ prevents the voltage from deviating too much from the original value and a high proportion of $C_1/C_2$ ($> 100$) is necessary to keep the control voltage of VCO stable during the PLL maintaining state.

### 3.4. Voltage controlled oscillator

A ring-oscillator is adopted in this design because of low area consumption at MHz frequency application. Figure 7 shows the ring-oscillator based on a three-stage differential current steering logic (DCSL) unit. The frequency of a ring oscillator incorporating this stage can be varied by more than four orders of magnitude with less than a twofold variation in the amplitude[6]. The output voltage swing can be deduced from a single current steering logic (SCSL). The swing of output voltage is expressed as

$$\begin{aligned} V_{\text{swing}} &= V_{\text{OH}} - V_{\text{OL}} \\ &= \sqrt{\frac{2I_{\text{bias}}}{\mu_{\text{n}} C_{\text{ox}} (W/L)_2}} \sqrt{\frac{(W/L)_1 - (W/L)_2}{(W/L)_1}} + V_{\text{th}}, \end{aligned} \tag{3}$$

where $V_{\text{th}}$ is the threshold voltage of the NMOS transistor. In the same way, the rise time $t_{\text{LH}}$ and fall time $t_{\text{HL}}$ can be derived according to the time of charging and discharging to capacitance of the next stage. The average delay time can be expressed as

$$\begin{aligned} t_{\text{p}} &= \frac{t_{\text{LH}} + t_{\text{HL}}}{2} \\ &\approx C_{\text{out}} \left[ \frac{V_{\text{th}}}{2I_{\text{bias}}} + \sqrt{\frac{1}{2\mu_{\text{n}} C_{\text{ox}} I_{\text{bias}} (W/L)_1}} \right. \\ &\quad \left. \times \left( 1 + \frac{1}{2} \sqrt{\frac{(W/L)_2}{(W/L)_1}} \right) \right], \end{aligned} \tag{4}$$

where $C_{\text{out}}$ is the total output capacitance of the MOS transistor at the next stage.

According to Eq. (3), the swing of the output voltage is proportional to the square root of the bias current. Meanwhile, Equation (4) shows that the average delay time is nearly inversely proportional to the bias current, which means that the oscillatory frequency is almost proportional to the bias current.

## 4. Experimental results

A prototype chip with a transceiver, baseband and other correlative circuit has been fabricated by the SMIC 0.18-$\mu$m EEPROM (2P4M) CMOS process and occupies an area of $2 \times 2$ mm$^2$, in which the CR occupies an active area of $0.5 \times 0.5$ mm$^2$. A chip micrograph is shown in Fig. 8. According to the size of a standard SIM card, a printed circuit board (PCB) with a chip on board (COB) package is manufactured for the system verification in mobile phones. Two non-overlap antennas are respectively printed on the face and on the back of the SIM

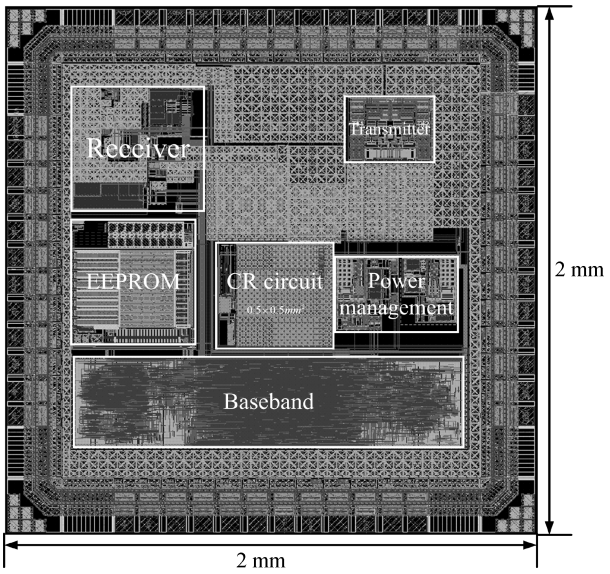


Fig. 8. Chip layout of CR circuit.

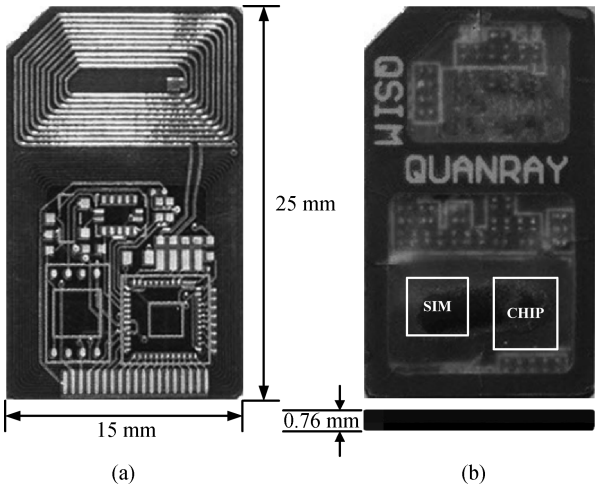


Fig. 9. PCB for testing and actual application. (a) The bottom PCB with antenna. (b) The product with a COB packing for testing.

card, which are shown in Fig. 9(a). A PCD compatible with the ISO/IEC 14443 protocol produces an energizing RF field, which couples to the designed chip through a $7 \times 13$ mm$^2$ receiver antenna. The tested signals are transferred to test devices by thin shielding wires for removal of the interference.

Figure 10 shows the test result of the CR circuit during one "pause" in write-command. The width of "pause" in the test is 3 $\mu$s. The test result shows that the recovered clock ($D_5$) during the "pause" doesn't vary with the variation of the comparator clock ($D_4$). Meanwhile, the ENABLE ($D_1$) signal gives the correct instruction to the PFD when "pause" appears. The same instruction occurs when "pause" disappears. The spur occurring on the REF doesn't affect the ENABLE signal, which proves the function of the delay cell. The frequency tested at the end of "pause" is 13.514 MHz, which shows a 0.34% deviation compared with the desired 13.56 MHz. High system sensitivity in the payment application is measured through as low as 8 mV input amplitude. The detailed current consumptions of the proposed clock recovery circuits in the tracking

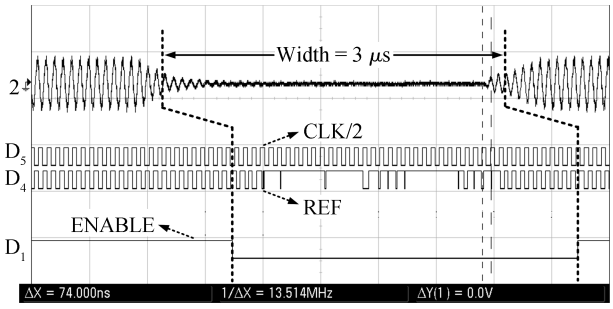


Fig. 10. Measured clock recovery result. $D_1$: the ENABLE signal; $D_4$: the comparator clock; $D_5$: the recovered clock, which is in the inverse state of the inner chip because of the testing buffer. Source 2: the OOK carrier produced by the PCD compatible with the 14443 protocol.

Table 1. Current consumption in different states.

| Blocks | CR current consumption ($\mu$A) | |
|---|---|---|
| | Tracking state | Maintaining state |
| Sampling circuit | 50 | 0 |
| Lock detector | 5 | 5 |
| PFD & CP & LF | 9 | $\approx 0$ |
| VCO | 16 | 16 |
| Total | 80 | 21 |

Table 2. Measured performance of CR circuit.

| Parameter | Ref. [5] | This work |
|---|---|---|
| Process | 0.35-$\mu$m 2P4M CMOS | 0.18-$\mu$m 2P4M CMOS |
| Supply voltage (V) | 3.3 | 1.5 |
| Frequency deviation (%) | 7.5 | 0.34 |
| System sensitivity (V) | > 1.5 | 0.008 |
| PLL set up time ($\mu$s) | 200 | 90 |
| Power dissipation ($\mu$A) | 17 @ 6.78 MHz | 80 @ 27.12 MHz |

state and maintaining state are listed in Table 1. When operating in the frequency tracking state, every functional block of the proposed clock recovery circuits consume power; while in the maintaining state, only the lock detector and VCO consume power. Finally, Table 2 summarizes the measured performance of the CR.

## 5. Conclusion

A high-sensitivity high-precision consecutive clock recovery circuit based on a sampling-detection module and a CP-PLL for 13.56 MHz mobile payment application is presented. The novel and smart sampling architecture solves the long absent reference frequency during the wireless communication. A hybrid analog/digital sample-and-hold circuit not only exhibits high sensitivity and an accurate "pause" instruction but also eliminate ripple and interference during "pause". The use of a dual control charge pump shortens the setup time of the PLL under a narrow loop bandwidth. 0.34% frequency deviation and 8 mV sensitivity are confirmed by the experimental result. Measured power consumption is 80 $\mu$A with a 1.5 V power supply.

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