A fractional-N frequency synthesizer-based multi-standard I/Q carrier generation system in 0.13 μm CMOS*

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Abstract: This paper proposes a sigma–delta fractional-N frequency synthesizer-based multi-standard I/Q carrier generation system. With reasonable frequency planning, the system can be used in multi-standard wireless communication applications (GSM, WCDMA, GPRS, TD-SCDMA, WLAN (802.11a/b/g)). The implementation is achieved by a 0.13 μm RF CMOS process. The measured results demonstrate that three quadrature VCOs (QVCO) continuously cover the frequency from 3.1 to 6.1 GHz (65.2%), and through the successive divide-by-2 prescalers to achieve the frequency from 0.75 to 6.1 GHz continuously. The chip was fully integrated with the exception of an off-chip filter. The entire chip area is only 3.78 mm^2, and the system consumes a 21.7 mA @ 1.2 V supply without output buffers. The lock-in time of the PLL frequency synthesizer is less than 4 μs over the entire frequency range with a direct frequency presetting technique and the auxiliary non-volatile memory (NVM) can store the digital configuration signal of the system, including presetting signals to avoid the calibration process case by case.

Key words: fractional-N synthesizer; $\Delta\Sigma$ modulator; multi-standard; quadrature VCO; divide-by-2; NVM
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1. Introduction

To reduce the overall terminal mobile phone cost, silicon integration of multimode transceivers is considered. Nevertheless, this is really cost effective only when transceiver blocks are shared between the different Rx and Tx chains. In recent years, there has been significant progress in wireless communications in terms of integration of various communication standards into a single mobile chip. This is a suitable design consideration for a single reconfigurable radio transceiver that is able to achieve all requirements of different communication standards. There are some crucial problems of power consumption, chip area, design flexibility and interoperability among different communication standards in such single systems. So we should make efforts to tradeoff those problems. One of the challenging blocks in such transceivers is the multi-standard carrier generation system. The frequency synthesizer should enable proper interoperability and seamless connectivity among the various standards considered. In particular, they can generate the in-phase and quadrature (I/Q) waves as LO signals for zero-IF or low-IF receivers. A single chip system fully compliant with the IEEE 802.11a/b/g standards was recently presented[1]. This generates two discrete frequency bands with mixers to satisfy the IEEE 802.11a/b/g standards. However, it has some spurious tones generated by mixers and needs an additional high frequency filter. Another multimode frequency synthesizer was developed[2]. This used two PLL loops to generate the LO signals, but the frequency band is not continuous and the signal is differential not the I/Q output. Also, the carrier generation systems mentioned above can't comply with all standards below the 6 GHz frequency band.

This paper presents a fractional-N frequency synthesizer with three quadrature VCOs, and it generates I/Q LO signals with a continuous range from 0.75 to 6.1 GHz. The rest of the paper is organized in four parts. First we introduce the architecture of the multi-standard I/Q carrier generation system, frequency planning and some novel design techniques. Then we present the detail of the circuit design and implementation. Further, we show the experimental results of this carrier generation system. Finally, we present our conclusion.

2. Multi-standard I/Q carrier generation system

2.1. Frequency synthesizer architecture

It is often difficult to generate a multi-standard carrier using one integer-N frequency synthesizer whose step size is limited by the reference frequency. So the fractional-N synthesizer is the more preferable option. Figure 1 shows the architecture of the proposed I/Q carrier generation system. This is the typical fractional-N architecture, including a phase frequency detector (PFD) that is a three-state phase/frequency detection scheme. The charge pump (CP) with the switch in the source is adopted. The presetting module can reduce the lock-in time greatly[3]. A programmable multi-module divider can generate the division ration from 32 to 127. Three Mux_Bufs selects the desired QVCO output. Successive divide-by-2 prescalers generate the I/Q signals. A powerful digital processor with a 15 bit $\Sigma\Delta$ modulator makes the frequency resolution less than 1.6

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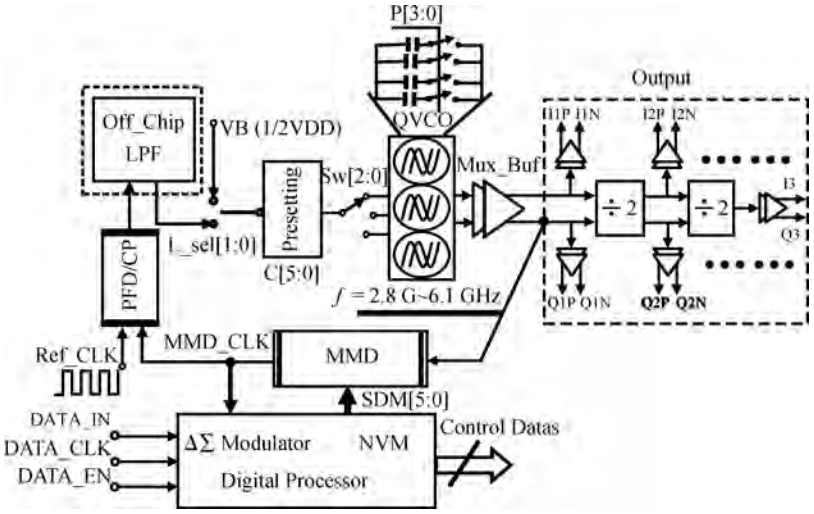

Fig. 1. Architecture of I/Q carrier generation system.

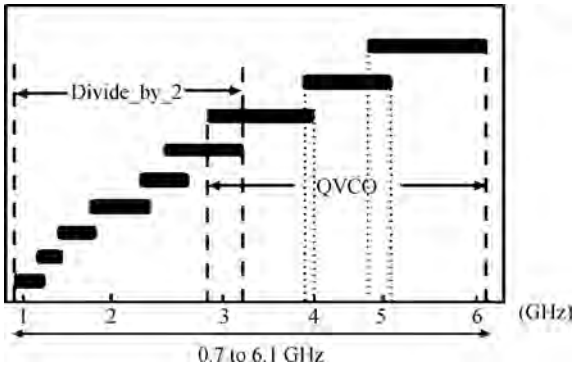

Fig. 2. Frequency plan of the system.

kHz. And a non-volatile memory (NVM)[4] is integrated into our design. All components, except for the loop filter (LPF), are integrated on a single chip. To cover the frequency band from 0.75 to 6.1 GHz continuously, three quadrature LC-tank VCOs are used. Their frequency is dependent on the output of the presetting module and digital signal P[3:0]. Two VCOs only can cover the important bands from 0.8 to 6.0 GHz not the whole band continuously[5]. It is a good idea to create a sum or difference frequency in a single-sideband (SSB) mixer by combing the QVCO output frequency with itself after division. However, imperfect gain or inaccuracy mismatch in the SSB mixer will degrade the I/Q signal. So, in Fig. 1, we use Sw to make one of the QVCOs to operate normally (the other two QVCOs are in sleep mode). Mux_buf selects the operating QVCO to output the frequency signals. Then the output signal is output directly or is divided by 2^i ($i = 1$ or 2) dividers. Thus the synthesizer can cover a 0.75–6.1 GHz continuously tunable frequency range and generate I and Q signals. Figure 2 shows the frequency range that covers the whole frequency band continuously.

2.2. Direct frequency presetting method

The mechanism by which the frequency presetting method reduces the lock-in time of the synthesizer significantly is as follows. First the lock-in time of the frequency synthesizer is defined as

$$T_{\mathrm{L}} = -\frac{\ln(\varepsilon\sqrt{1-\xi^2})}{\xi\varpi_{\mathrm{n}}}, \tag{1}$$

where the specified frequency accuracy is

$$\varepsilon = \frac{f_{\mathrm{error}}}{|f_2 - f_1|}, \tag{2}$$

where f_{error} is the acceptable frequency error, and f_1 and f_2 are the initial frequency and target frequency, respectively. ξ is the damping factor and ϖ_{n} is the natural frequency of the PLL loop. Because the lock-in time depends on the magnitude of the initial frequency error, the lock-in time can be shortened as long as the initial frequency error can be reduced. In our design, in order to reduce the locked time, the PLL can work in two modes: calibration mode and operation mode. When the synthesizer starts up or receives a reset signal, it first works in the calibration mode. The digital processor measures the output frequency of the QVCO and calibrates the relation between the output frequency and the presetting digital signals, C and P, automatically. The whole calibration process can be carried out by the frequency sampler and the linear interpolation module of the digital processor[6]. After the calibration process is finished, the synthesizer switches to operation mode. The digital processor outputs the presetting signals C and P to directly preset the frequency of the QVCO. After the output frequency of the QVCO is preset with a very small initial frequency error, the output voltage V_{a} of the LPF precisely tunes the frequency of the QVCO. Therefore the synthesizer can settle down in a very short time. Its lock-in time does almost not depend on the frequency step, process variation, device parasitic effect and chip temperature.

2.3. Auxiliary non-volatile-memory

A non-volatile memory (NVM) inside the PLL frequency synthesizer is used to store the presetting signals and other effective configuration information in order to avoid the calibration process case by case. After the digital processor calculation，we can store the digital signal P[3:0], C[5:0] and switch signal of the QVCO Sw[2:0] to NVM. In most situations, we

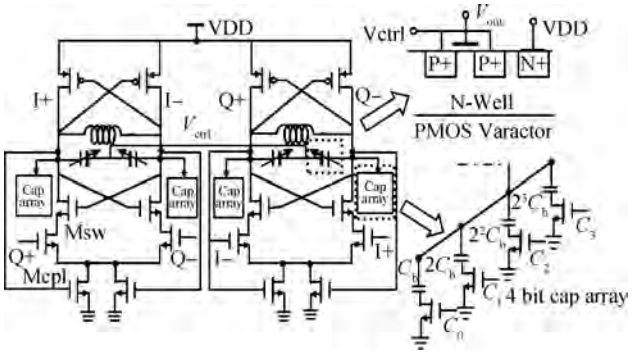

Fig. 3. Proposed QVCO with switchable tail current.

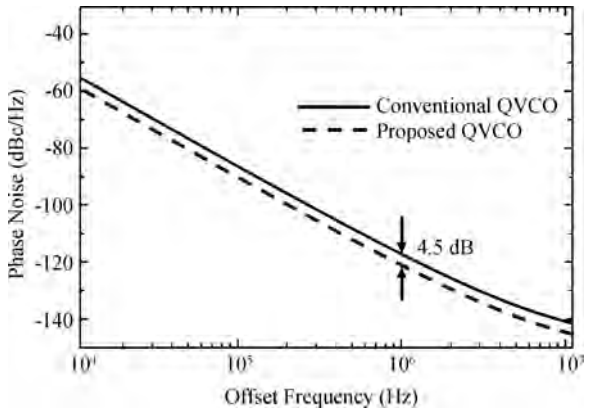

Fig. 4. SpectreRF phase noise simulation for QVCOs.

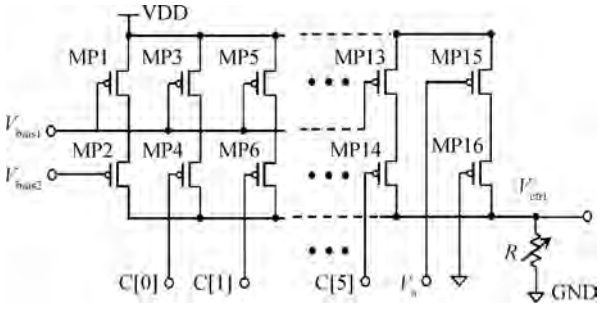

Fig. 5. Presetting module circuit.

need to store several different presetting signals C and P in the NVM, which are related to several different frequencies, so the process described above may be carried out several times. After several groups of presetting signals C and P are stored in the NVM, calibration mode is finished. Then the PLL can work in operation work. The digital processor can control the NVM to read out the P/C and Sw digital signals to control the presetting module and QVCO according to the divide ratio information. On the other hand, the typical EEPROM or FLASH memory requires additional masks so that even a small size of embedded memory brings additional cost for the whole system. Furthermore, these kinds of memory usually consume a lot of power. Recently, an ultra low power NVM with a high efficiency charge pump circuit was designed by our lab[4]. The memory can be integrated into a standard CMOS process and it is based on the FN tunneling phenomenon with an extremely small current density. Therefore it will not add additional power consumption to our design.

3. Circuit design and implementation

3.1. Switchable tail current source QVCO

Figure 3 shows the proposed QVCO with a switchable tail current source. The standard complementary CMOS cross-pair topology has been used because the structure combining PMOS and NMOS cross-pairs achieves a lower phase noise than a single NMOS topology for the same power due to symmetry properties of the resulting periodic waveform. The complementary structure offers higher transconductance for a given current, which results in a faster switching cross-coupled differential pair. It also offers better rise and fall time symmetry, which results in a smaller $1/f$ noise corner. The tank consists of a full symmetric spiral inductor and two MOS varactors. For a wide tuning range and a small VCO gain, a 4-bit binary switchable capacitor array (SCA) is connected to the LC tank for coarse tuning. The tail current is the dominant source of the flicker noise, but, without the tail current source, the amplitude will be more variable than with the current tail source[7]. Sometimes, in the worst case, the oscillator with a small amplitude will not enable driving of the CMOS divider in the synthesizer. So the tail current source is used in our design, but not the fixed bias voltage. We use the switched biasing scheme in the design. This can reduce the impact of $1/f$ noise from the tail current source[8]. According to the SpectreRF simulation result shown in Fig. 4, the phase noise is improved by 4.5 dB at 1 MHz compared to the conventional QVCO with the same current consumption.

3.2. Presetting module circuit

Figure 5 shows the presetting module circuit[3]. This is a mixed-signal circuit that consists of six parallel current sources and a resistor with a 3-bit digital signal to make the presetting frequency more accurate. A 6-bit digital signal C[5:0] control the current source on and off with the switch MOS in the circuit. MP3, MP5–MP11 and MP13 transistors constitute a series of current sources with different ratios of currents: 2^n ($n = 0$, 1, 2, 3, 4, 5), respectively. When signal C[5:0] is input into the frequency-presetting module, it will produce the voltage signal $V_{\rm ctrl}$ to control the frequency of the QVCO with a small initial frequency error. That is the presetting to get the frequency near the target frequency. Then the output voltage $V_{\rm a}$ of the LPF accurately tunes the frequency of the QVCO by adjusting the current through the MP15 transistor. When frequency-hopping occurs, the presetting signals C[5:0] and the output voltage $V_{\rm a}$ of the LPF will adjust the frequency of the QVCO within in a very short time.

3.3. Lower power non-volatile-memory implementation

The NVM proposed in this paper is based on the FN tunneling phenomenon with an extremely small current density. It is fully compatible with the standard CMOS process. It is used to store the frequency presetting signals C[5:0], P[3:0] and some useful digital configuration signals after calibration, which can avoid the system calibration case by case to save

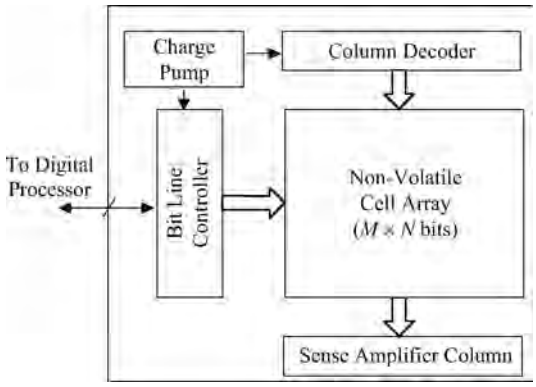

Fig. 6. Architecture of the NVM.

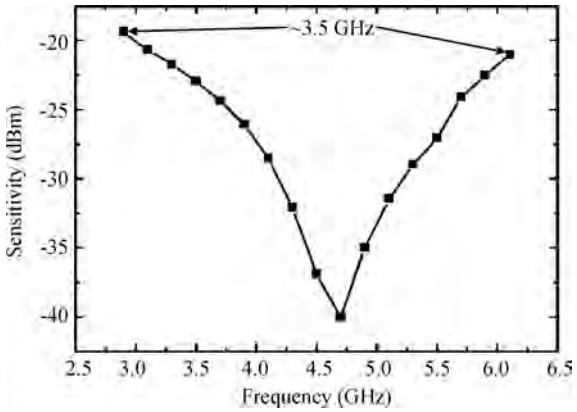

Fig. 8. Sensitivity of the divide-by-2.

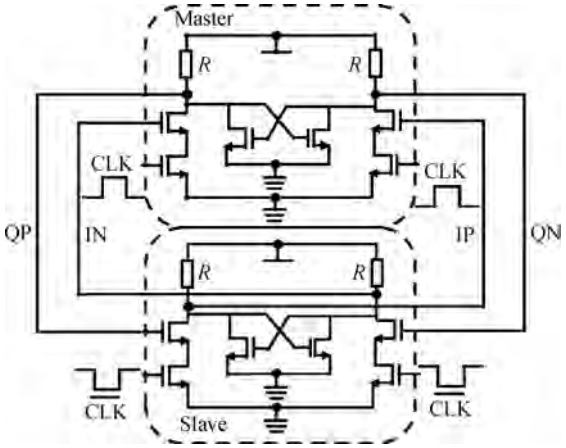

Fig. 7. Divide-by-2 prescaler with CML latch.

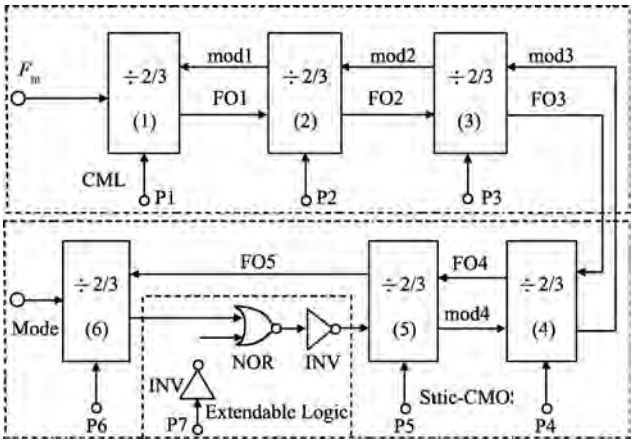

Fig. 9. Division ratio extensible MMD.

power consumption and enhance the versatility. The architecture of the NVM is shown in Fig. 6. It consists of a NV cell array, a bit line controller, a column decoder, a sense amplifier column and a charge pump. The bit line controller controls the writing operation of the NV memory. The column decoder selects the active column. The sense amplifiers detect the outputs of the active-column cells in the reading operation. The charge pump generates a high voltage and a medium voltage in the writing operation. The implementation method of the circuits is discussed in Ref. [4].

3.4. Divide-by-2 prescaler and programmable multi-module-divider

Figure 7 shows a current-mode logic (CML) static frequency divider that is widely used in high-speed PLLs due to simple design and robust operation. The divider without a current source was used. This can increase the maximum frequency, reduce the power consumption and increase the voltage headroom[9]. The CML divide-by-2 is more ideal than the TSPC or ILFD divider below 6 GHz frequency operation. The successive divide-by-2 prescalers achieve the frequency from 0.75 to 6.1 GHz continuously and generate the I/Q signals. Figure 8 shows the sensitivity simulation of the divide-by-2. It has an approximately 3.5 GHz frequency tuning span when the input signal power is less than –20 dBm.

The swallow-pulse programmable divider is usually used as divider in the PLL frequency synthesizer. However, it is not suitable for the wideband PLL frequency synthesizer with a higher maximum frequency because the circuit parameters are optimized with difficulty. However, the multi-module divider (MMD) is widely used in the fractional-N synthesizer, especially with the MASH1-1-1 modulator, because it supports seamless dithering on a wide-range divide modulus. Figure 9 shows the circuit of the division ratio extensible MMD, which consists of a chain of 2/3 dividers and an extendable logic. It exploits a hybrid CMOS/CML style to trade off between speed and consumption. Since N cells provide division ratio from 2^N to $2^{N+1} - 1$, we use 6 bit control words that cover the 64–127 range. Moreover, additional bit P7 and extendable logic are inserted in the circuit that can bypass cell 6. Thus this technique makes the division ratio extend to the 31–127 range. The high frequency cells adopt differential CML and the low frequency cells adopt static CMOS logic that can optimize the consumption for this divider. This draws about 2.5 mA from a 1.2 V supply.

4. Experimental results

The proposed fractional-N frequency synthesizer multi-standard I/Q carrier generation system was implemented in a 1P8M, 0.13 μm, RFCMOS process. A microphotograph of the chip is shown in Fig. 10. The die area of the prototype mea-

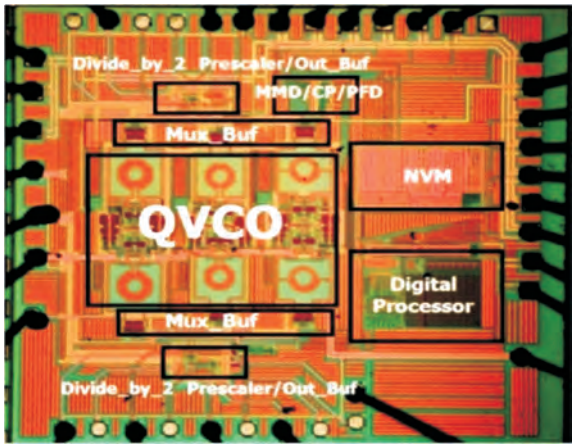

Fig. 10. Microphotograph of the system.

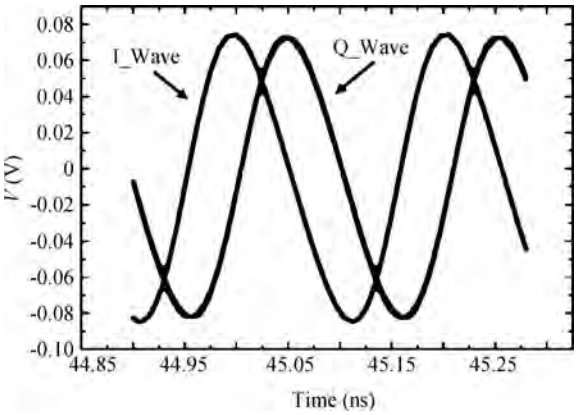

Fig. 11. Output I/Q signal @ 4.86 GHz.

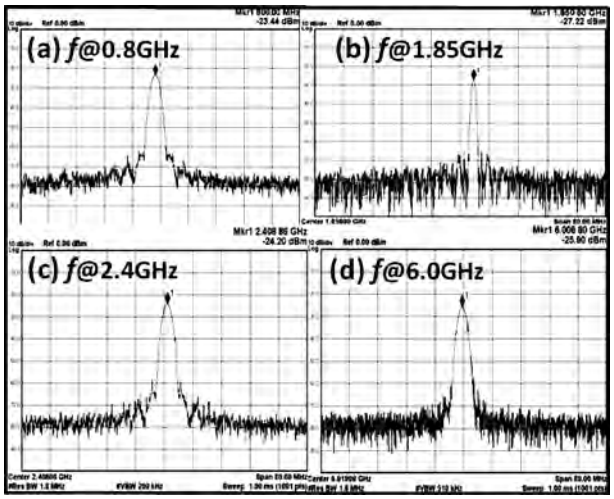

Fig. 12. Typical frequency power spectra at (a) 0.8 GHz, (b) 1.85 GHz, (c) 2.408 GHz, and (d) 6.008 GHz.

sures 3.78 mm^2 (including pads). All control signals are supplied through the digital processor, and the reference frequency is 50 MHz.

Figure 11 shows the in-phase and quadrature signals, which are post simulated with a 50 Ω load at the SS corner. It can be deduced that the amplitude and phase mismatch between the two signals is 1.2% and 3°, respectively. It is crucial to plan the symmetrical I/Q signal path in the layout design, especially for high frequency signals because very small asymmetry will affect the phase and amplitude of the I/Q signal. The typical frequency point power spectra measured at the output are shown in Fig. 12.

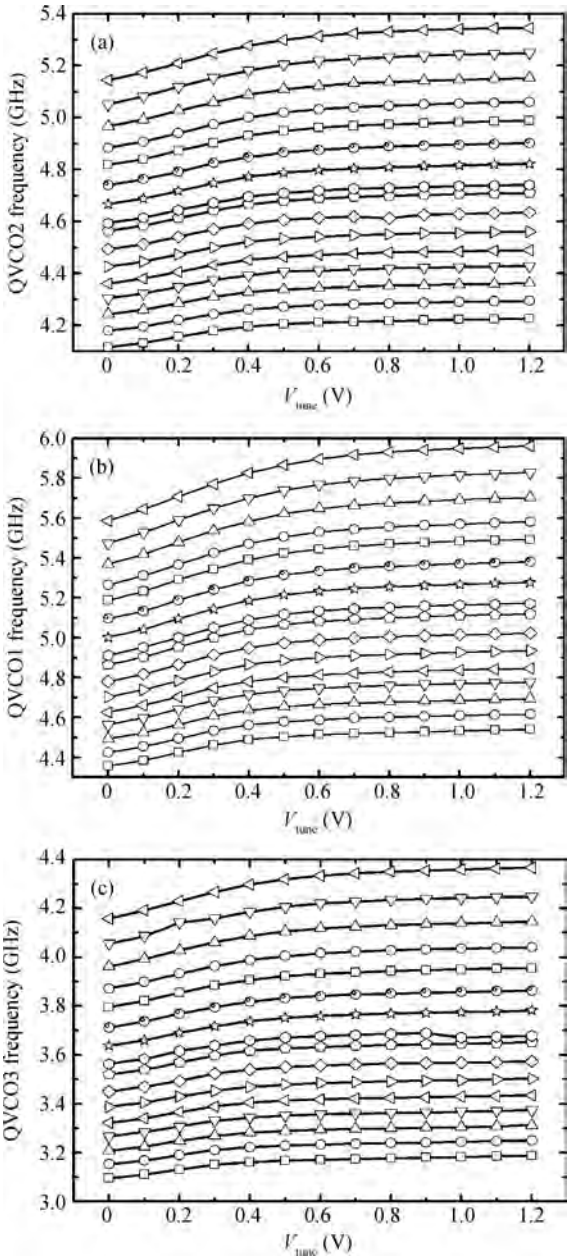

Fig. 13. Measured tuning range of the QVCOs. (a) QVCO1. (b) QVCO2. (c) QVCO3.

Figure 13 shows the measured QVCO output frequency versus the continuous tuning voltage and digital words controlling the SCA. The minimum frequency is 3.1 GHz (QVCO3 @ 1111 SCA digital input) and the maximum frequency is 6.1 GHz (QVCO1 @ 0000 SCA digital input). The tuning range is about 3 GHz (65.2%). Three QVCOs with 4-bit digital control (QVCO1, QVCO2 and QVCO3) cover three frequency ranges: 3.1–4.37 GHz (about 30% of the center frequency), 4.12–5.35 GHz (about 25.9%) and 4.45–6.1 GHz (about 30%), respec-

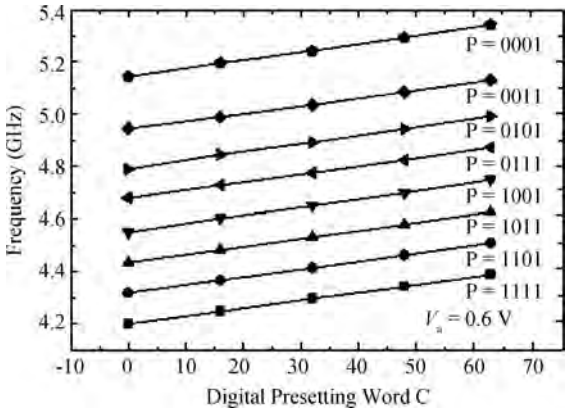

Fig. 14. Frequency versus presetting signal C [5:0] with different values of P.

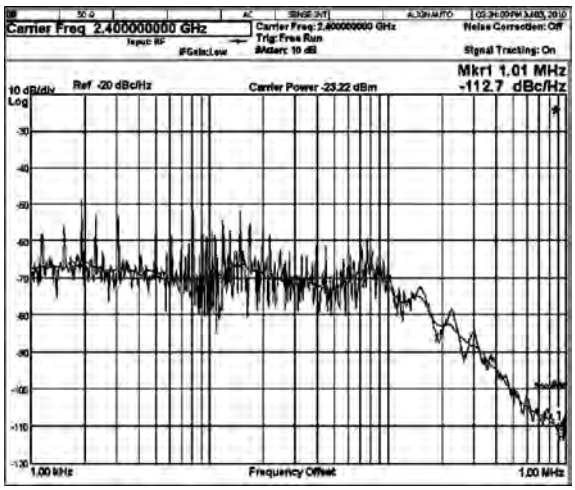

Fig. 15. Phase noise of the proposed carrier generation system at 2.4 GHz.

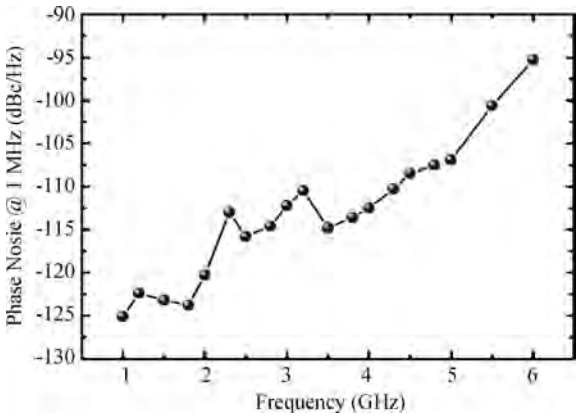

Fig. 16. Phase noise from 1 to 6 GHz.

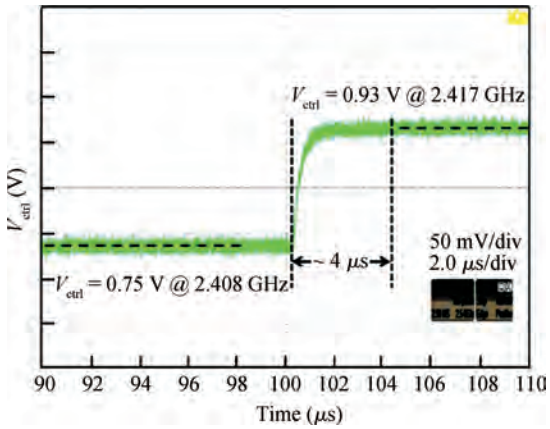

Fig. 17. Typical setting time of the synthesizer.

tively. All of the gains K_{vco} are about 100 MHz/V in the three QVCOs. Every QVCO has 16 curves, and overlapping regions between adjacent curves is kept large enough to prevent PVT variation. At the same time, we get the curves of the frequency band after divide-by-2 and divide-by-4. Thus, the frequency from 0.75 to 6.1 GHz can be tuned continuously. As expected, the spectra of the considered standard are continuous with sufficient margin to compensate temperature and process variations.

Figure 14 shows the dependence of the QVCO2 presetting frequency on the signals C and P at V_a = 0.6 V. As shown in Fig. 13, the measured result shows a good linear relation between the presetting frequency and the control signal P/C. The better the linear relation between the presetting frequency and the signal C, the smaller the initial frequency error will be. Then the lock-in time will be smaller.

Figure 15 shows the phase noise measured at the output of the I/Q carrier generation system @ 2.4 GHz under the PLL locked state, as the division ratio is set to 96 with a 50 MHz reference frequency. The measured phase noise at 1 MHz offset is –112.7 dBc/Hz and the in-band phase noise is about –70 dBc/Hz. The measured loop bandwidth is approximately 200 kHz. Operating at 4.8 GHz of the QVCO2 (through divide-by-2 prescaler get the 2.4 GHz frequency), the whole system draws 21.7 mA from a 1.2-V supply, and it can be extrapolated to –142 dBc/Hz at 10 MHz from a 800 MHz carrier.

Figure 16 shows the phase noise performance over 1–6 GHz of the carrier generation system. The worst case phase noise is about –95 dBc/Hz @ 1 MHz off the operation frequency 6 GHz, and the phase noise is about –125 dBc/Hz @ 1 MHz off the operation frequency 1 GHz.

Figure 17 shows the typical frequency hopping characteristics of the proposed synthesizer with a direct frequency presetting technique during the QVCO2 operation. The bandwidth of the PLL is 200 kHz, the reference frequency is 50 MHz and the off-chip loop filter is a third-order type with C_2 = 9 pF, R_z = 17 kΩ, C_z = 50 pF, R_3 = 20 kΩ and C_3 = 0.5 pF. The lock-in time is less than 4 μs from 2.408 to 2.417 GHz at 100 μs, which is much shorter than the synthesizer without a frequency-presetting function.

Based on the measured results above, a comparison of this synthesizer with the literature is summarized in Table 1.

5. Conclusion

We have proposed a multi-standard I/Q carrier generation system. This system was implemented with a 0.13 μm 1.2 V RF CMOS process. All components in the system are integrated on the chip except for the loop filter. The chip area is

Table 1. Frequency synthesizer performance comparison.

Parameter	Ref. [10] (simulation)	Ref. [11]	This work
Technology	0.13 μm CMOS	0.5 μm BiCMOS	0.13 μm CMOS
Architecture	Integer-N	Fractional-N	Fractional-N
Frequency range (GHz)	3–5.0 (not continuous)	2.4, 5.1–5.3	0.75–6.1 (continuous)
VCO frequency range	6.05–6.55 (8%)	2.4, 5.1–5.3	3.1–6.1 (65.2%)
Output wave type	I/Q	Differential	I/Q
Phase noise @ 1 MHz (dBc/Hz)	~ -110 (VCO)	~ 120 (PLL)	–95 to –125.1 (PLL)
Frequency resolution (kHz)	NA	< 500	< 2
Setting time (μs)	NA	NA	< 4
Chip area (mm^2)	6	3.22	3.78
Power consumption (mA@V)	75 @ 1.5	36 @ 2.5	21.7 @ 1.2

3.78 mm^2 (including pads). The measured results demonstrate that the frequency can be tuned from 0.75 to 6.1 GHz continuously. And the output waves are I/Q signals that are suitable for the zero-IF or low-IF receivers. In the whole frequency range, the phase noise under the PLL locked state is –95 to –125.1 dBc/Hz @ 1 MHz offset carrier frequency. It has a less than 4 μs setting time with the direct frequency presetting technique. The whole implemented system draws 21.7 mA from a 1.2 V supply.

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