A 50 MHz–1 GHz high linearity CATV amplifier with a 0.15 μm InGaAs PHEMT process

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Abstract: A 50 MHz–1 GHz low noise and high linearity amplifier monolithic-microwave integrated-circuit (MMIC) for cable TV is presented. A shunt AC voltage negative feedback combined with source current negative feedback is adopted to extend the bandwidth and linearity. A novel DC bias feedback is introduced to stabilize the operation point, which improved the linearity further. The circuit was fabricated with a 0.15 μm InGaAs PHEMT (pseudomorphic high electron mobility transistor) process. The test was carried out in 75 Ω systems from 50 MHz to 1 GHz. The measurement results showed that it gave a small signal gain of 16.5 dB with little gain ripples of less than ±1 dB. An excellent noise figure of 1.7–2.9 dB is obtained in the designed band. The IIP3 is 16 dBm, which shows very good linearity. The CSO and CTB are high up to 68 dBc and 77 dBc, respectively. The chip area is 0.56 mm^2 and the power dissipation is 110 mA with a 5 V supply. It is ideally suited to cable TV systems.

Key words: low noise; high linearity; MMIC; InGaAs PHEMT process; CATV amplifier

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1. Introduction

In recent years, tri-network integration has become a hot topic of research. Tri-network integration means the integration of telecommunication networks, cable TV networks and the Internet. So, the CATV meets the great opportunities of development with the two-directional transformation of CATV infrastructure. The CATV amplifier is a key element of such equipment and it plays a major role in amplifying damped TV signals (compensating for loss of signal power). The CATV amplifier needs low distortion, low noise and high linearity from a 50 MHz to 1 GHz frequency band in 75 Ω systems[1, 2].

At the same time, GaAs monolithic-microwave integrated-circuit (MMIC) technology has been expected with more reasons to extend its roles from the area of military applications to commercial communications recently[3–5]. Because many products need an operation range from sub-gigahertz to a few gigahertz, the uses of GaAs MMICs are continuously growing. They are especially suitable for high linearity and low noise applications[6–9].

In this article, we present a CATV amplifier that was fabricated with a 0.15 μm InGaAs PHEMT (pseudomorphic high electron mobility transistor) process from WIN semiconductor. The circuit used a shunt AC voltage negative feedback and a source current negative feedback to improve the bandwidth and linearity. The measurement results represent excellent noise performance and high linearity. The chip area is 0.56 mm^2 and the power dissipation is 110 mA with a 5 V supply.

2. Circuit design

2.1. InGaAs PHEMT process

The chip was fabricated with the 0.15 μm InGaAs PHEMT process from WIN semiconductor, which used an InGaAs layer as the channel material. The advanced 6-inch process and epitaxial design provides excellent low noise and power performance with good temperature stability and reliability. We used the depletion-mode PHEMT transistors in our design. Figure 1 gives the I–V curve of the transistor in our design.

2.2. Circuit design

A schematic diagram of the designed amplifier is shown in Fig. 2. The circuit is designed as a stack of two depletion-mode PHEMT transistors. The cascode structure consists of M1 and M2, which provide high reverse isolation. For our 0.15 μm GaAs PHEMT process, the trans-conductance of the transistor is

$$\mathrm{GM} = \mathrm{GMO}(\mathrm{NOF} \cdot \mathrm{Ugw})/(1.5 \times 10^{-4}). \tag{1}$$

Here, Ugw is the reference unit gate width, NOF is the number of fingers and GMO is the unit of the trans-conductance gain. The bigger the gate width, the larger the gain will be. However, it will increase the parasitic capacitance at the same time. As a

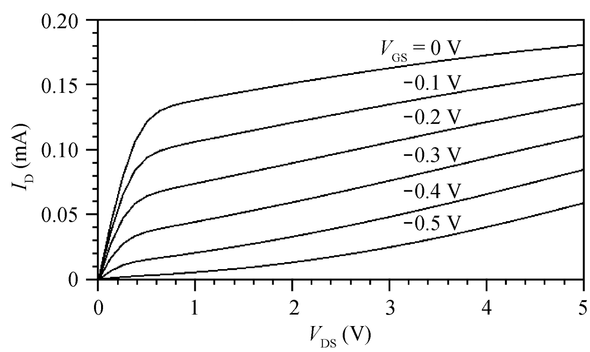

Fig. 1. I–V curve of the PHEMT transistor.

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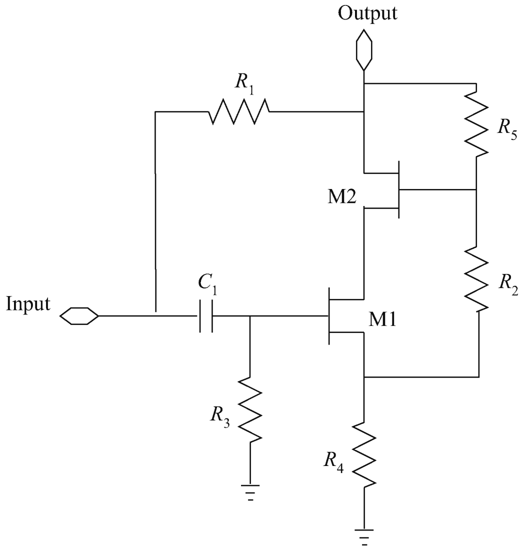


Fig. 2. Schematic diagram of the circuit.

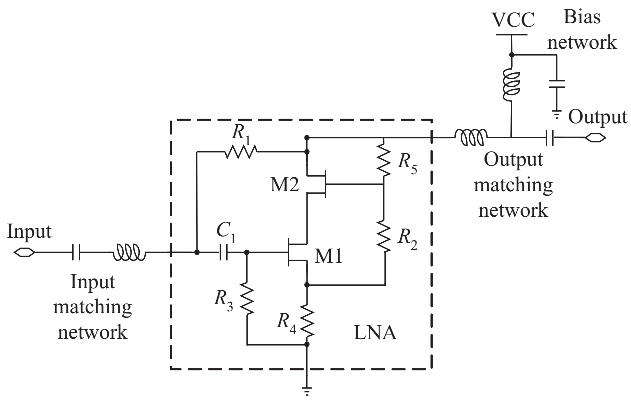


Fig. 3. External connection of test circuit.

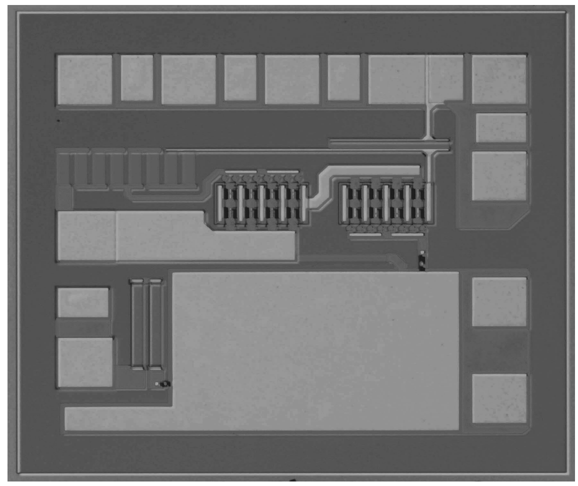


Fig. 4. Micrograph of the circuit.

trade-off among the gain, bandwidth and linearity factors, the gate sizes of the M1 and M2 are all chosen as 600 μm/0.15 μm, which are divided into 8 fingers.

The resistor R_3 connects the gate of M1 with the ground, which provides the zero-bias for M1. Another function of this resistor is for a better input impedance match. Here, two classical feedback techniques are used to provide the high bandwidth and linearity. The resistor R_1 and C_1 provide a shunt AC voltage negative feedback. The R_4 provides the source current negative feedback. The feedback techniques extend the bandwidth and linearity. The R_1 (R_4) is smaller (larger), the better the bandwidth and linearity. However, the gain of the amplifier would be sacrificed in this condition. As a trade-off, the R_1 and R_4 are chosen as 750 Ω and 3 Ω, respectively. In addition, for the conventional cascode structure, the bias voltage of the gate of cascade transistor is fixed. In our design, the R_5, R_2, and R_4 constitute the gate bias of the cascade transistor M2 as

$$V_{\mathrm{G2}} = V_{\mathrm{DD}} - (V_{\mathrm{DD}} - i_{\mathrm{D}} R_4) \frac{R_5}{R_2 + R_5} = \frac{R_2}{R_2 + R_5} V_{\mathrm{DD}} + \frac{R_4 R_5}{R_2 + R_5} i_{\mathrm{D}}. \quad (2)$$

Here, V_{DD} is the supply voltage, i_{D} is the drain current of M1. If the i_{D} increases, the drain voltage of M1 will rise. According to the above formula, the gate bias voltage of M2 and then the drain potential of M1 will also increase. This is actually DC negative feedback to stabilize the operating point of M1, which increases the linearity further.

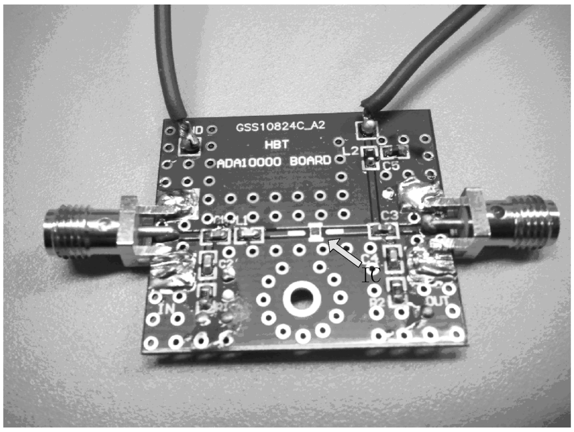
The external connection for the amplifier is shown in Fig. 3. A choking coil is inserted between the output port and the VDD. This provides the DC bias current and isolation of the AC signal at the same time. Also, the series LC networks constitute the input and output impedance match network, which is set at 75 Ω to ensure impedance-matched transmission of TV signals.

3. Measurements results

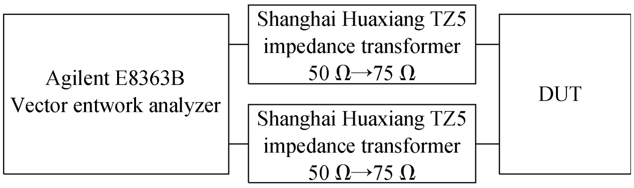
Figure 4 gives the micrograph of the designed CATV amplifier in our work. The chip area is 0.56 mm^2 and the power dissipation of the amplifier is 110 mA from a 5 V supply. The test bench is shown in Fig. 5. The measurements of the circuit were carried out using an Agilent E8363B vector network analyzer and a E4440A spectrum analyzer.

The S parameter from 50 MHz to 1 GHz is given in Fig. 6. We can see that the small signal gain is 16.5 dB with high flatness of less than $\pm$1 dB. The S_{11} and S_{22} are all below –8 dB and the S_{12} is below –23 dB. Good noise performance is obtained, as shown in Fig. 7. The measured NF is 1.7–2.9 dB in the designed band. The feedback resistors R_4 and R_1 introduce the thermal noise to some extent. However, it is still good enough considering that the noise figure is normally 4–9 dB for the CATV amplifier in applications. Figure 8 gives the relation of the output power versus the input power at 850 MHz and it shows that the output 1-dB compressing point is up to 18.3 dBm.

The inter-modulation distortion of a microwave amplifier is often specified in IP2 and IP3. The greater the IP2 and IP3, the lower the distortion products and the higher the quality of the CATV signals. Figures 9 and 10 present the measurements of the IIP2 (second order input intercept point) and IIP3 (third



(a)



(b)

Fig. 5. (a) Photo of the PCB. (b) Test bench of the chip.

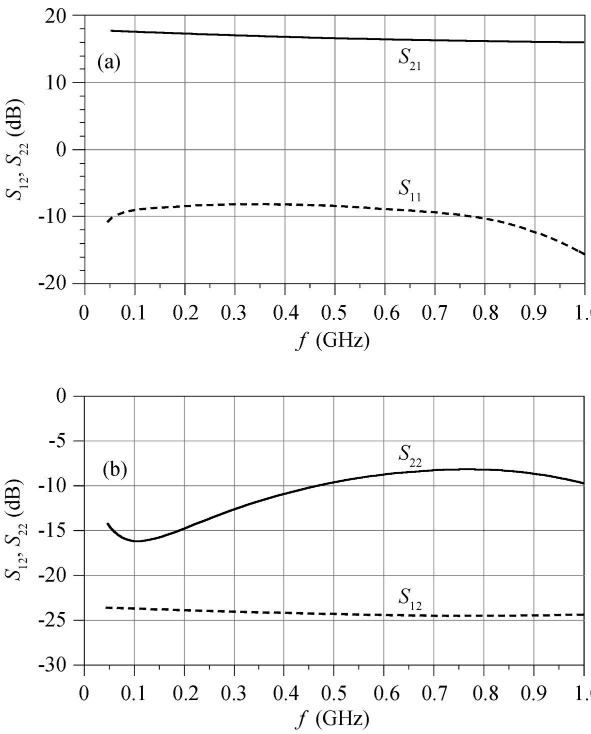


Fig. 6. S parameter from 50 MHz to 1 GHz.

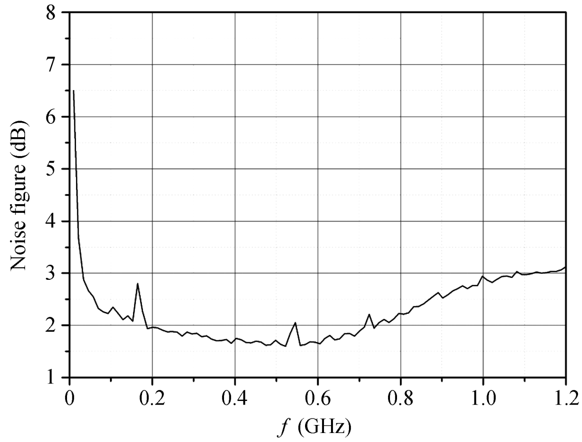


Fig. 7. Noise figure.

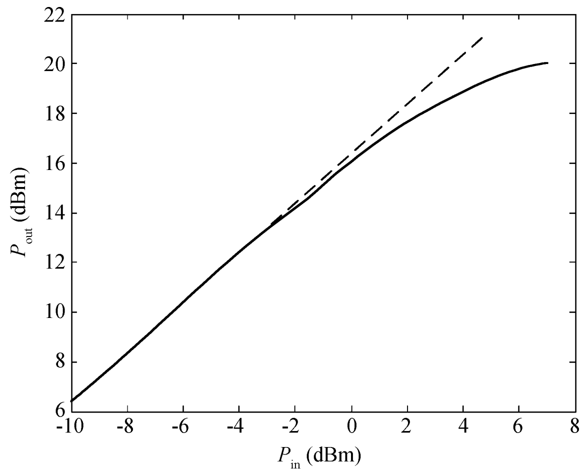


Fig. 8. Measured P_{1dB}.

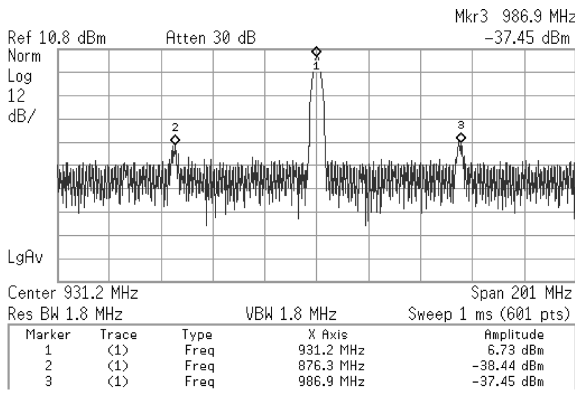


Fig. 9. IIP2 test.

order input intercept point) at 986.5 MHz. For the IIP2 test, the input powers of two tones are both –10 dBm and the frequency is 55.25 MHz and 931.25 MHz, respectively. For the IIP3 test, the input powers of two tones are also both –10 dBm and the frequency is 986.5 MHz and 992.5 MHz, respectively. IIP2 and IIP3 can be set by the following equations,

$$\mathrm{IIP3} = P_{\mathrm{in}} + (P_{\mathrm{out}} - P_{\mathrm{IM3}})/2, \tag{3}$$

$$\mathrm{IIP2} = P_{\mathrm{in}} + (P_{\mathrm{out}} - P_{\mathrm{IM2}}), \tag{4}$$

where P_{in} is the input power, P_{out} is the output power, P_{IM3} is the power of 3rd order intermediation product IM3 and P_{IM2} is the power of 2nd order intermediation product IM2. According to the measurements result as Figs. 9 and 10, we can get the IIP2 and IIP3 as 34.7 dBm and 16 dBm, respectively. This exhibits excellent performance of linearity.

Because of the large number of separate signals involved

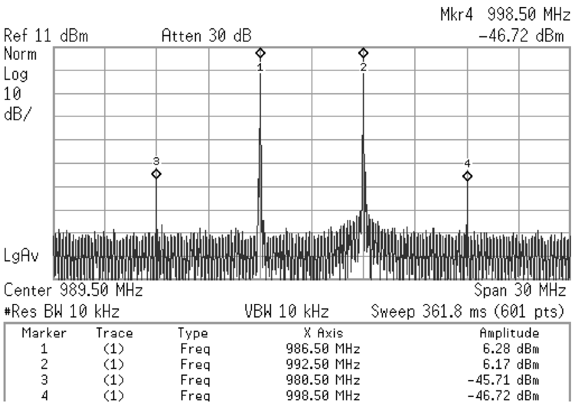


Fig. 10. IIP3 test.

Table 1. Performance summary of the circuit.

Parameter	Value
Supply voltage	5 V
Bandwidth	50 MHz–1 GHz
S_{21}	16.5 dB
S_{11}	< 8 dB
S_{22}	< 8 dB
IIP2	34.7 dBm
IIP3	16 dBm
Noise figure	1.7–2.9 dB
Power consumption	110 mA @ 5 V
CSO (160 channels)	68 dBc
CTB (160 channels)	77 dBc

in the CATV distribution system, the CATV industry measures third-order distortion in terms of CSO (composite second order) and second-order order distortions by CTB (composite triple beat). The cable carries a number of video NTSC or PAL channels modulated onto a carrier. When these multiple carriers pass through amplifiers, there is so called inter-modulation distortion leading to poor picture quality down the line. CTB and CSO are two such parameters measured to observe the picture quality[10−12]. CTB and CSO represent "composite triple beat ratio" and "composite second order ratio" in CATV broadcast. We verified the CSO and CTB performance with 160 channels in ADS. The simulated CSO and CTB are high up to 68 dBc and 77 dBc, respectively.

The performance summary is given in Table 1. It shows that the designed circuit meets the stringent requirements of the CATV systems.

4. Conclusions

In this article, we present a 50 MHz–1 GHz low noise and high linearity amplifier MMIC for cable TV applications. A shunt AC voltage negative feedback combined with source current negative feedback was adopted to increase the bandwidth and linearity. A novel DC bias feedback was introduced to stabilize the operation point, which improved the linearity further. The circuit was fabricated in a Win semiconductor using a 0.15 μm InGaAs PHEMT process. The test was carried out in 75 Ω systems from 50 MHz to 1 GHz. The measurement results gave a small signal gain of 16.5 dB with little gain ripples of less than ± 1 dB. An excellent noise figure of 1.7–2.9 dB was obtained in the designed band. IIP2 is 34 dBm and IIP3 is 16 dBm. The CSO and CTB are high up to 68 dBc and 77 dBc, respectively. It exhibited very good linearity. The chip area is 0.56 mm^2 and the power dissipation is 110 mA with a 5 V supply. This proves that the designed chip is ideally suited to cable TV systems.

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