A 4 GS/s 4 bit ADC with 3.8 GHz analog bandwidth in GaAs HBT technology*

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Abstract: An ultra-wideband 4 GS/s 4 bit analog-to-digital converter (ADC) which is fabricated in 2-level interconnect, 1.4 μm InGaP/GaAs HBT technology is presented. The ADC has a –3 dB analog bandwidth of 3.8 GHz and an effective resolution bandwidth (ERBW) of 2.6 GHz. The ADC adopts folding-interpolating architecture to minimize its size and complexity. A novel bit synchronization circuit is used in the coarse quantizer to eliminate the glitch codes of the ADC. The measurement results show that the chip achieves larger than 3.4 ENOBs with an input frequency band of DC–2.6 GHz and larger than 3.0 ENOBs within DC–4 GHz at 4 GS/s. It has 3.49 ENOBs when increasing input power by 4 dB at 6.001 GHz of input. That indicates that the ADC has the ability of sampling signals from 1st to 3rd Nyquist zones (DC–6 GHz). The measured DNL and INL are both less than $\pm$0.15 LSB. The ADC consumes power of 1.98 W and occupies a total area of 1.45 × 1.45 mm^2.

Key words: ADC; folding; interpolating; GaAs; ultra-wide-band; synchronization
DOI: 10.1088/1674-4926/32/6/065007 **EEACC:** 2570B

1. Introduction

There has been a continued trend in telecommunication standards moving from narrow band to wide band, from lower to higher carrier frequencies. The high-speed wide band analog-to-digital converter (ADC) is the key component of, e.g., ultra-wideband (UWB) communication systems, digital radar system, software-defined radio, and electro-optical receiver. The ADC presented in this paper is designed for a UWB receiver which can capture signals from 1 to 3 Nyquist-zones. That enables the ADC operating in under-sampling mode for direct down conversion of radio frequency (RF) signals.

Previous works[1−15] have demonstrated low bit wide ultra high speed ADCs with a sample frequency of 1–50 GHz which are fabricated in SiGe BiCMOS, CMOS, InP HBT, and GaAs HBT technologies. The ultra high speed ADC which is built in GaAs HBT has been rare during the last 10 years. The state-of-the-art GaAs HBT ADC developed in 1995 achieves 4 GS/s with 6 bit resolution[10]. It shows that the GaAs technology still has a comparable performance to other technologies.

A 3.8 GHz bandwidth 4GS/s 4bit ADC which is fabricated by commercial 1.4 μm InGaP/GaAs HBT technology is presented in this paper. The ADC consumes power of 1.98 W and occupies a total area of 1.45 × 1.45 mm^2. Compared to other technologies, GaAs HBT technology has the advantages of higher substrate resistance and higher breakdown voltage, which are important in mixed-signal MMIC design. It also costs much less than InP HBT and SiGe technologies due to its simpler process and lower precision requirement of the masks. In addition, InGaP/GaAs HBTs have been shown to be inherently radiation hard, making them well suited for use in the space environment[16, 17].

2. Architecture and operational principle

The architectures of high speed ADCs mainly include flash, two-step, folding-interpolating (FI) and pipeline. Furthermore, the time-interleave technique can be used to expand the sample frequency of any ADC architecture, but it usually needs extra calibration circuits to ensure that the ADC slices have the same amplitude response which produces more challenges to the clock distribution circuit design and acquires more area and power consumption. Flash architecture is usually chosen for ADCs with high speed and low pre-

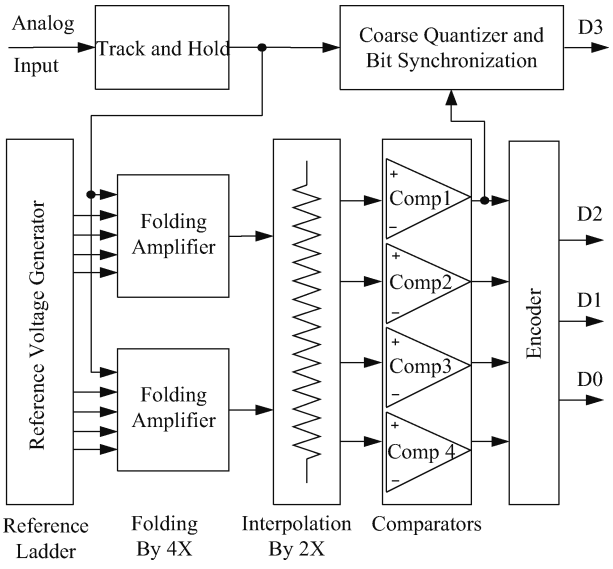

Fig. 1. Block diagram of the proposed ADC.

* Project supported by the State Key Development Program for Basic Research of China (No. 2010CB327505).
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Received 17 December 2010, revised manuscript received 29 December 2010

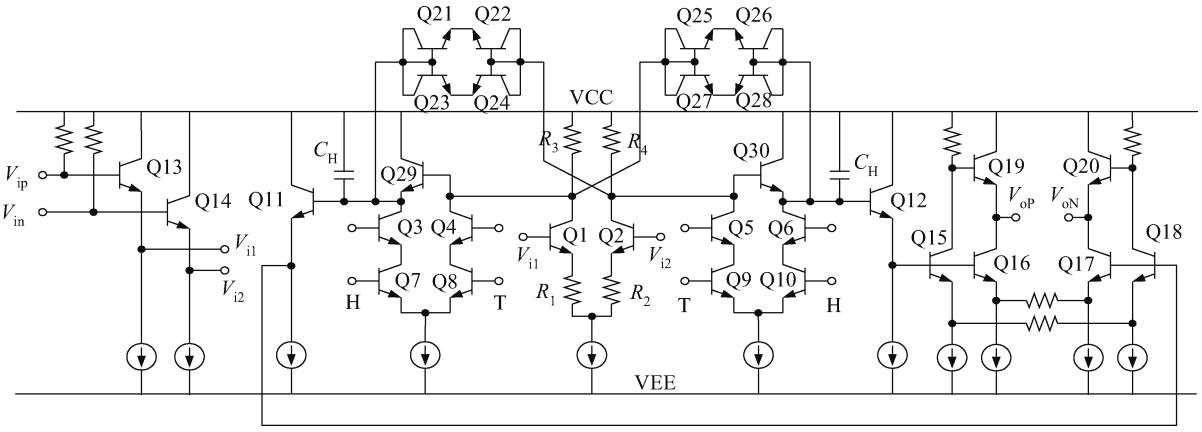

Fig. 2. Circuit diagram of the track/hold amplifier.

cision (4 to 6 bits). However, it calls for $2^{\text{number of bits}}-1$ of comparators, and an encoding circuit with $2^{\text{number of bits}}-1$ inputs. In contrast, folding-interpolating architecture splits the ADC into a fine ADC and a coarse ADC. The fine ADC converts the folded signal while the coarse ADC directly converts the input signals. The architecture reduces the number of comparators and simplifies the encoder. E.g., a 4-bit flash converter needs 16 comparators and a 16-to-4 encoder while the folding-interpolating architecture only needs 4 comparators and a simple encoder. FI architecture is chosen in this paper, which offers the best trade-off between speed, accuracy and power consumption in GaAs HBT technology. In order to eliminate the glitch codes of FI ADC, a 1-bit coarse quantizer with bit synchronization circuits is built. The block diagram of the proposed ADC chip is shown in Fig. 1.

As shown in Fig. 1, the output of the track-and-hold (T/H) circuit is applied to the coarse quantizer and two folding amplifiers. Then it is compared to the reference voltages and folded into 2 signals by the folding amplifiers. The outputs of the folding amplifiers, which are applied to four comparators after $2\times$ of interpolation, are a set of phase-shifted sinusoid-like signals. The outputs of the comparators are the representation of the input signal in circular thermometer codes. These codes are eventually converted back to binary codes to produce the three least significant bits (LSBs) by a digital encoder. The most significant bit (MSB) is generated by a 1-bit coarse quantizer. A synchronization circuit is built to make the coarse quantizer synchronize with the fine ADC encoder. The ADC only needs 2 folding amplifiers and 4 comparators to keep the sampling speed as high as 4 GS/s.

3. Circuit design

3.1. Track/hold amplifier

In a high speed ADC design, the track/hold amplifier (THA) is a major design issue. The distortion of the front end T/H will directly affect the performance of the ADC. The structure retained for the T/H stage was based on a fully differential switched emitter follower (SEF), since this structure is well known for its robustness[18, 19]. The switched diode bridge is another THA topology, but it is not suitable for this GaAs HBT technology with pure NPN transistors[20]. A simplified circuit diagram of the THA circuits is given in Fig. 2. It consists of an input buffer, sampling switches and output buffers. The differential input buffer consists of two differential emitter followers (Q13 and Q14) and a differential pair (Q1 and Q2). The differential pair with negative feedback resistors (R_1 and R_2) is loaded with resistors (R_3 and R_4). The differential outputs of the input buffer are connected to two switched-emitter-followers (SEF). Each SEF is made up of five transistors (Q3 − 4, Q7 − 8, Q29 and Q5 − 6, Q9 − 10, Q30), a holding capacitor (C_H) and two emitter followers (Q11 and Q12). In bipolar technology, the base current of transistors cannot be omitted, thus the voltage "stored" in the hold capacitors will drop on the hold mode time duration. There is a compromise between the voltage droop rate and the analog bandwidth of the THA by choosing a proper value for C_H. Lowering the value of C_H increases the bandwidth but reduces the drop rate. A 400 fF of C_H is chosen to achieve a wide analog bandwidth and keep the drop rate as low as 25 mV/ns in this work. A highly linear differential buffer is adopted to eliminate the voltage drop of the SEF outputs and, at the same time, to drive the coarse quantizer and the folding amplifiers. No voltage drop is observed in simulation at the node VoP and VoN in Fig. 2.

Two extra feed forward capacitors are used to provide a negative feed-through for the input to cancel out the feed through of the SEF in the hold phase. Each capacitor is implemented by four transistors with the same size of Q29 and Q30. The value of the feed forward capacitor is exactly the same as the C_{BE} of Q29 and Q30 in the hold phase. Figure 3 shows a comparison of THA outputs with and without the feed forward capacitors (C_{ff}) at a 4 GHz sampling frequency.

The THA output without C_{ff} ($V_{o\_wo\_Cff}$) has a voltage drift caused by the feed-through of the SEF in the hold phase, as shown in Fig. 3. In contrast, the THA output with C_{ff} (V_{o_Cff}) markedly suppresses the voltage drift.

3.2. Folding amplifier

The folding amplifier is used to convert the full scale input signal into the folded signal. In this paper, the 4 bit ADC contains 2 folding amplifiers, which generate 2 folded signals of the input voltage. The offset of the folded signals is 119 mV. The 2 differential outputs of the folding amplifiers are then in-

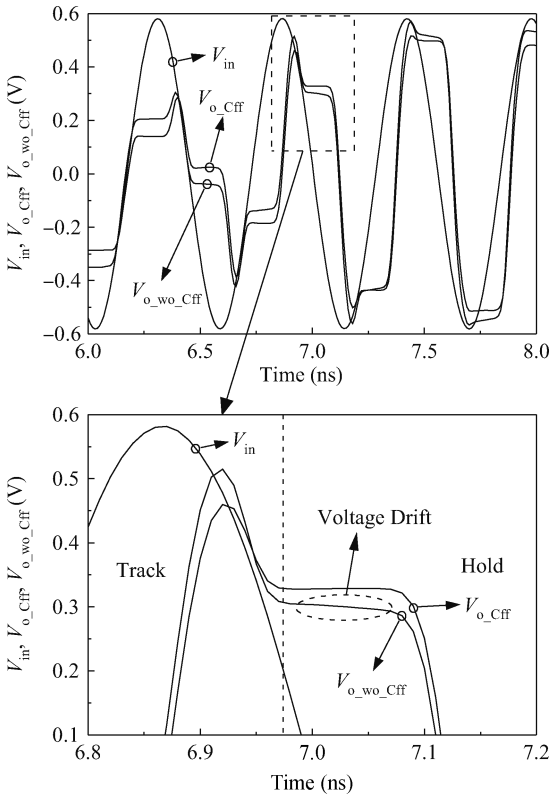

Fig. 3. Comparison of THA outputs with C_{ff} or without C_{ff} at 4 GS/s.

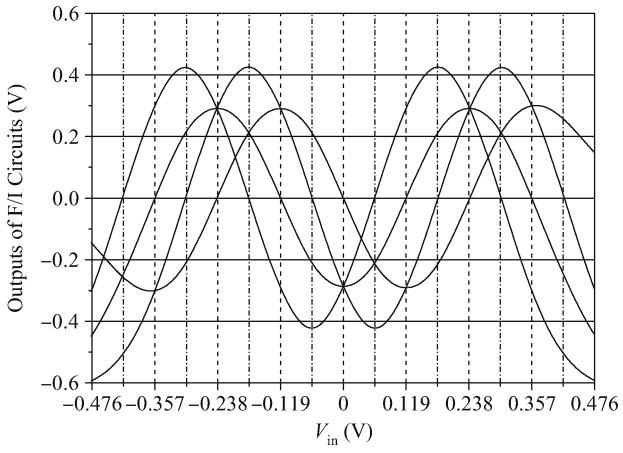

Fig. 4. Static response of F/I circuits.

terpolated to 4 signals by using interpolation resistors. The interpolation operation also provides an extra benefit of improving the linearity of the ADC[4]. The folding amplifiers are designed to be full differential, which improves both the common mode rejection of the input and the power to signal rejection ratio (PSRR). The static response of the folding-interpolating circuits is shown in Fig. 4.

The F/I circuits cut the input voltage into 16 levels. Each level is about 59.5 mV (LSB) and the full scale of the F/I circuits is about ±476 mV. This enables the following comparators to only use cross zero comparison, which can be easily realized using bipolar differential pair.

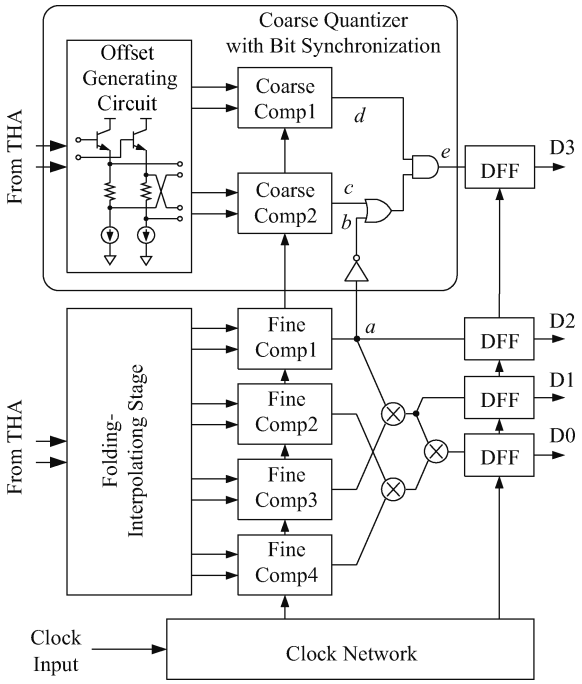

Fig. 5. Detailed structure of coarse and fine quantizers.

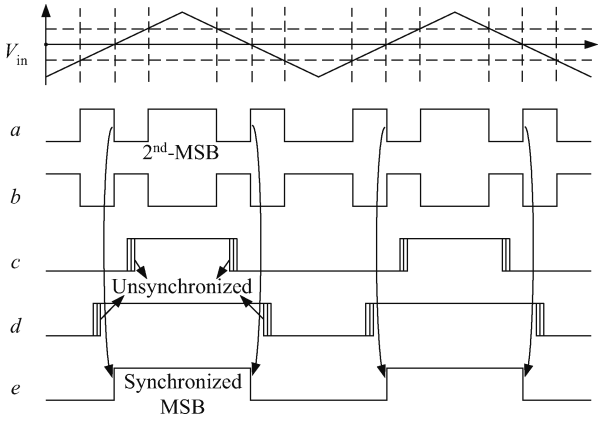

Fig. 6. Waveforms of bit synchronization circuits of coarse quantizer.

3.3. Coarse and fine quantizers

The detailed structure of coarse and fine quantizers is shown in Fig. 5. The coarse quantizer includes an offset generating circuit, some logic gates for bit synchronization and two comparators. The fine quantizer utilizes 4 comparators and 3 XOR gates to encode the 4 bits of circular thermometer codes into 3 bits of binary data. The encoding circuits are much simpler than those in a 4 bit flash ADC.

The offset generating circuit in the coarse ADC shifts the input signal up and down a little to generate two signals c and d which are not synchronized with the fine quantizer. Then the signals are combined with the 2nd-MSB signal by a simple logic operation $e = (\bar{a} + c)d$ to generate the synchronized MSB signal. This operation eliminates the glitch codes of the F/I ADC, and the correlated waveforms are shown in Fig. 6.

Both the coarse and the fine ADC need comparators to convert the analog signal to digital "0" or "1" at each positive edge of the sample clock. The comparators are designed to op-

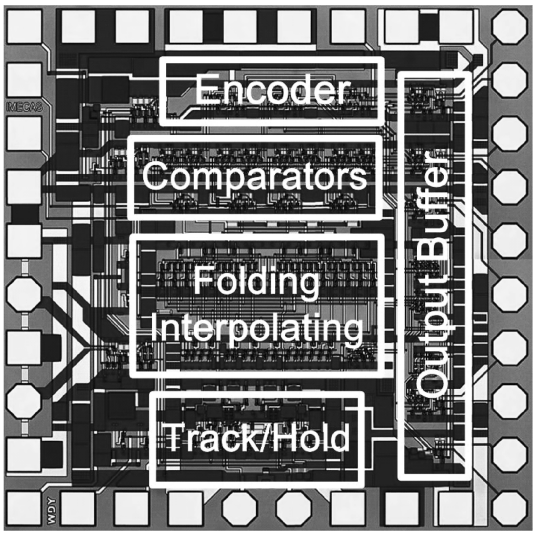

Fig. 7. Die photo of the ADC chip.

erate at 4 GHz. The main design target is to achieve a setup time much less than half the clock cycle (125 ps) and keep the impact to the adjacent comparators as low as possible. The comparators are based on differential latch topology with an input bandwidth (–3 dB) larger than 9 GHz and with a delay of about 20 ps. Preamplifiers are adopted to obtain a proper gain to make sure that the differential voltage amplitudes of the interpolating stage are big enough to be determined by the comparators and also to provide isolation between the interpolating resistors and comparators.

3.4. Layout design

Because the analog circuits are much more sensitive than the digital circuits, the analog and digital parts of the circuit are isolated to two different domains to prevent the coupling between them. The layout of the clock tree is split into three domains and clock loads of each domain are similar to ensure that all of the DFFs are properly driven. A clock skew between the THA and comparators is purposely incorporated into the design to increase the maximum sampling frequency. Figure 7 shows the die photo of the whole ADC chip. The chip consists of 487 HBTs, 284 resistors and 36 pads.

To optimize the clock tree and prevent signal integrity problems, a 2.5-D EM simulation is performed on the circuit by extracting interested parts of layout into ADS momentum. The whole circuit is then co-simulated in the schematic simulation environment with the EM model, which is generated by ADS momentum. The clock skew between different DFFs can be checked and adjusted accurately by using this simulation method.

4. Measurement and results

A wideband 4 channel digital oscilloscope is used for receiving the high speed output data stream of the ADC chip. The bit rate of each output digital signal is 4 Gbps, which generally needs at least 5 GHz bandwidth for data capture. A digital oscilloscope, Agilent DSA91304A, which has four 13 GHz input channels is chosen to directly capture the 4 channel data

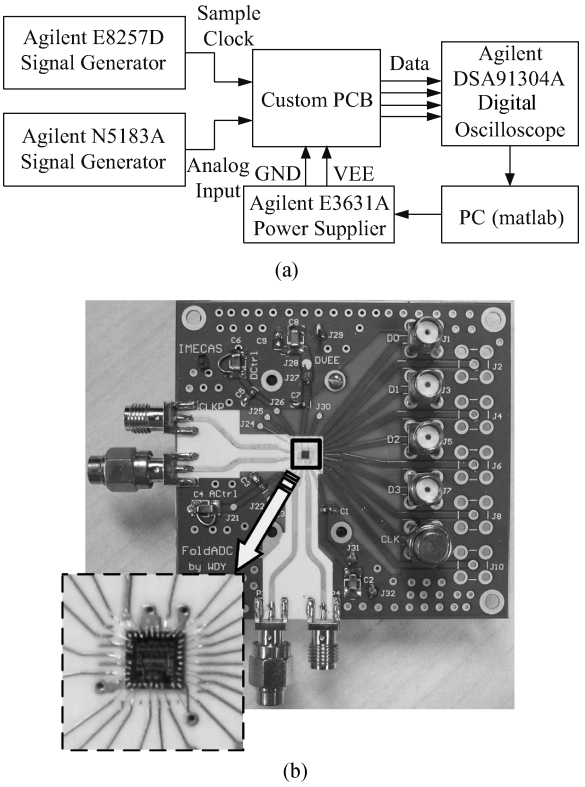

Fig. 8. (a) ADC measurement setup diagram. (b) Photograph of ADC evaluation board.

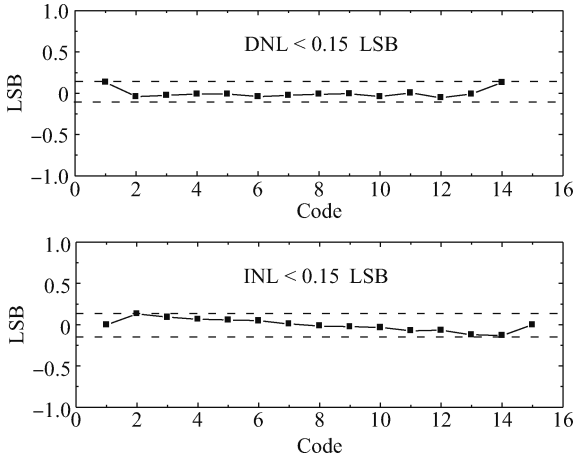

Fig. 9. Measured DNL and INL of the ADC at 4 GS/s.

stream. The measurement setup is shown in Fig. 8(a). The delay of each of the coaxial cables that are connected to the oscilloscope must be measured first and then calibrated to align the 4 signal channels. A photograph of the ADC evaluation board is shown in Fig. 8(b).

The DNL and INL are measured at 4 GHz of sample frequency by using a ramp signal as the input, as shown in Fig. 9. This shows that both the DNL and the INL are less than ± 0.15 LSB. The measured spur free dynamic range (SFDR), signal to noise and distortion ratio (SNDR) and effective number of bits (ENOB) are shown in Fig. 10. This shows an ENOB of larger than 3.4 with an input signal frequency of DC–2.6 GHz and larger than 3.0 in DC–4 GHz (1st and 2nd Nyquist zone). The analog response is estimated by transforming the 4 bit output

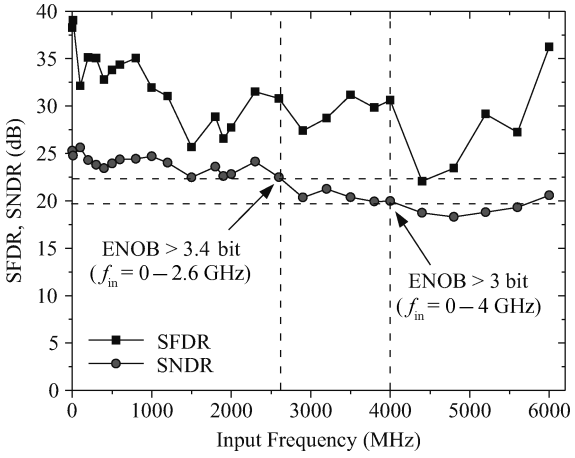

Fig. 10. Measured SFDR and SNDR versus input frequency at 4 GS/s.

Table 1. Summary of the fabricated ADC.

Parameter	Value
Technology	1 μm InGaP/GaAs HBT (2-metal)
Resolution	4 bits
Sampling rate	4 GS/s
Input bandwidth (–3 dB)	3.8 GHz
Input range	±450 mV differential
ENOB	3.96 @ f_{in} = 100 MHz 3.50 @ f_{in} = 2.001 GHz 3.02 @ f_{in} = 4.001 GHz 3.12 @ f_{in} = 6.001 GHz 3.49 @ f_{in} = 6.001 GHz (with increased 4 dB of input amplitude)
SFDR (DC–4 GHz)	30.6 dB (Average) 25.7 dB (Worst case)
Max DNL	±0.15 LSB
Max INL	±0.15 LSB
Power supply	Single –6 V
Power consumption	1.98 W
Die size	1.45 × 1.45 mm^2

code (peak to peak) into a logarithmic scale. The ADC achieves a measured analog bandwidth of 3.8 GHz, which enables it for direct sampling of the UWB signal at the 2nd Nyquist zone.

Figure 11 shows the reconstructed spectrum of the sampled data at 4 GS/s with an input frequency of 300 MHz, 1.8 GHz and 3.8 GHz. The ADC performs 3.7 ENOBs at f_{in} = 300 MHz; 3.6 bits at 1.8 GHz; and 3.0 bits at 3.8 GHz.

Table 1 summarizes the main feature of the ADC. The chip is fabricated using a commercial 2-level interconnect 1.4 μm InGaP/GaAs HBT technology with a f_t of about 60 GHz. The ADC has a maximum sampling frequency of 4 GS/s and 4 bit resolution. It achieves 3.96 ENOBs at 100 MHz, 3.5 bits at 2.001 GHz, 3.02 bits at 4.001 GHz and 3.12 at 6.001 GHz of input with a fixed input power of 4 dBm. The ENOB can be further improved to 3.49 bits at 6.001 GHz of input when increasing the input power to 8 dBm. This indicates that the ADC has the ability of capturing signals from DC–6 GHz (1st to 3rd Nyquist zones). The ADC consumes power of 1.98 W from a single –6 V of power supply and occupies an area of 1.45 × 1.45 mm^2.

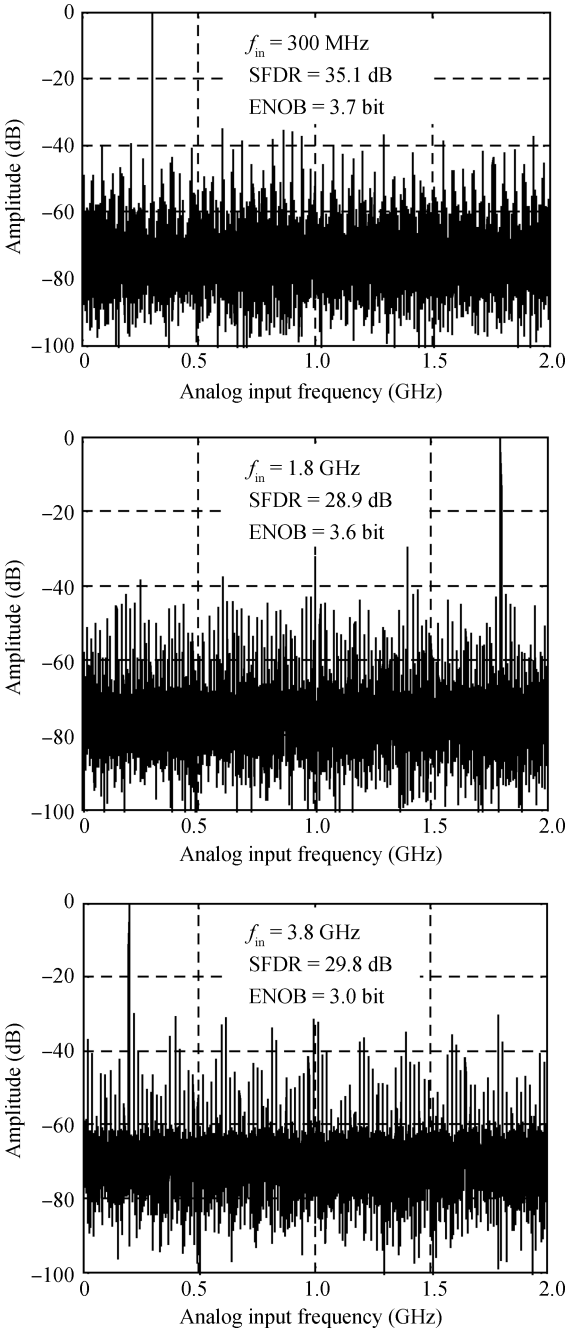

Fig. 11. Reconstructed spectrum at 4 GS/s with an input frequency of 300 MHz, 1.8 GHz and 3.8 GHz.

5. Survey

Table 2 summarizes the ultra-high-speed ADCs with a sample frequency larger than 1 GSps in different technologies. It can be concluded that ADCs fabricated in CMOS technology typically consume much less power than those in bipolar technologies, such as SiGe, InP and GaAs. ADCs usually need to be calibrated when fabricated by CMOS, but SiGe HBT, InP and GaAs ADCs do not need calibration. It should be noted that in SiGe BiCMOS technology, SiGe HBT is chosen to build the main circuit block rather than CMOS.

Table 2 shows a growing trend that SiGe BiCMOS and deep sub-micron CMOS technologies are being used in ultra-

Table 2. Survey of ultra-high-speed ADCS (> 1 Gsps, < 7 bits).

Reference	Technology	Architecture	f_s (GHz)	Resolution (bits)	Bandwidth (GHz)	ENOB @ f_{in}	Power (W)	Year	Location
[1]	0.18 μm SiGe BiCMOS	Flash	35	4	8(1)	3.2 @ 8 GHz	4.5	2009	Toronto, Canada
[2]	0.18 μm SiGe BiCMOS	Flash/TI	50	5	18(1)	3.4 @ 22 GHz	5.4	2010	NJ, USA
[3]	0.13 μm SiGe BiCMOS	Flash	22	5	5.3(1)	4.4 @ 5 GHz	3	2006	Ottawa, Canada
[5]	0.13 μm SiGe BiCMOS	Flash	20	5	9(1), 20(2)	4.1 @ 9 GHz	6.5	2009	MN, USA
[6]	0.18 μm CMOS	Flash	4	4	0.8(1)	3.48 @ 0.1 GHz	0.61	2007	CA, USA
[11]	0.13 μm CMOS	Flash	10	4	1(1)	3.4 @ 1 GHz	0.115 (Core)	2008	Taiwan, China
[13]	0.18 μm CMOS	Flash	2	6	< 0.2(1)	5.78 @ 1.22 MHz	0.57	2010	Nanjing, China
[14]	0.18 μm CMOS	Flash	2	4	N/A	N/A	0.038	2009	Beijing, China
[15]	0.13 μm CMOS	Flash	1	6	0.1(1)	4.86 @ 500 MHz	0.066	2009	Shanghai, China
[12]	65 nm CMOS	SAR/TI	40	6	7.3(1)	4.5 @ 10 GHz	1.5	2010	Ottawa, Canada
[7]	1 μm InP HBT	Flash	20	3	< 10(1)	2.3 @ 10 GHz	3.84	2004	Kanagawa, Japan
[8]	InP HBT ($f_t \approx$ 108 GHz)	Flash	10	4	N/A	3.9 @ 4.9 GHz	5.9	2004	CA, USA
[9]	0.8 μm InP HBT	FI	5	7	10(1)	5.7 @ 7.5 GHz	8.4	2008	CA, USA
[10]	1.4 μm GaAs HBT	FI	4	6	1.8(1)	4.7 @ 1.8 GHz	5.7	1995	CA, USA
This work	1.4 μm GaAs HBT	FI	4	4	2.6(1), 3.8(2)	3.50 @ 2 GHz 3.02 @ 4 GHz 3.12 @ 6 GHz	1.98	2010	Beijing, China

(1) Effective resolution bandwidth (ERBW); (2) Analog –3 dB bandwidth

high-speed ADC design to meet the growing needs of the bandwidth of wired or wireless communication. The state-of-the-art SiGe BiCMOS ADC which is developed by Lee achieves 50 GHz of sampling frequency, 18 GHz of ERBW and 5 bit resolution. It adopts two channel interleaved flash architecture and consumes power of 5.4 W[2]. In comparison, the state-of-the-art CMOS ADC which is fabricated by 65 nm CMOS achieves 40 GS/s, 6 bit resolution and consumes power of only 1.5 W. It uses 16 interleaved Successive Approximation (SAR) ADCs. Each sub ADC can operate at 2.5 GS/s and consumes power of < 40 mW[12]. ADCs built in InP HBT and GaAs HBT have become rare during the last 10 years, but they still show a comparable performance. The state-of-the-art GaAs HBT ADC achieves 4 GS/s with 6 bit resolution, which was developed by Poulton in 1995[10].

This paper proposes a 4 GS/s 4 bit ADC fabricated by InGaP/GaAs HBT technology which has a competitive performance compared to those in other technologies. Compared to other technologies, GaAs HBT has the advantages of higher substrate resistance and higher breakdown voltage, which are important in mixed-signal MMIC design.

6. Conclusion

In this paper, a 4 GS/s 4 bits ADC with folding-interpolating architecture is fabricated and measured. The ADC adopts switched-emitter-follower as its THA core, which achieves an analog input bandwidth of 3.8 GHz. A novel bit synchronization circuit is used in the coarse quantizer to eliminate the glitch codes of the F/I ADC. The chip is mounted to a custom PCB board and measured using a Wideband Oscilloscope. The measurement results show that the chip achieves larger than 3.4 ENOBs with an input frequency band of DC–2.6 GHz and larger than 3.0 ENOBs with DC–4 GHz (1st and 2nd Nyquist zone). It has 3.49 ENOBs when applying 8 dBm of input power with 6.001 GHz of input at 4 GS/s. It shows that the ADC has the ability of sampling signals from 1st to 3rd Nyquist zones (DC–6 GHz). The measured DNL and INL are

both less than ± 0.15 LSB. The chip was designed using 2-level interconnect 1.4 μm GaAs HBT technology with a full scale of input of about ± 450 mV, and it is suitable for ultra-wideband digital receivers. In addition, InGaP/GaAs HBTs have been shown to be inherently radiation hard for both proton and electron exposure, and they are well suited for use in the space environment[16, 17]. To the best of our knowledge, this work represents the fastest single chip ADC with resolution of 4bits or above in mainland China.

Acknowledgment

We would like to thank Dr. Toby Dong and Lu Jia of the electronic measurement group of Agilent Technologies for their support of our measurements.

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