A 9.8-mW 1.2-GHz CMOS frequency synthesizer with a low phase-noise LC-VCO and an I/Q frequency divider

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Abstract: A 1.2 GHz frequency synthesizer integrated in a RF receiver for Beidou navigation is implemented in standard 0.18 μm CMOS technology. A distributed biased varactor LC voltage-controlled oscillator is employed to achieve low tuning sensitivity and optimized phase noise performance. A high-speed and low-switching-noise divider-by-2 circuit based on a source-coupled logic structure is adopted to generate a quadrature (I/Q) local oscillating signal. A high-speed 8/9 dual-modulus prescaler (DMP), a programmable-delay phase frequency detector without dead-zone problem, and a programmable-current charge pump are also integrated into the frequency synthesizer. The frequency synthesizer demonstrates an output frequency from 1.05 to 1.30 GHz, and the phase noise is –98.53 dBc/Hz at 100-kHz offset and –121.92 dBc/Hz at 1-MHz offset from the carrier frequency of 1.21 GHz. The power dissipation of the core circuits without the output buffer is 9.8 mW from a 1.8 V power supply. The total area of the receiver is 2.4×1.6 mm^2.

Key words: Beidou receiver; frequency synthesizer; voltage-controlled oscillator; quadrature output divider; phase noise

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1. Introduction

With the continuous development in the feature size of MOSFETs, the low-power characteristic of CMOS integrated circuits has attracted more attention due to reliability and thermal issues[1, 2]. The CMOS frequency synthesizer is one of the most important building blocks in the implementation of a single radio chip in today's various wireless communication systems[3–5]. Therefore, to design a low-power frequency synthesizer is important for multi-gigahertz wireless communication systems as the battery lifetime is limited by the power consumption of the electronics circuit. A phase-locked loop (PLL)-based frequency synthesizer, which works similarly with the PLL circuit, can lock the phase of a divided feedback clock from the voltage-controlled oscillator (VCO) to the phase of reference clock, and the frequency division ratio is made variable to set the output frequency to meet the requirement of the system[6, 7].

This paper presents the design of a 1.2-GHz CMOS low-power frequency synthesizer for a Beidou receiver consuming only 9.8-mW at a 1.8-V power supply. In the proposed synthesizer, a distributed biased varactor LC-VCO is employed to achieve optimized phase noise performance, and a high-speed and low-switching-noise frequency divider circuit based on a source-coupled logic (SCL) structure is adopted to generate a quadrature local oscillating (LO) signal, which is used for quadrature downconversion of the Beidou receiver due to their good image-rejection performance.

2. Architecture of synthesizer

In this paper, a 1.2 GHz integer-N frequency synthesizer is implemented in the RF front-end system of a Beidou receiver, as shown in Fig. 1, to generate the quadrature local oscillating (LO) signal for quadrature downconversion. The frequency synthesizer, as shown in Fig. 2, is chosen to be a type-2 fourth-order loop, including phase frequency detector (PFD), charge pump (CP), voltage-controlled oscillator (VCO), third-order loop filter (LPF), adaptive frequency calibration (AFC) block, divider-by-R prescaler, and down-scaling circuit[8]. Except for the LPF, all circuit blocks are integrated on-chip, and programmably controlled by a serial peripheral interface (SPI) block to facilitate optimization and testing. The physical designs of the digital parts, such as SPI, AFC, and digital dividers, are digitally synthesized by EDA tools.

The down-scaling circuit includes four parts: a 2:1 quadrature frequency divider to provide I/Q signals, a dual-modulus prescaler (DMP), a programmable counter, and a pulse swallow counter[9]. The total division ratio M generated by dual-modulus prescaler $N/(N+1)$, programmable counter /P, and pulse swallow counter /S is

$$M = (N+1)S + N(P-S) = PN + S. \tag{1}$$

The input frequency is named as $f_{\rm OSC}$, so the output LO frequency $f_{\rm OUT}$ can be described as

$$f_{\rm OUT} = 2Mf_{\rm OSC}/R. \tag{2}$$

In this design, the division ration of divider-by-R is controlled by SPI. If the input frequency $f_{\rm OSC}$ is 10 MHz, we can set the division ration of divider-by-R as 5, so the reference frequency $f_{\rm REF}$ of PFD is 2 MHz. The loop bandwidth can be set to 50 kHz, which is lower than 1/10 of the $f_{\rm REF}$. The dual-modulus prescaler is 8/9 prescaler.

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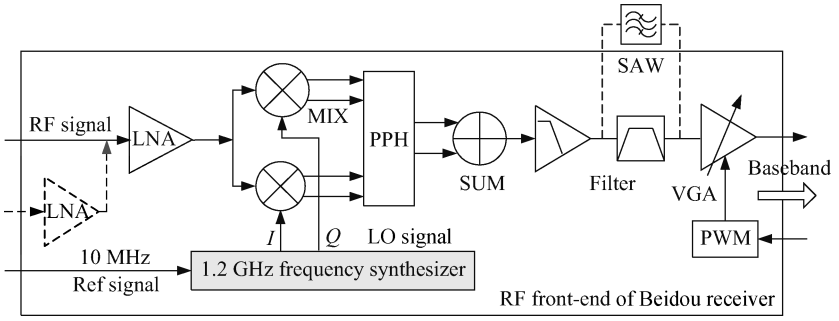

Fig. 1. Architecture of RF front-end of Beidou receiver.

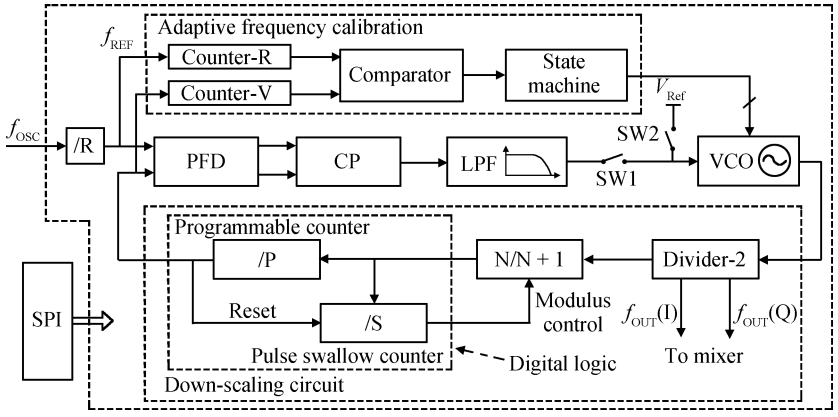

Fig. 2. Architecture of integer-N frequency synthesizer.

3. Building block implementations

3.1. Low phase noise LC-VCO

One of the most important performances of VCO is the phase noise, which is a factor to evaluate how much the spectrum spread from the center frequency. The sources of noise coming from several different frequencies make it difficult to discern which noise is the dominant one. In the conventional Leeson's formula[10], phase noise is given by

$$L(f_{\rm m}) = 10\ \lg\left\{\frac{2FkT}{P_{\rm s}}\left[1+\left(\frac{f_{\rm o}}{2Qf_{\rm m}}\right)^2\right]\left(1+\frac{f_{\rm c}}{f_{\rm m}}\right)\right\}, \tag{3}$$

where $f_{\rm o}$ is the carrier frequency, $f_{\rm m}$ is the offset frequency from $f_{\rm o}$, $f_{\rm c}$ is the flicker noise corner frequency, Q is the quality factor, $P_{\rm s}$ is the power consumption, F is the noise factor, k is Boltzmann's constant, and T is the temperature.

Any noise on the control line will modulate the carrier frequency and create additional phase noise[11], and this modulation effect will be determined by the VCO gain ($K_{\rm VCO}$)[12]. Taking this additional noise mechanism into account, Leeson's formula can be modified as

$$L(f_{\rm m},\ K_{\rm VCO}) = 10\ \lg\left\{\left(\frac{f_{\rm o}}{2Qf_{\rm m}}\right)^2\left[\frac{FkT}{2P_{\rm s}}\left(1+\frac{f_{\rm c}}{f_{\rm m}}\right)\right] + \frac{1}{2}\left(\frac{K_{\rm VCO}V_{\rm m}}{2f_{\rm m}}\right)^2\right\}, \tag{4}$$

where $V_{\rm m}$ is the total amplitude of all low frequency noise sources.

The features of wide band and low phase-noise have been in high demand in frequency synthesizers for the multiband RF transceivers[13]. Analyzed from Eq. (4), large $K_{\rm VCO}$ will degrade the phase noise $L(f_{\rm m}, K_{\rm VCO})$[11]. So, $K_{\rm VCO}$ is desired to be as small as possible in order to achieve low phase-noise performance, but a small $K_{\rm VCO}$ will decrease the frequency tuning range. At present, combining the analog and digital tuning is the most effective way for the LC-tank VCO design to achieve simultaneously small $K_{\rm VCO}$ and wide tuning range by using the varactor and switched-capacitor bank, respectively[11−13].

The proposed structure of a conventional fully-integrated cross-coupled CMOS LC-VCO is shown in Fig. 3. Analog tuning and digital tuning are realized by applying an analog voltage to the varactor and setting a proper digital code to the switched-capacitor bank, respectively. In this paper, an accumulation MOS (AMOS) varactor is applied to form the VCO varactor resonator, and a binary-weighted structure is adopted in switched-capacitor bank to expand the tuning range. Also, we apply the method of connecting several varactors in parallel and to bias them with different DC biases[14], so we can obtain lesser and constant $K_{\rm VCO}$. As an example, we adopt a structure of three-stage distributed biased varactor (DBV) resonator for the analog tuning, and a 3-bit binary-weighted switched-capacitor bank for the digital tuning. The simulated f–V characteristic of the proposed VCO is represented in Fig. 4, compared to the conventional biased varactor (CBV) VCO and only analog tuning (OAT) VCO, which have the same total number of varactors.

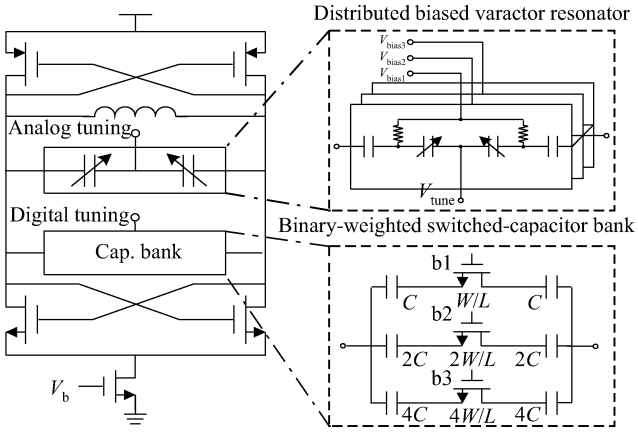

Fig. 3. Structure of proposed VCO.

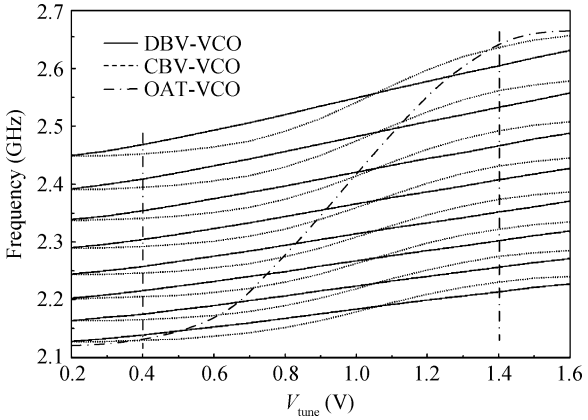

Fig. 4. Simulated $f-V$ characteristic of different VCO structures.

The simulation result shows that, based on the contribution of a three-stage DBV resonator and a 3-bit binary-weighted switched-capacitor bank, K_{VCO} is decreased largely with only a tiny decrease in tuning range, so it can improve the phase noise performance[11], especially over the tuning range from 0.4 to 1.4 V decided by our charge pump. In the schematic of the proposed LC-VCO, two complementary nMOS and pMOS are used to generate negative resistance to cancel losses in the LC resonator. The tail current source is controlled and configured programmably by a SPI block to achieve optimized phase noise performance and power consumption. The test result of VCO power is only 1.4 mW, which is significant for our low-power frequency synthesizer.

3.2. 2:1 quadrature frequency divider and 8/9 DMP

The output frequency of the frequency synthesizer is used as a LO signal adopted by mixer. Many RF transceivers apply a quadrature downconversion mixer due to their good image-rejection performance. In this paper, the adopted 2:1 quadrature frequency divider employs a master-slave D-flip-flop (DFF) with negative feedback to generate the I and Q components of LO, as shown in Fig. 5(a). Compared to the traditional RC-I/Q generation scheme, this approach is easier to implement, is lower in power consumption, and can offer smaller amplitude and phase imbalance. Compared to the injection-locked type, it shows more stable operation anda wider dividing range[1].

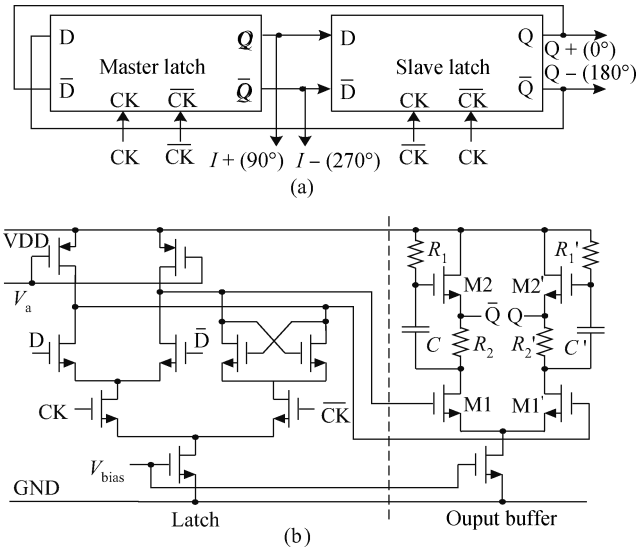

Fig. 5. (a) Block diagram of the divide-by-2 circuit. (b) Circuit of SCL latch with output buffer.

A novel latch circuit with an output buffer amplifier is proposed in the quadrature frequency divider, shown in Fig. 5(b), and a high-speed source-coupled logic (SCL) structure[15, 16] is used in the latch circuit to reduce the switching noise[17]. The inputs are driven by the VCO outputs directly, which have lower phase noise and large amplitude. In this paper, we use the PMOS transistors as the active loads to improve the precision of the resistance loads in the SCL circuit. The bias voltage V_a is grounded to increase the maximum operating frequency by operating PMOS in the linear region, which lowers the RC time constants associated with the output nodes[18].

The interference of load can affect not only the syntonic frequency but also the output amplitude, and so degrade the phase noise performance. So, we apply a novel high-speed output buffer to effectively isolate the parasitical capacitance from the loading site. This buffer introduces a left-half plane zero-point due to capacitance C, transistor M2, and resistors R_1 and R_2, as shown in Fig. 5(b). This zero-point contributes a larger bandwidth and band pass characteristic for the output buffer, so that the useful high frequency signal can pass through, and the output waveform can be reshaped. The transistor M2 is modeled as a source follower, which has a low output resistor. After the input signals pass through transistor M1, parts of them can go to the gate of transistor M2, so the efficiency of the output buffer amplifier will be improved. As a result, this buffer can yield a strong driving ability to drive the following circuit effectively. In addition, the buffer can adjust the DC voltage of the output according to the requirements of the mixer circuit. This divider consumes only 1 mA for dividing operation and 1 mA for buffering, and the operating frequency can be up to 4 GHz.

The 8/9 DMP applied in this paper consists of a divide-by-4/5 synchronous circuit, a divide-by-2 asynchronous circuit, and a modulus control block[16], as shown in Fig. 6. The 8/9 DMP block operates on the RF band, so a high speed DFF based on SCL structure, which is similar to the divider-by-2 circuit but without output buffer, is applied in the DMP circuit. And a novel NAND-DFF structure integrating the DFF

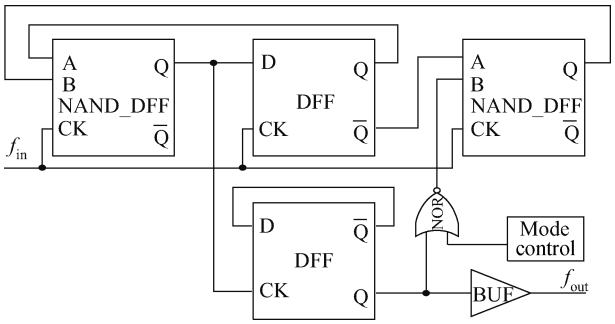

Fig. 6. Block of 8/9 DMP based on NAND-DFF.

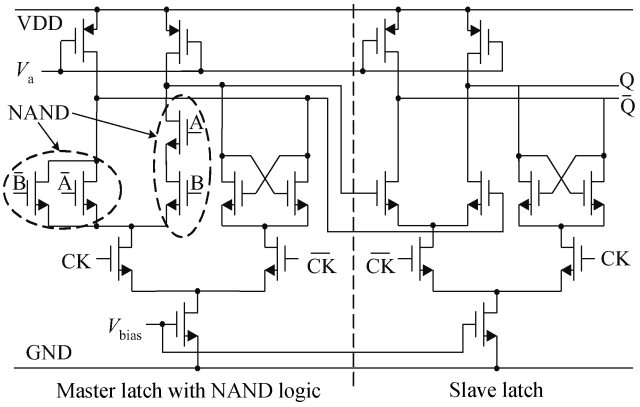

Fig. 7. Schematic of SCL DFF embedded NAND function.

and NAND logic functions is adopted to increase the operating speed and dividing capacity. The 4/5 counter will work in the 4 mode when the mode signal is set to high, and the input signal is divided by 8. The 4/5 counter will work in the 5 mode when the mode signal is set to low, and the total modulus becomes 9. The circuit of NAND-DFF is shown in Fig. 7.

The programmable counter, pulse swallow counter, divider-by-R, and control circuit work at a lower frequency band than the prescaler, so they were described by Verilog-HDL language and physically implemented by EDA tools.

3.3. PFD, CP and LPF

The PFD compares the frequency and phase between the feedback signal and the reference signal to generate a down or up signal to the CP. In this paper, a conventional PFD employed three-state machine structure based on standard DFF is implemented[19]. A delay cell is adopted that should be long enough to eliminate the dead-zone, while short enough to decrease the ripples on the control voltage of VCO[16, 20]. In this paper, a flexible programmable delay unit is inserted in the path of the reset signal to get the optimal delay value, so as to eliminate the dead-zone and minimize the voltage ripples easily under different process, voltage, and temperature (PVT) condition, as shown in Fig. 8(a).

The delay cell consists of several differential inverters, so the total delay time can be formed by adding the delay time of every inverter. The delay time of one inverter is given by $\tau_n = R_n C_n$, where R_n is the output resistor of inverter, and C_n is the output capacitor of inverter. Each inverter is controlled by

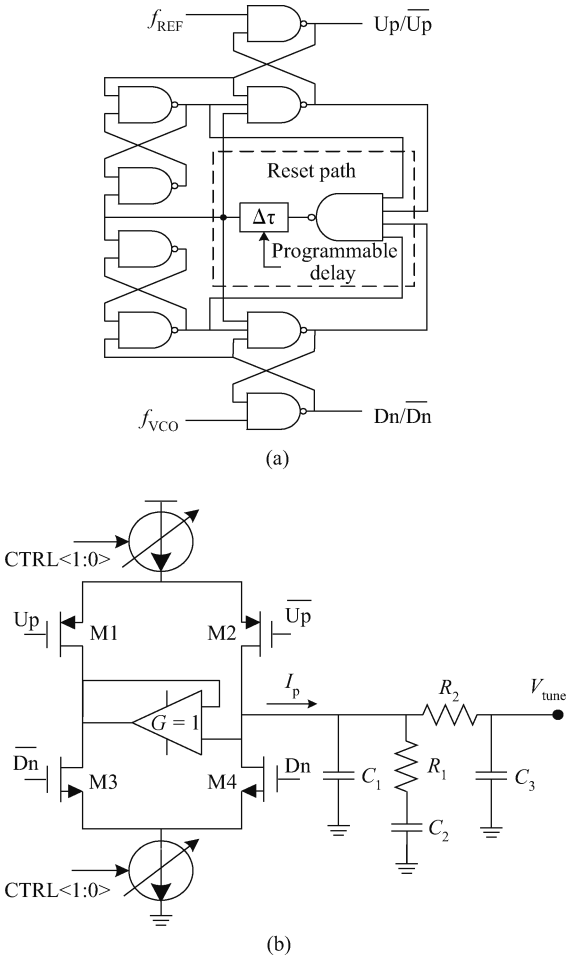

Fig. 8. (a) Block of PFD with programmable delay. (b) Simplified schematic of programmable CP.

an enable signal, and an additional capacitor ΔC will be added to the output of this inverter when the control signal is enabled, then the delay time of the inverter will be rearranged as $\tau_n = R_n(C_n + \Delta C)$. It is obvious that the delay time of each inverter becomes larger, the same as the total delay time. However, if the control signal is disabled, the delay time of the inverter will not be influenced by the capacitor ΔC. Overall, when the value of capacitor ΔC is fixed, the total delay time only varies with the input control signals, which can be programmed flexibly by the SPI digital interface.

The CP is controlled by the up and down signals come from PFD by switches. The conventional structures have a charge-sharing problem when the switches are switched. This feature will induce glitches in the CP current, and increase phase noise and power level of the PLL spurs. In this paper, a unity-gain buffer is inserted in the circuit of the CP to minimize the charge-sharing effect and the spurious tones at the VCO outputs[1, 20], as shown in Fig. 8(b). The performance of the CP is important for PLL, especially the charging and discharging current, which is a key influence element for the loop characteristic and phase noise of the PLL[21]. In this paper, a programmable CP structure is adopted in our design, in which the charging and discharging current I_p can be adjusted by the programmable current sources controlled by signal CTRL<1:0>, so to optimize the performance of PLL, such

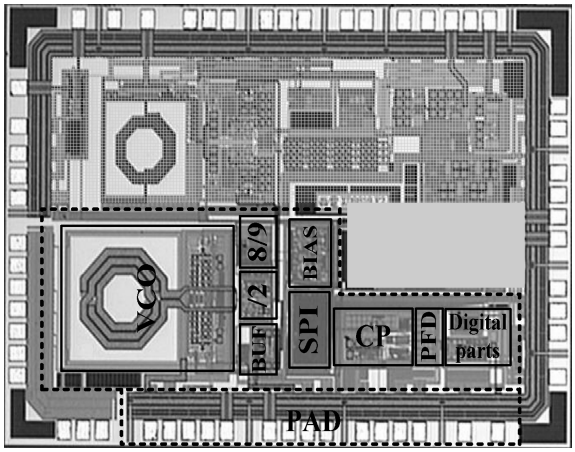

Fig. 9. Beidou receiver chip micrograph.

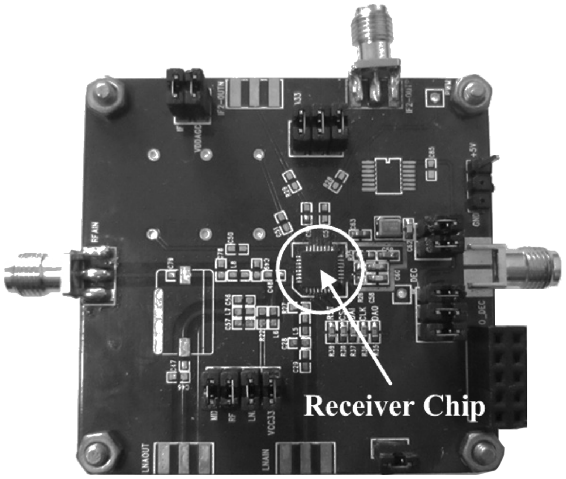

Fig. 10. Test PCB for Beidou receiver chip.

as lock time, stability and phase noise. By using this structure, the output voltage range of CP will not be influenced by the change in programmable current sources compared with other programmable CP structures, so the lock range of the PLL will remain invariant.

An off-chip third-order passive loop filter is applied in this paper, as shown in Fig. 8(b). The resulting PLL is then a type-2 fourth-order loop, which provides great noise suppression for the switching activities in the PLL. In this paper, we choose loop bandwidth $\omega_c = 50$ kHz, and phase margin $\phi_P = 50°$, according to Ref. [22], and the parameters of the loop filter are summarized as $C_1 = 10$ pF, $C_2 = 470$ pF, $R_1 = 110$ kΩ, $C_3 = 3.3$ pF, and $R_2 = 30$ kΩ.

4. Experimental results

Based on the structure shown in Fig. 2, this proposed frequency synthesizer is integrated in a RF receiver for Beidou navigation, and is fabricated in a 0.18 μm, 1.8 V, 1P6M, standard CMOS technology. The chip micrograph of our RF receiver is shown in Fig. 9, which has a size of 2.4 × 1.6 mm^2, including the pad. The chip is welded and tested on a printed circuit board (PCB) as shown in Fig. 10. An Agilent E4440A spectrum analyzer is used to measure the synthesizer parameters, and the relevant results are summarized in Table 1.

Table 1. Measured synthesizer parameters.

Parameter	Result
Technology	0.18 μm CMOS
Supply voltage	1.8 V
Output frequency	1.05–1.30 GHz
Phase noise	–98.53 dBc/Hz @ 100 kHz –121.92 dBc/Hz @ 1 MHz
Reference frequency	2 MHz
Reference spurs	–68 dB
Power diss. (without buffer)	9.8 mW
Receiver chip area	2.4 × 1.6 mm^2

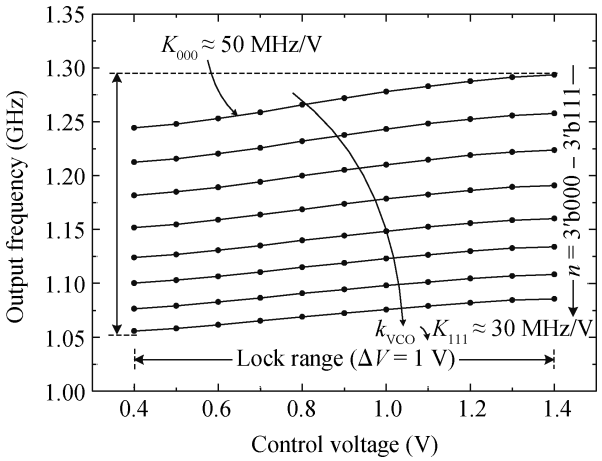

Fig. 11. Measured tuning characteristic of the synthesizer.

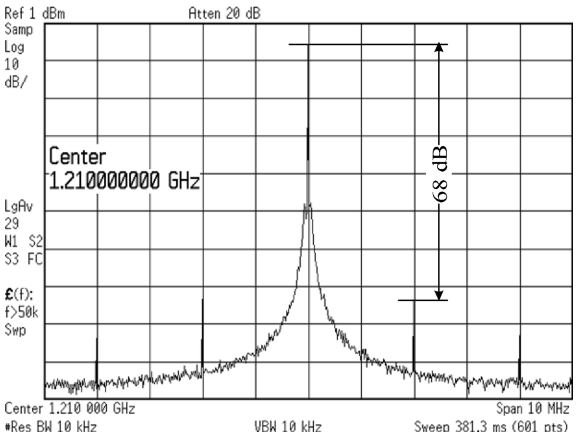

Fig. 12. Measured synthesizer output spectrum.

The frequency tuning characteristics of the proposed synthesizer are shown in Fig. 11, in which the range of output frequency is from 1.05 to 1.30 GHz. Based on the proposed VCO, the tuning sensitivity of the synthesizer is decreased, especially over the lock range from 0.4 to 1.4 V decided by our charge pump. The relevant gain of the frequency tuning curve is from 50 to 30 MHz/V when the digital code n is changed from 3'b000 to 3'b111.

Figure 12 depicts the measured synthesizer output frequency spectrum at 1.21 GHz, and the reference spurs are approximately –68 dB below the center frequency. The measured phase noise of 1.21 GHz LO frequency is –98.53 dBc/Hz at

Table 2. Comparison with other frequency synthesizers.

Reference	Ref. [2]	Ref. [5]	Ref. [6]	Ref. [8]	Ref. [22]	Ref. [23]	This work
Technology (μm)	0.25 CMOS	0.35 CMOS	0.6 CMOS	0.18 CMOS	0.13 CMOS	0.18 CMOS	0.18 CMOS
Tuning range (GHz)	5.14–5.70	1.31–1.88	1.675–1.795	5.15–5.35	3.96	5.45–5.65	1.05–1.30
Phase noise @ 1 MHz (dBc/Hz)	–110	–122	–118	–104	–113	–111	–121.92
Reference freq (MHz)	10	4.9	20	4	44	11	2
Spurs (dBc)	–70 @ 10 MHz	–60 @ 1 MHz	–70 @ 2.5 MHz	–40 @ 4 MHz	–68.8 @ 44 MHz	–80 @ 11 MHz	–68 @ 2 MHz
Power (mW)	13.5	57	52	18	15.6	27.5	9.8
Supply (V)	2.5	3	3.3	1.8	1.2	1	1.8

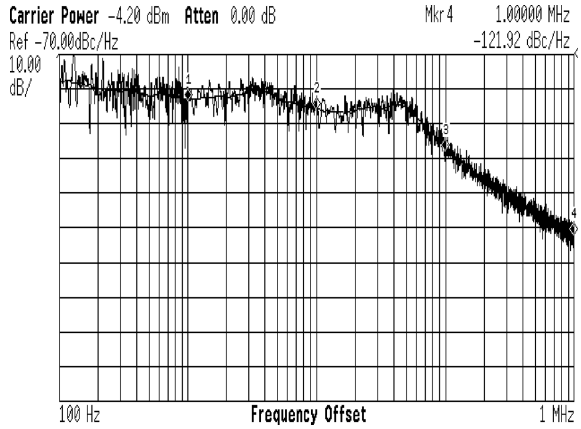

Fig. 13. Measured synthesizer phase noise.

100-kHz offset and –121.92 dBc/Hz at 1-MHz offset, as shown in Fig. 13.

The performance of the implemented frequency synthesizer is compared with other recently published frequency synthesizers in Table 2. As a result, based on the proposed LC-VCO, quadrature divider and other circuits, our frequency synthesizer achieves better phase noise and spurs performance, and the power consumption is far lower than others that are fabricated by similar standard CMOS technology.

5. Conclusion

In this paper, a 1.2 GHz frequency synthesizer integrated in a Beidou RF receiver has been presented in standard 0.18 μm CMOS technology, and the area of the RF receiver chip is 2.4×1.6 mm^2, including the pad. The LC-VCO employed in the frequency synthesizer can achieve optimized phase-noise performance, so as to relax the requirements for the other integrated components and their calibration of the frequency synthesizer. A high-speed and low-switching-noise divider-by-2 circuit based on a SCL structure is adopted to generate a quadrature (I/Q) LO signal. A high speed 8/9 DMP, a programmable-delay PFD without dead-zone defection, and a programmable-current CP are also integrated in our frequency synthesizer. The frequency synthesizer achieves an output range of 1.05–1.30 GHz, and the phase noise is –98.53 dBc/Hz at 100-kHz offset and –121.92 dBc/Hz at 1-MHz offset from the carrier frequency of 1.21 GHz. The power dissipation of core circuits without the output buffer is 9.8 mW from a 1.8 V power supply.

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