A current mode feed-forward gain control system for a 0.8 V CMOS hearing aid*

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Abstract: A current mode feed-forward gain control (CMFGC) technique is presented, which is applied in the front-end system of a hearing aid chip. Compared with conventional automatic gain control (AGC), CMFGC significantly improves the total harmonic distortion (THD) by digital gain control. To attain the digital gain control codes according to the extremely weak output signal from the microphone, a rectifier and a state controller implemented in current mode are proposed. A prototype chip has been designed based on a 0.13 μm standard CMOS process. The measurement results show that the supply voltage can be as low as 0.6 V. And with the 0.8 V supply voltage, the THD is improved and below 0.06% (–64 dB) at the output level of 500 $mV_{p\text{-}p}$, yet the power consumption is limited to 40 μW. In addition, the input referred noise is only 4 μV_{rms} and the maximum gain is maintained at 33 dB.

Key words: current mode; gain control; hearing aid
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1. Introduction

For patients with hearing impairment, the automatic gain control (AGC) in the analog front-end of a hearing aid system is necessary to adjust the microphone output signal within a desired range. Figure 1 shows the relationship between the input sound signal and output voltage signal of the microphone. Usually, a normal sound level in daily life ranges from 30 to 70 dB sound pressure level (SPL), denoted as range 1 in Fig. 1. Within range 1, a high-gain analog front end is required to amplify the quite weak signal. While the sound level is beyond 70 dB SPL, i.e. from range 2 to range 8, in Fig. 1, the gain of the front-end needs to be damped proportionally in the logarithmic scale for the sake of safe sound reception[1].

Conventionally, there are two approaches to realizing AGC with low power consumption. The first is to vary the transconductance of the closed (series–series feedback) or open-loop operational amplifier (op-amp)[2−4]. The second method is to adjust the shunt–shunt feedback coefficient of the operational transconductance amplifier (OTA) by adopting the MOS resistive circuit (MRC)[5, 6]. However, the total harmonic distortion (THD) in such designs usually degrades considerably with the output swing increased. As reported in Refs. [2–6], the THD higher than –46 dB is measured for the output swing equal to 500 $mV_{p\text{-}p}$.

For better sound amplification quality, the industry is trying to achieve a significant improvement in THD while maintaining low power. However, for a conventional analog AGC, it would be difficult to achieve low THD at the same time with low power consumption and high gain. For example, in an AGC[2−4], the way to minimize THD is usually by increasing the op-amp transconductance, yet at the cost of the extra power required. Although lower power and higher gain may be optimized by employing an MRC feedback network[5, 6], the distortion is inevitably brought in by the MRC network.

In order to minimize the distortion contributed by the feedback network[5, 6], we present a current mode feed-forward gain control (CMFGC) technique for the front end system. In detail, the system with the CMFGC technique is described, and the circuits with the current mode technique are described.

2. The system with the CMFGC technique

The CMFGC technique is characterized by the use of current mode circuits to obtain digital gain control codes according to the extremely weak output signal from the microphone. With the gain control codes, the gain of the system can be automatically changed with the sound level range varying. According to the sound level ranges and the output voltage characteristic of the microphone shown in Fig. 1, the proposed front end system with the CMFGC technique is illustrated in Fig. 2.

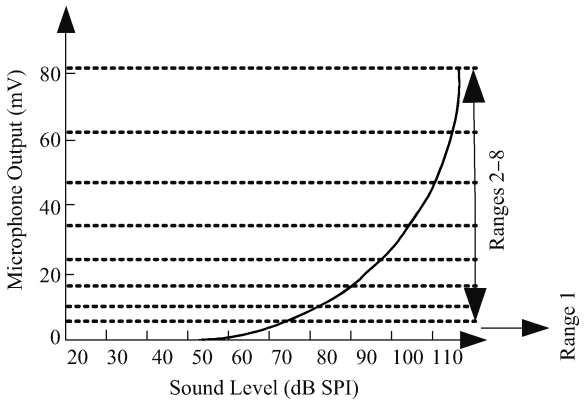

Fig. 1. Characteristics of the microphone for the hearing aid.

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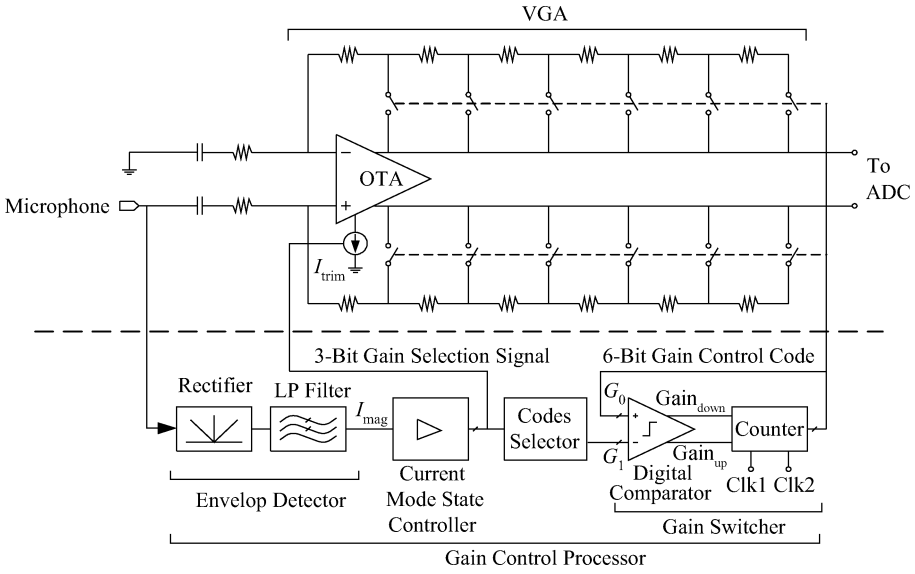


Fig. 2. Proposed front-end system with the CMFGC techinque.

The topology is divided into two parts: the VGA (variable gain amplifier) and the gain control processor.

2.1. VGA

The VGA includes the bias current trimming OTA[7], and the feedback network is formed by the resistor taps and complementary MOS switches. The gain of the VGA is determined by the number of resistors that are connected into the feedback loop, while the switches are controlled by digital control codes.

To examine the THD of the VGA, since the outputs of the system are differential, assuming $V_{\text{in}}(t) = V_{\text{in}}\cos\,\omega t$, the approximate transfer function of the VGA should be expressed as

$$V_{\text{out}}(t) = [V_{\text{out-ideal}} + 3(A_1 + A_2)V_{\text{in}}^3/4]\cos\omega t + [(A_1 + A_2)V_{\text{in}}^3\cos 3\omega t]/4, \quad (1)$$

where V_{in} is the amplitude of the input signal, $V_{\text{out-ideal}}$ is the amplitude of the output signal without the distortion, and $V_{\text{out}}(t)$ is the output signals of the VGA; coefficient A_1 is contributed by the non-ideality of the OTA and A_2 is contributed by the mismatch of the resistor array. Hence, the THD is given by

$$\text{THD} = \frac{\left(A_1 V_{\text{in}}^3/4 + A_2 V_{\text{in}}^3/4\right)^2}{\left(V_{\text{out}} + 3A_1 V_{\text{in}}^3/4 + 3A_2 V_{\text{in}}^3/4\right)^2}. \quad (2)$$

The A_1 contribution to the THD can be reduced to below –65 dB through the high open loop gain of the OTA[8]. As long as the resistor array is well matched, A_2's value should be limited to an extremely small value. Compared with other approaches[2–6], the THD of the CMFGC system could be improved by almost 20 dB. For the system operating with the extremely low supply voltage, the transistors in the OTA should be biased in the sub-threshold region except for the current sources. To optimize the noise of the system, a large gate area and large W/L ratio ($W/L = 3600\ \mu$m/2 μm) are adopted in the OTA PMOS input transistors, which can minimize the flicker noise and increase trans-conductance of the input stage.

2.2. Gain control processor

In order to obtain the digital gain control codes of the VGA according to the microphone's weak output signal, a current mode gain control processor is introduced, as shown in Fig. 2. This detects the input signal strength, and automatically chooses the proper gain by generating the gain control codes.

The current mode gain control processor is divided into four parts: the envelope detector, the current mode state controller, the decoder, and the gain switcher. A rectifier and an envelope filter constitute the envelope detector, which can output current signal I_{mag} reflecting the strength of the microphone input. The output of the envelope detector I_{mag} is then digitized by the current mode state controller, according to the 8 sound level ranges shown in Fig. 1. The digital signal from the state controller trims the OTA bias current I_{trim} to enhance the power efficiency. At the same time, the digital signal chooses new gain control codes in the gain control codes selector. Then the gain switcher is used to switch the original gain control codes to the new ones.

As the analog component of the gain control processor, the envelope detector and the state controller consume most of the power. To minimize the processor's power, tens of nA of bias current in the envelope detector is applied. In order to improve the sensitivity of the gain control processor under the low supply voltage, the envelope detector and the state controller are implemented by the current-mode. Since the attack and release time[9] is mainly determined by the corner frequency of the current mode envelope filter[10, 11], the corner frequencies of 15 and 3 Hz in the envelope filter are selected to set the attack and release time as 20 and 100 ms.

3. Circuits with the current mode technique

Since the microphone output voltage signal is weak, the gain control processor's sensitivity mainly depends on the cur-

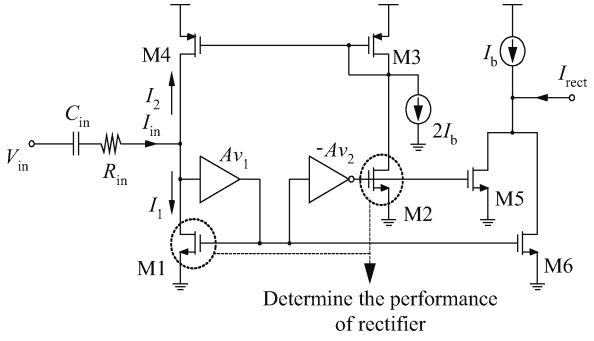
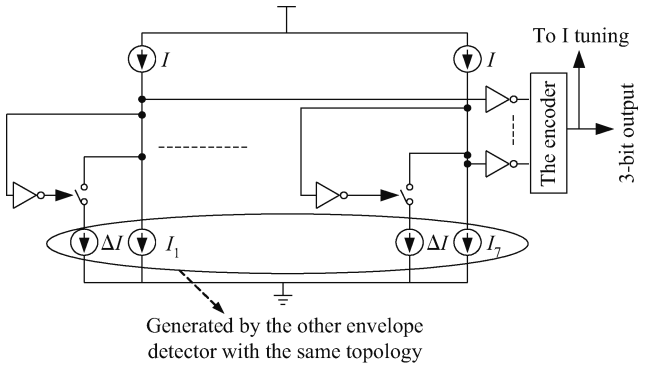
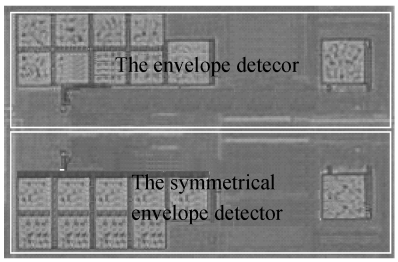


Fig. 3. The current mode full-wave rectifier.



(a)



(b)

Fig. 4. (a) Architecture of the current mode state controller. (b) The two envelope detectors on the chip.

rent mode rectifier and the current mode state controller, which are proposed and analyzed as follows.

3.1. The current mode rectifier

The rectifier shown in Fig. 3 is a full-wave rectifier, which is used to minimize the ripple of the output of the envelope detector. In Fig. 3, $I_{\rm in}$ is the input current transformed from the input voltage $V_{\rm in}$ by the resistor $R_{\rm in}$, and $I_{\rm rect}$ is the full-wave rectified output current. Amplifier Av_1 forms a feedback of the transistor M1 with the purpose of decreasing the input resistance, and M2 and M5 are biased in the cut-off region because of the amplifier Av_2.

The linearity of the envelope detector mainly depends on the full-wave rectification of the rectifier. Assuming the $I_{\rm in}$ is split into I_1 and I_2, as shown in Fig. 3, the rectifier works as follows.

When $I_{\rm in}$ flows into the rectifier, the gate voltage of M1 thus increases. This results in a much greater decrease in the gate voltage of M2. This will make M2 even more cut-off. As a result, I_2 can be ignored, and the whole of $I_{\rm in}$ flows through M1. $I_{\rm in}$ then will be mirrored to M6 and causes the change in $I_{\rm rect}$. So $I_{\rm rect}$ is equal to $I_{\rm in}$ when $I_{\rm in}$ flows into the rectifier.

In contrast, when $I_{\rm in}$ flows out of the rectifier, M2 will open up, letting the closed-loop (formed by M1–M4) work properly. Because the dimensions of the transistors M3 and M4 are set to be equal, the ratio between I_1 and I_2 thus equals

$$\frac{I_2}{I_1} = \frac{g_{\rm m2}\,(W/L)_4}{g_{\rm m1}\,(W/L)_3} Av_2 = \frac{g_{\rm m2}}{g_{\rm m1}} Av_2, \tag{3}$$

where $g_{\rm m1,2}$ is the transconductance of M1,2. In order to maximize the ratio, the M1 needs to be biased with an extremely low current to reduce $g_{\rm m1}$. The implication of the ratio is that when the $I_{\rm in}$ increases, the ratio I_2/I_1 will be augmented with the $g_{\rm m2}$ increasing. Eventually almost all of the $I_{\rm in}$ flows along the M4, and it will be mirrored through M3, M2 and M5, and causes the counter change of $I_{\rm in}$. Because $Av_2 \gg 1$, when the $g_{\rm m2}$ is the same as the $g_{\rm m1}$, it can be concluded that

$$I_{\rm M2} = -I_2 \approx -I_{\rm in}, \tag{4}$$

$$I_{\rm rect} = -I_2 \approx -I_{\rm in}, \tag{5}$$

where the $I_{\rm M2}$ is the current of M2. Thus, the minimum $V_{\rm in}$, which determines the envelope detector linearity range, is limited by the transconductance of M2 during its negative half of a cycle. Because the dimensions of the transistors M1 and M2 are set to be uniform, the currents of M1 and M2 are the same when the $g_{\rm m2}$ is equal to $g_{\rm m1}$. So the minimum $V_{\rm in}$, which makes the $g_{\rm m2}$ equivalent to the $g_{\rm m1}$, can thus be calculated as

$$V_{\text{in-min}} = I_{\text{bias-M1}} R_{\rm in}, \tag{6}$$

where $I_{\text{bias-M1}}$ is the biased current of M1. Because the Av_2 is designed to be 33 dB, the $V_{\text{in-min}}$ is much lower than the value that we calculate. Thus, in order to design the minimum $V_{\rm in}$ to be much less than 1 mV, $I_{\text{bias-M1}}$ is chosen to be 40 nA and $R_{\rm in}$ is designed to be 25 kΩ.

Such a rectifier can operate under a low supply voltage. With the simplest architecture of amplifier[12, 13] applied in the amplifier Av_1 and Av_2, the minimum power supply can be as low as

$$V_{\rm dd,\,min} = V_{\rm gs,\,PMOS} + V_{\rm gs,\,NMOS} - V_{\rm th,\,NMOS}. \tag{7}$$

Our design is based on the Chartered 0.13 μm standard CMOS process, and its typical threshold voltages of PMOS and NMOS are equal to 400 mV and 300 mV, respectively. For the maximum $V_{\rm in}$ of the linearity range to be 100 mV with the supply voltage 0.6 V, the over-drive voltage of NMOS and PMOS transistors in the circuit is designed to be as low as 10 mV.

3.2. The current mode state controller

Figure 4(a) illustrates the topology of the current mode state controller: it comprises seven current mode comparators and an encoder. The current mode comparators compare the output current of the envelope detector I with the different reference currents $I_{1\text{-}7}$. The reference currents are generated by

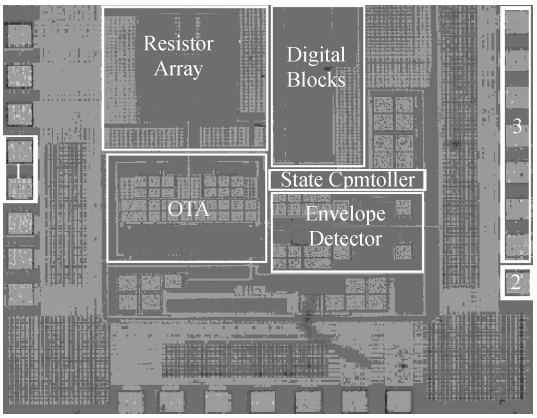


Fig. 5. Microscope photography of the CMFGC chip.

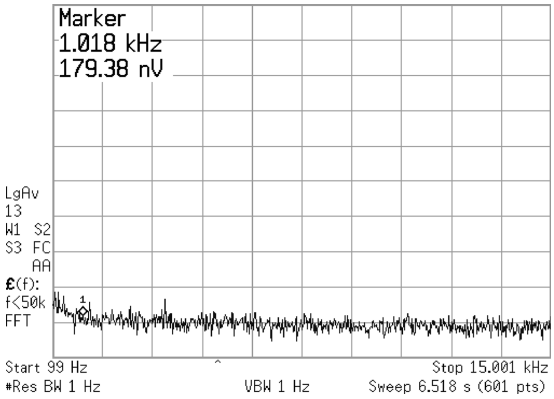


Fig. 6. Output noise of the CMFGC.

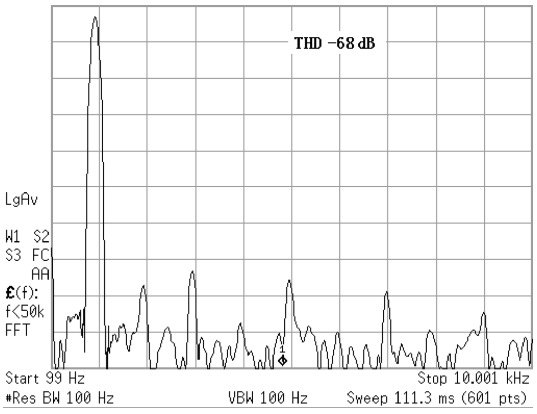


Fig. 7. Measured THD at maximum gain.

another envelope detector with the same topology without the input signal, and the two envelope detectors are placed symmetrically on the chip to minimize the mismatch, shown in Fig. 4(b). Hence, the current mode state controller can correctly determine the range of the sound level, regardless of the PVT's influence on the controller.

The hysteretic current ΔI is introduced to erase the possibility of oscillation at the threshold of the comparator, so the patient's listening intelligence can be preserved. And the hysteretic current ΔI is also obtained from the other envelope detector, as the reference currents $I_{1\text{-}7}$ are.

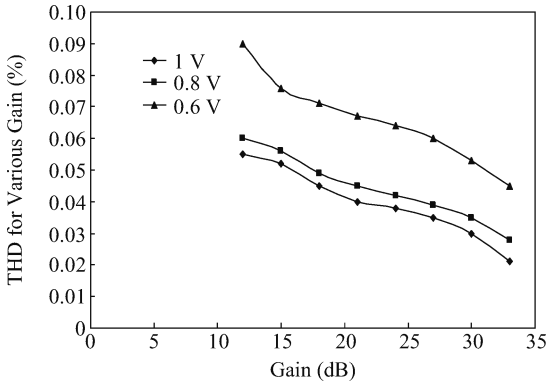


Fig. 8. Measured THD under various gains.

The 3 bit output would be achieved through the encoder, whose function is to encode the digital outputs from the parallel comparators. At the same time, the digital outputs are transferred to be used as the tuner of the OTA's bias current. Because the output signal of the envelope detector's frequency range is near DC, the current mode state controller dissipates little power during operation.

4. Measurement results and discussion

The proposed design was fabricated by a chartered 0.13 μm standard CMOS process and the chip occupies 2 × 1.8 mm^2 silicon areas, as shown in Fig. 5. The pads 1 are for the test of the system output signals, while the pads 2 and 3 are for the measurement of the envelope detector and the state controller, respectively. The system input voltage is a sinusoid signal at a typical audio frequency (1-kHz). The measurement results are summarized as follows.

4.1. VGA

The output noise of the system is about 180 nV/$\sqrt{\text{Hz}}$ with 12 dB gain of the system, as shown in Fig. 6. So the input referred noise in the audio frequency bandwidth (100–10 kHz) is about 4 μVrms.

Under a 0.8 V supply voltage, the total harmonic distortion with a gain of 33 dB at the output voltage 500 $mV_{p\text{-}p}$ is measured. The measured total harmonic distortion reaches –68 dB, as shown in Fig. 7. Under 1 V, 0.8 V and 0.6 V supply voltages, the measured total harmonic distortion (THD) against various gains at a 500 $mV_{p\text{-}p}$ output voltage is plotted in Fig. 8.

As shown in Fig. 8, under a 0.8 V supply voltage, when the gain reaches the minimum, the maximum THD (0.06%) occurs. In contrast, the THD under the maximum gain reaches the minimum (0.03%). The phenomenon may attribute to the varied output impedance that sources or sinks the current from the OTA. On the other hand, the THD improves for supply voltages increasing from 0.6 to 1 V.

The relationship between the power consumption and the gain under 1 V, 0.8 V and 0.6 V supply voltages is shown in Fig. 9. Since a current trimming OTA is employed in the system, the power dissipation of the system reaches its maximum of 35–45 μW with the highest gain of 33 dB, and minimum of 25–35 μW with the lowest gain of 12 dB.

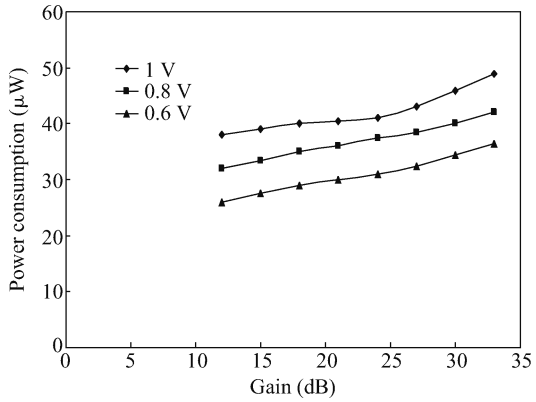


Fig. 9. Power dissipation at various gains.

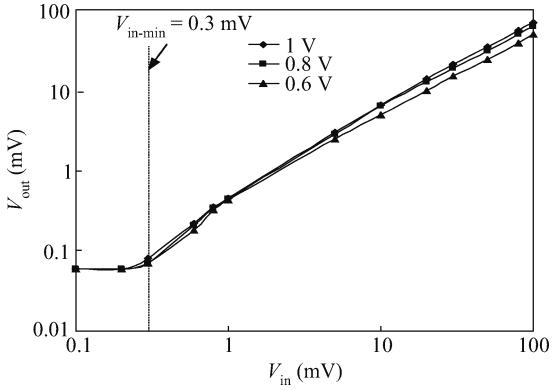


Fig. 10. The measured envelope detector characteristics.

4.2. Gain control processor

In order to measure the characteristics of the envelope detector, the output current of the envelope detector is transformed to voltage by the resistor equal to R_{in}. Figure 10 shows experimentally measured envelope detector characteristics for input signal amplitudes ranging over the entire sound level of operation under 1 V, 0.8 V and 0.6 V supply voltages. It reveals that the envelope detector provides proportional and linear information about the input signal envelope over 0.3–100 mV at a 0.6 to 1 V supply voltage. Due to the input voltage resolution of the rectifier that we set, the plot flattens out at approximately V_{in} = 0.3 mV on the low end.

For the 8 ranges of the sound level to be correctly determined, the comparison error of the state controller is measured under a 0.6 V supply voltage. Judging from Fig. 1, the least-significant bit (LSB) of the microphone output voltage is chosen to be 4 mV. Figure 11 shows that the measured differential error and integral error of the state controller are in the range of –0.07/0.09 LSB and 0.01/0.1 LSB, respectively. This illustrates that the state controller functions well.

With the gain step of 3 dB between range 1 and range 8 (33–12 dB), the steady input-output characteristics of the system and the THD of the output signal under 0.8 V supply voltage are shown in Fig. 12. In range 1, the THD is below –70 dB, which illustrates the high performance of the system in the normal sound level. While in ranges 2–8, the amplitude of the

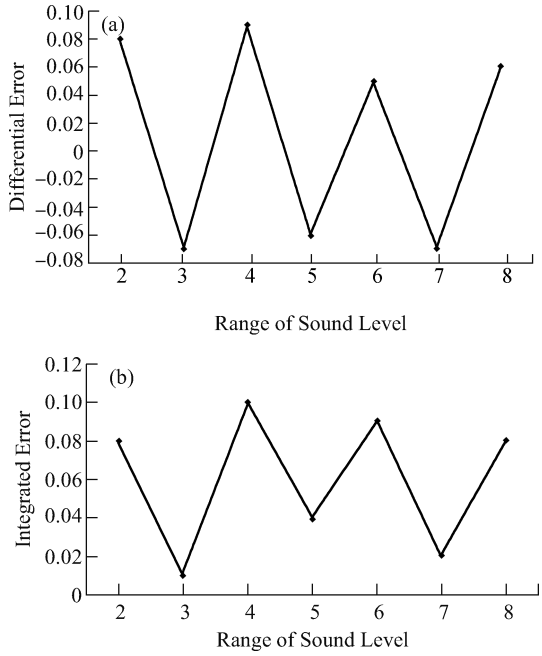


Fig. 11. Measured result of the state controller. (a) Differential error of the controller. (b) Integrated error of the controller.

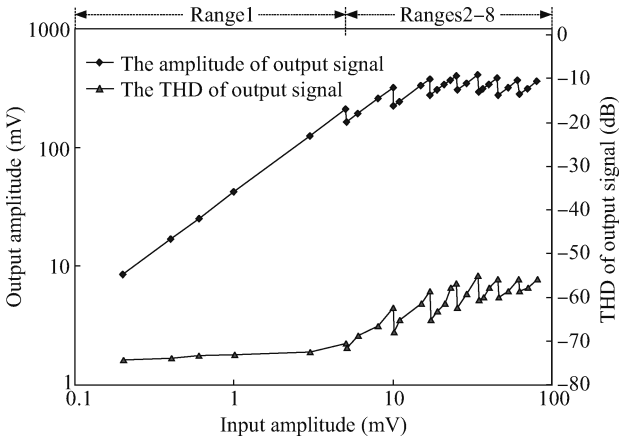


Fig. 12. Measured input–output characteristics and the THD of the output signal.

output signal is limited within 400 mV (800 $mV_{p\text{-}p}$) and satisfies the comfort ability of the patients, so the hearing ability of the patients can be protected. Moreover, the THD is maintained below –55 dB. Thus the dynamic range of the input signal is extended.

The transient output response behavior is measured with the input amplitude transferring between range 1 and range 8. The transient behavior shows the attack time equal to approximately 20 ms to ensure fast protection against overshoots, and the release time is up to approximately 100 ms to preserve speech intelligibility[15], as shown in Fig. 13.

4.3. Comparison

For comparison with other AGCs, the figure of merit (FOM) is adopted to evaluate the parameters of power, gain,

Table 1. Comparison with other AGCs.

Reference	Supply voltage (V)	THD (%)	Input referred noise (min) (μVrms)	Gain (MAX) (dB)/ BW (kHz)	Power (μW)	FOM
JSSC2006[3]	2.8	1 (@ 520 mV_{p-p}) @ 19 dB gain	54	22/9.6	34	0.2 (520 mV_{p-p})
CDS2005[4]	1	0.6 (500 mV_{p-p}) @ 30 dB gain	2	40 /10	60	13 (500 mV_{p-p})
ICECS2008[8]	1	0.7 (400 mV_{p-p}) @ 40 dB gain	2.2	40/10	100	6 (500 mV_{p-p})
This work	0.8	< 0.06 (500 mV_{p-p}) @ > 12 dB gain	4	33/9.8	40	34 (500 mV_{p-p})

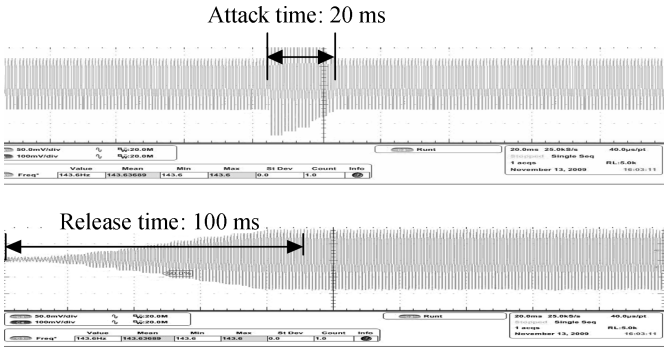


Fig. 13. Measured CMFGC transient output with the input change between the range 1 and range 8 for the attack time and release time characteristic. Time scale: 20 ms/div.

THD, and the input referred noise. For the interrelationship between the parameters discussed in the introduction, FOM is defined as

$$\mathrm{FOM} = \frac{\mathrm{Gain} \times \mathrm{BW}}{\mathrm{Power} \times \mathrm{THD} \times \mathrm{Noise}}. \quad (8)$$

The system's performances compared with other analog feedback AGCs[3, 4, 8] are summarized in Table 1. From the table, we can see that the FOM of this work is improved significantly.

5. Conclusion

This paper has demonstrated a tens of microwatt front-end system with the CMFGC technique for a hearing aid chip. By digital gain control codes, the system with the technique has achieved a much lower THD compared with other approaches. In addition, low noise and low power consumption have been realized. We have also confirmed that the current mode rectifier and the state controller are useful in obtaining the codes. Hence, the advantages of the system have been achieved on a chip.

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