A 8.75–11.2-GHz, low phase noise fractional-N synthesizer for 802.11a/b/g zero-IF transceiver*

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Abstract: An ultra broadband fractional-N frequency synthesizer for 802.11a/b/g zero-IF transceiver application is presented. The mathematical models for the behavior of the synthesizer's spur and phase noise are analyzed, and the optimization methodology is proposed. Measurement results exhibits that the frequency synthesizer's integrated phase noise is less than 1° (1 kHz to 100 MHz) with a 4.375 GHz carrier (after divide-by-2), and the reference frequency spur is below –60 dBc operating with a 33 MHz reference clock. The frequency synthesizer is fabricated on a standard 0.13 μm RF CMOS process and consumes 39.6 mW from a 1.2 V supply voltage.

Key words: frequency synthesizer; VCO, phase frequency detector; sigma–delta modulator; charge pump
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1. Introduction

Frequency synthesizer (FS) is ubiquitous building block which is widely used in modern radio frequency (RF) communication system. Existing FS can be categorized into two groups: Integer-N and fractional-N (Frac-N) synthesizer. Compared to the integer one, the Frac-N synthesizer has the characteristic that frequency precision is free from integer ratio of input reference frequency. For a multimode system, Frac-N synthesizer is a good choice. Previous work has shown that many effective method to lower the phase noise and spur of the Frac-N synthesizer[1−3]. In Refs. [1, 2], a compensation charge pump circuit's is adopted. In Ref. [3], three VCO is used to lower the phase noise. Unfortunately, these techniques still suffer from these limitations - large chip area, excessive power consumption.

In this paper, a low phase noise Frac-N FS for 802.11a/b/g zero-IF transceiver is described, which is able to cover the 2.4–2.48 GHz range (802.11b/g) and 5.15–5.35 GHz (802.11a band I). We proposed a lower phase noise and spur method without sacrificing the chip area and power; a single VCO is used to save area. The rest of paper is arranged as follows. Section 2 explains in detail the Frac-N FS spur and phase noise generation mechanism. Section 3 presents the optimized method and the detailed circuit implementation. Section 4 shows the chip test results and the conclusion are given in finally section.

2. System analysis

Figure 1 shows the block diagram of the Frac-N FS for 802.11a/b/g zero-IF transceiver. The frequency of the 802.11a is obtained by a divide-by-2 after VCO. A second divide-by-2 provides the orthogonal frequency for 802.11b/g transceiver. The phase noise and spur are two key figure of merit in 802.11a/b/g transceiver application. This section will introduce the mathematical models for the behavior of the synthesizer's spur and phase noise.

2.1. Sources of spur

In-band spur will affect the integrated phase noise of the synthesizer, out-band spur will interfere the adjacent channel signal to noise ratio. There are several sources that can cause spur in synthesizer system[4].

(1) Fractional spurs. The sigma–delta modulator (SDM) output controls the division modulus of the prescaler. The output frequency $f_{\rm div}$ and reference frequency $f_{\rm ref}$ are not equal in steady state, but the average output frequency output $\overline{f_{\rm div}}$ and $f_{\rm ref}$ are equal. The dynamic balance leads to possible spurious. Fractional spurs are usually located at the frequency offset $\left(\frac{M}{2^k}\right) f_{\rm ref}$, k is the number of bits of the SDM, M is the digital input of the modulator, the spur can be reduced by input a random "dithering" [5, 6].

(2) Reference spurs. Frac-N FS also exists reference spurs due to the modulation of the VCO control voltage by the reference clock, which locate at sidebands $\pm n f_{\rm ref}$ and its harmonics with respect to the carrier. The relative reference spur level to the carrier can be described as[6]

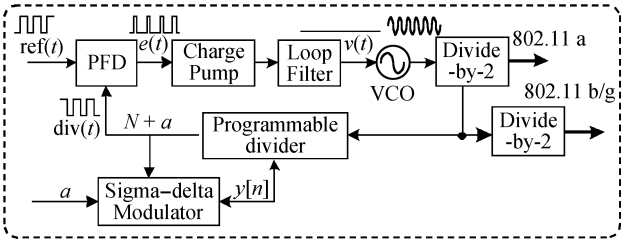

Fig. 1. Block diagram of the Frac-N FS for 802.11a/b/g.

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$$L(nf_{\rm ref}) = 20\lg\frac{I_\varepsilon Z_{\rm filt}(nf_{\rm ref})K_{\rm VCO}}{nf_{\rm ref}}, \quad (1)$$

where $K_{\rm VCO}$ is the gain of the VCO, $Z_{\rm LPF}(nf_{\rm ref})$ is the transfer function of the loop filter, and $f_{\rm ref}$ represents the reference clock. The maximum equivalent current mismatch I_ε results from leakage current $I_{\rm leak}$, current mismatch Δi in the CP and timing mismatch $\Delta T_{\rm mis}$ in the PFD, which is given by

$$I_\varepsilon = I_{\rm leak} + \Delta i\frac{\delta T_{\rm on}}{T_{\rm ref}} + I_{\rm cp}\frac{\delta T_{\rm rms} + \Delta T_{\rm mis}}{T_{\rm ref}},$$

where $\delta T_{\rm rms}$ is the root mean square (RMS) value of the time difference between the reference signal and the divided VCO signal, which is related to the type of SDM; $I_{\rm cp}$ is the nominal value of the CP current. The reference spur can be degraded by reducing $I_{\rm leak}$, $\Delta T_{\rm mis}$ and $\delta T_{\rm on}$. It is also helpful to reduce the value of $K_{\rm VCO}$.

2.2. Sources of noise

As shown in Fig. 1, the synthesizer consists of a crystal oscillator, a phase frequency detector, a charge pump with programmable output current, a multi-modulus divider, a SDM, a loop filter and a wideband voltage-controlled oscillator (VCO). These building blocks noise will directly affect the phase noise of the synthesizer. Phase noise power spectrum density (PSD) due to the individual building blocks of the synthesizer can be expressed by

$$\begin{aligned}\theta^{\rm out}_{\rm n,\,total}(f_{\rm m}) = {} & \theta^{\rm out}_{\rm n,\,REF}(f_{\rm m}) + \theta^{\rm out}_{\rm n,\,FIL}(f_{\rm m}) + \theta^{\rm out}_{\rm n,\,Div}(f_{\rm m}) \\ & + \theta^{\rm out}_{\rm n,\,VCO}(f_{\rm m}) + \theta^{\rm out}_{\rm n,\,CP}(f_{\rm m}) \\ & + \theta^{\rm out}_{\rm n,\,SDM}(f_{\rm m}) + \theta^{\rm out}_{\rm n,\,n}(f_{\rm m}), \end{aligned} \quad (2)$$

where $\theta^{\rm out}_{\rm n,\,REF}(f_{\rm m})$, $\theta^{\rm out}_{\rm n,\,FIL}(f_{\rm m})$, $\theta^{\rm out}_{\rm n,\,Div}(f_{\rm m})$, $\theta^{\rm out}_{\rm n,\,CP}(f_{\rm m})$, and $\theta^{\rm out}_{\rm n,\,SDM}(f_{\rm m})$ represent equivalent phase noise contributions due to each building block, $\theta^{\rm out}_{\rm n,\,n}(f_{\rm m})$ is the noise which is caused by nonlinearities of the PFD/CP, and $f_{\rm m}$ is the offset frequency. Following we will discuss the last four items noise contribution of the system.

(1) VCO noise. The equivalent output noise contributions of the VCO can be expressed as

$$\theta^{\rm out}_{\rm n,\,VCO}(f_{\rm m}) = \theta_{\rm n,\,VCO}(f_{\rm m})\left|\frac{1}{1 + H_{\rm o}(f_{\rm m})/N}\right|^2, \quad (3)$$

where $\theta_{\rm n,\,VCO}(f_{\rm m})$ is the VCO phase noise PSD, and $H_{\rm o}(f_{\rm m})$ is the synthesizer's open loop transfer function. In Eq. (3), VCO phase noise has high pass characteristic, which can be suppressed inside the loop band-width. A wide-band loop filter and low phase noise VCO are benefit for reducing noise contribution to synthesizer.

(2) Charge pump noise. The noise of CP does not always contribute to the output noise, only valid when the CP is on activated status. For Frac-N synthesizer, the CP's average activated time is $\delta T_{\rm rms} + \delta T_{\rm on}$, the second term is decided by the PFD and CP. The noise contribution of the CP can be approximately given by

$$\theta^{\rm out}_{\rm n,\,CP} = \left[(i^2_{\rm p,\,n} + i^2_{\rm n,\,n}) \circledast S_{\rm on}(f_{\rm m})\right]\left|\frac{H_{\rm o}(f_{\rm m})}{1 + H_{\rm o}(f_{\rm m})/N}\frac{2\pi}{I_{\rm cp}}\right|^2, \quad (4)$$

where $i^2_{\rm p,\,n}$ and $i^2_{\rm n,\,n}$ are represent the CP's PMOS and NMOS current power spectrum density (PSD), $\circledast$ is a convolution operator, $S_{\rm on}(f_{\rm m})$ is the Fourier function of the $\delta T_{\rm rms} + \delta T_{\rm on}$ at the spectrum and can be written as

$$S_{\rm on}(f_{\rm m}) = \sum_{+\infty}^{-\infty} a^2_{\rm n}\delta(f_{\rm m} - nf_{\rm o}), \quad (5)$$

where $nf_{\rm o}$ is the harmonic frequency, $a_{\rm n}$ is the Fourier coefficient and can be expressed as

$$a_{\rm n} = \frac{\sin[n\pi(\delta T_{\rm rms} + \delta T_{\rm on})/2T_{\rm ref}]}{n\pi}. \quad (6)$$

In Eq. (4), we can suppress the CP noise contribution by reducing $\delta T_{\rm on}$ and the CP noise. Moreover decreasing the loop bandwidth is another effective method.

(3) Sigma–delta quantization noise. For an mth-order MASH-type SDM, the quantization noise is given by[7]

$$\theta_{\rm n,\,SDM}(f_{\rm m}) = \frac{\pi^2\Delta^2}{3f_{\rm s}}\left(2\sin\frac{\pi f_{\rm m}}{f_{\rm s}}\right)^{2(L-1)}, \quad (7)$$

where L is the order of the modulator, $f_{\rm s}$ is the sample frequency, Δ is the minimum step size of the quantizer. The SDM quantization contributed to the noise of FS output signal can be expressed as

$$\theta^{\rm out}_{\rm n,\,SDM}(f_{\rm m}) = \theta_{\rm n,\,SDM}(f_{\rm m})\left|\frac{H_{\rm o}(f_{\rm m})}{1 + H_{\rm o}(f_{\rm m})/N}\right|^2. \quad (8)$$

The high frequency quantization noise of the SDM can be filtered as the loop filer has a low pass characteristic for this noise.

(4) Nonlinear noise. SDM high frequency quantization noise can be brought into the signal bandwidth through intermodulation caused by nonlinearities in the sub-block, results in a significant increase in-band phase noise floor. This has been reported previously in Refs. [8, 9]. In sigma–delta synthesizer, these nonlinearities mainly due to charge pump PFD characteristics.

When the synthesizer is on locked status, the output frequency $f_{\rm out}$ is fixed. But the frequency $f_{\rm div}$ is changing with the division ratio of the divider, which is difficult to align with the reference clock $f_{\rm ref}$, but the average of the $f_{\rm div}$ is aligned with the reference clock. Assume time difference between reference signal and the divided VCO signal at the kth-period is δT_k, and the corresponding charge and discharge current of the charge pump are $I_{\rm up}$ and $I_{\rm dn}$, respectively. The charge variation caused by CP charge and discharge current can be approximately as

$$\begin{aligned} Q_{\rm up,\,k} &= I_{\rm up}(\delta T_{\rm k} + \delta T_{\rm on}) + \frac{I_{\rm up}}{2}(\tau_{\rm f,\,up} - \tau_{\rm r,\,up}) + Q_{\Delta,\,\rm up} \\ Q_{\rm dn,\,k} &= I_{\rm dn}\delta T_{\rm on} + \frac{I_{\rm dn}}{2}(\tau_{\rm f,\,dn} - \tau_{\rm r,\,dn}) + Q_{\Delta,\,\rm dn}, \end{aligned} \quad (9)$$

or

$$Q_{\mathrm{up,k}} = I_{\mathrm{up}}\delta T_{\mathrm{on}} + \frac{I_{\mathrm{up}}}{2}(\tau_{\mathrm{f,up}} - \tau_{\mathrm{r,up}}) + Q_{\Delta,\mathrm{up}},$$
$$Q_{\mathrm{dn,k}} = I_{\mathrm{dn}}(\delta T_{\mathrm{k}} + \delta T_{\mathrm{on}}) + \frac{I_{\mathrm{dn}}}{2}(\tau_{\mathrm{f,dn}} - \tau_{\mathrm{r,dn}}) + Q_{\Delta,\mathrm{dn}}, \tag{10}$$

where $\tau_{\mathrm{f,up}}$ and $\tau_{\mathrm{r,up}}$ are the fall and rise time of the CP charge current, $\tau_{\mathrm{f,dn}}$ and $\tau_{\mathrm{r,dn}}$ are fall and rise times of the CP discharge current, $Q_{\Delta,\mathrm{up}}$ is the charge caused by clock feed-through, current leakage and charge sharing of the UP transistor, $Q_{\Delta,\mathrm{dn}}$ is the charge caused by clock feed-through, current leakage and charge sharing of the DN transistor. The net charge $Q_{\Delta,\mathrm{k}}$ delivered to the loop filter is

$$Q_{\Delta,\mathrm{k}} = |Q_{\mathrm{up,k}} - Q_{\mathrm{dn,k}}|. \tag{11}$$

Substituting Eqs. (9) and (10) to Eq. (11), assume $I_{\mathrm{up}} = I_{\mathrm{cp}}\left(1 + \frac{\varepsilon}{2}\right)$ and $I_{\mathrm{dn}} = I_{\mathrm{cp}}\left(1 - \frac{\varepsilon}{2}\right)$, the total net charge is:

$$\begin{aligned} Q_{\Delta,\mathrm{k}} = \Big| & \pm I_{\mathrm{cp}}\delta T_{\mathrm{k}} + \frac{\varepsilon}{2} I_{\mathrm{cp}}\,\delta T_{\mathrm{k}} + \frac{\varepsilon}{2} I_{\mathrm{cp}}\delta T_{\mathrm{on}} \\ & + (Q_{\Delta,\mathrm{up}} - Q_{\Delta,\mathrm{up}}) + \frac{I_{\mathrm{cp}}}{2}[(\tau_{\mathrm{f,up}} - \tau_{\mathrm{r,up}}) \\ & - (\tau_{\mathrm{f,dn}} - \tau_{\mathrm{r,dn}})] \\ & + \frac{\varepsilon}{4} I_{\mathrm{cp}}[(\tau_{\mathrm{f,up}} - \tau_{\mathrm{r,up}}) - (\tau_{\mathrm{f,dn}} - \tau_{\mathrm{r,dn}})]\Big|, \end{aligned} \tag{12}$$

where ε is relative mismatch between charge and discharge currents. The first term in Eq. (12) represents the desired charge; the second item represents the nonlinear item. the other items are constant item merely resulting in a DC offset, which can be eliminate by introducing a finite static phase error.

From Eq. (12), the nonlinearity is caused by the static mismatch of the charge pump. The input-referred phase error due to the nonlinearity is

$$i_{\mathrm{k,err}} = \frac{\partial Q_{\Delta,\mathrm{k}}}{\partial T} \approx \frac{Q_{\Delta,\mathrm{k}}}{T_{\mathrm{ref}}} = \frac{\varepsilon I_{\mathrm{cp}}\delta T_{\mathrm{k}}}{2T_{\mathrm{ref}}}. \tag{13}$$

For high-order SDM, the distribution of δT_{k} is approximately Gaussian with mean 0 (under lock). The noise power spectral density due to the nonlinearities will be[10]

$$\theta_{\mathrm{n,n}}(f_{\mathrm{m}}) = \frac{i_{\mathrm{k,err}}^2}{f_{\mathrm{ref}}}\left(1 - \frac{2}{\pi}\right), \tag{14}$$

and substituting Eq. (13) into Eq. (14), we get:

$$\theta_{\mathrm{n,n}}(f_{\mathrm{m}}) = \frac{(\varepsilon I_{\mathrm{cp}})^2}{f_{\mathrm{ref}}}\frac{\sigma_{\delta T_{\mathrm{k}}}^2}{(2T_{\mathrm{ref}})^2}\left(1 - \frac{2}{\pi}\right), \tag{15}$$

where $\sigma_{\delta T_{\mathrm{k}}}^2$ is the variance of δT_{k}. The CP current mismatch exhibits an approximately white noise PSD. The low frequency noise cannot be filtered as the loop filer has a low pass characteristic for this noise. So the in-band noise of the FS will be increased by the CP current mismatch.

From above analysis, any nonlinearity in the PLL building blocks, mainly in the PFD/CP IO characteristic, increases in-band noise and spurs; the VCO's phase noise increases out-band noise. Therefore, the effective way is decrease the CP current mismatch (dynamic and static) and the VCO's phase noise.

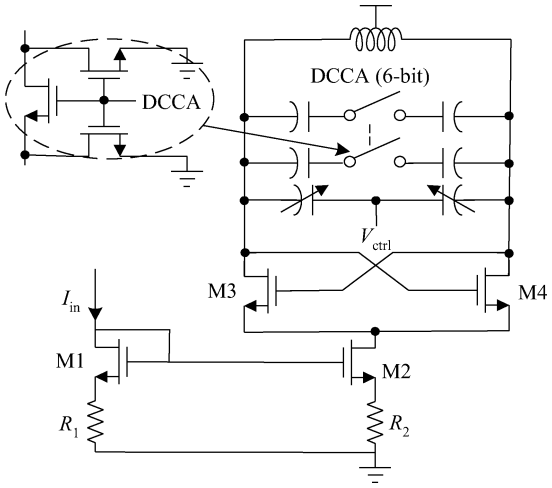

Fig. 2. Ultra wideband VCO.

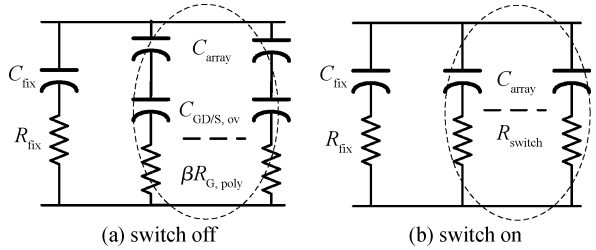

Fig. 3. (a) Capacitor array equivalent model (off). (b) Capacitor array equivalent model (on).

3. Circuit design

The synthesizer is designed for 802.11a/b/g zero-IF transceiver application, the synthesizer's frequency locking range from 9.6 (2.4–2.48 GHz for 802.11b/g) to 10.7 GHz (5.15–5.35 GHz for 802.11a band I) is required. 802.11a/b/g system imposes strict requirement on synthesizers phase noise and spur.

3.1. VCO

To cover this range with single VCO, while maintaining a small VCO gain, the VCO must feature several tuning curves, by using a 6-bit digital controlled capacitor array (DCCA). Figure 2 shows the VCO architecture. The cross-coupled negative transconductance cell (M3, M4) is used to compensate the losses in the LC tank, a resistor is used in the tail-current source to lower the noise of the VCO[11]. When the operating frequency is higher than 10 GHz, the nMOS cross coupled pair is normally used since nMOS transistor has larger g_{m} than pMOS transistor that has the same channel Length and Width.

When VCO works at the frequency of above 10 GHz, excepting the Q factor of the inductor, the parasitic capacitance's Q factor of the switch device will also affect the phase noise of the VCO. Figure 3 is the DCCA equivalent model. The Q factor of the capacitor is determined not only by Q factor of fixed capacitor but also Q factor of the DCCA. When the DCCA switches are all off, assuming $C_{\mathrm{array}} \gg C_{\mathrm{GD/S,\,ov}}$, the Q factor of the DCCA can be approximated as

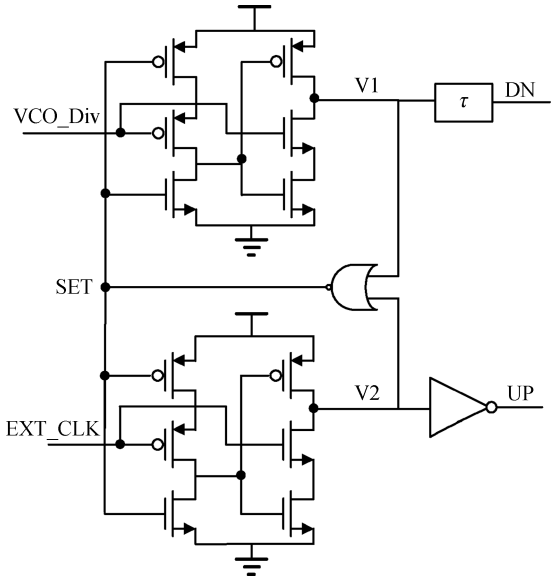

Fig. 4. Block diagram of the PFD.

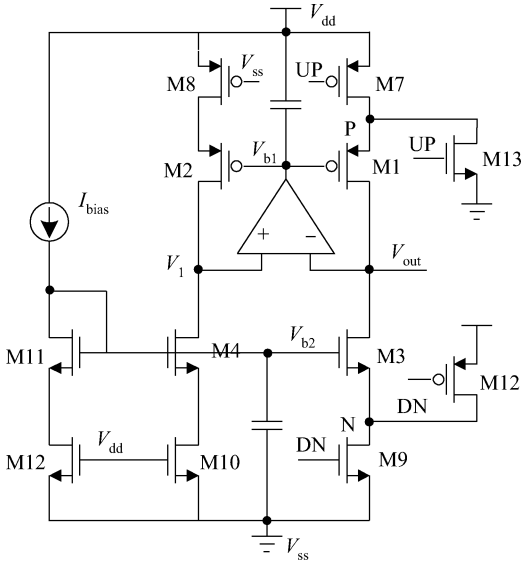

Fig. 5. Block diagram of the CP.

$$Q_{\mathrm{DCCA,off}} = \frac{1}{2\pi f N_{\mathrm{f}} W_{\mathrm{f}} L_{\mathrm{f}} C_{\mathrm{GD/S,ov}} (\beta R_{\mathrm{G,poly}} + R_{\mathrm{D,S}})}, \quad (16)$$

where W_{f} is the channel width per finger, N_{f} is the number of fingers; $C_{\mathrm{GD/S,ov}}$, $R_{\mathrm{D,S}}$ and $R_{\mathrm{G,ploy}}$ are the switch's drain/source overlap capacitance per unit width, the source/drain parasitic resistance and the poly resistance of the gate, and β is the scale factor. $R_{\mathrm{G,ploy}}$ can be expressed as[12]

$$R_{\mathrm{G,ploy}} = \frac{R_{\mathrm{G,sh}}}{N_{\mathrm{f}} L_{\mathrm{f}}} \left(W_{\mathrm{ext}} + \frac{W_{\mathrm{f}}}{\alpha} \right), \quad (17)$$

where $R_{\mathrm{G,sh}}$ is the gate sheet resistance, L_{f} is the channel length, and W_{ext} is the extension of the poly-silicon gate over the active region. α is the factor, which is dependent on the layout structure, and $\alpha < 1$. Substituting Eq. (18) into Eq. (17) and omitting W_{ext} and R_{DS}, Equation (17) can be simplified as

$$Q_{\mathrm{DCCA,off}} = \frac{\alpha}{2\pi f \beta C_{\mathrm{GD/S,ov}} R_{\mathrm{G,sh}}} \frac{L_{\mathrm{f}}}{(W_{\mathrm{f}})^2}. \quad (18)$$

When the DCCA switches are all on, the Q factor of the capacitor can be approximated as

$$Q_{\mathrm{DCCA,on}} = \frac{\mu_{\mathrm{n}} C_{\mathrm{ox}} (V_{\mathrm{GS}} - V_{\mathrm{t}})}{\pi f C_{\mathrm{array}}} \frac{N_{\mathrm{f}} W_{\mathrm{f}}}{L_{\mathrm{f}}}, \quad (19)$$

where C_{array} is the capacitance of the capacitor array. To ensure $\frac{N_{\mathrm{f}} W_{\mathrm{f}}}{L_{\mathrm{f}}}$ at a certain value for the condition, decreasing the value of W_{f} is useful to improve the value of $Q_{\mathrm{DCCA,off}}$. However, too short W_{f} will increase the parasitic capacitance, which is adverse to lowering the phase noise of the VCO. So we should make a trade-off between the finger number and the width value of the per-finger.

3.2. PFD and CP

From Eqs. (1), (4) and (15), the CP and PFD circuits are the main sources of spurs and in-band noise. Reduction of the current mismatch (dynamic and static) of the CP is the most effective way to lower phase noise and spur of the synthesizer. For an ideal CP, the transfer curve of the output charge versus phase error is linear, but in fact the curve deviates from the ideal transfer curve. Whatever error remains in the charge pump output will impact the performance of the Frac-N FS.

According to Eq. (4), the short turn-on time contributes to reducing the phase noise of the CP. Figure 4 shows a high speed dynamic PFD[13]; the reset time is less than 200 ps. The PFD compares the phase and frequency between the reference signal and the feedback signal to generate an up or down signal to the CP.

Figure 5 is a block diagram of the perfect current matching CP[14]; M13 and M12 transistors are used to reduce dynamic response timing and charge injection of the CP. A rail-to-rail error amplifier in a feedback loop actively maintains the voltage V_1 equal to V_{out}, and the up current equal to down current in a wide range of the V_{out}. The mismatch of static current is less than 0.5% when the V_{out}, voltage is between 0.3–0.9 V. In order to reduce the clock feed-through and charge injection, the switch is not directly connected to the output. A delay unit in the PFD is used to eliminate the UP and DN signal timing mismatch.

3.3. Divider

Figure 6 shows the divider's block diagram. The frequency divider is composed of a 7.5/8 prescaler, a programmable counter, a 5-bit P counter and a 4-bit S counter. If the prescaler's control signal is set to "1", the division "8" will be selected. The P and the S counters divide the output signal frequency of the prescaler simultaneously. Note that the content of P must be larger than that of S. According to Eq. (8), a 7.5/8 prescaler is selected to reduce the quantization noise of the SDM.

Table 1. Performance summary and comparison.

	ISSCC[1]	JSCC[15]	RFIC[16]	This work
Technology (μm)	0.25 BiCMOS	0.18 CMOS	0.35 SiGe	0.13 CMOS
Power consumption (mW)	23.8	34	17	39.6
Ref. freq. (MHz)	25	20	1	33
Output frequency (GHz)	4.9	10	6	4.375
Phase noise @ 1 MHz (dBC/Hz)	NA	–102	–110	< -114
Ref. spur (dBc)	–68	< -48	< -65	< -60
Frequency range (GHz)	2.4–2.555, 4.18–6.12	8.67–10.12	5.5–6.4	8.75–11.2
Supply voltage (V)	2.5	1.8	2.2	1.2

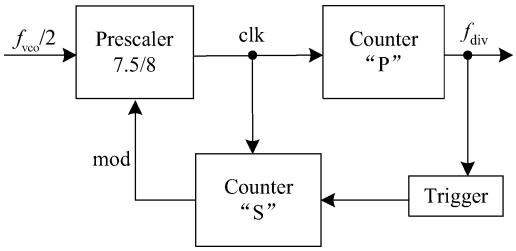

Fig. 6. Block diagram of the divider.

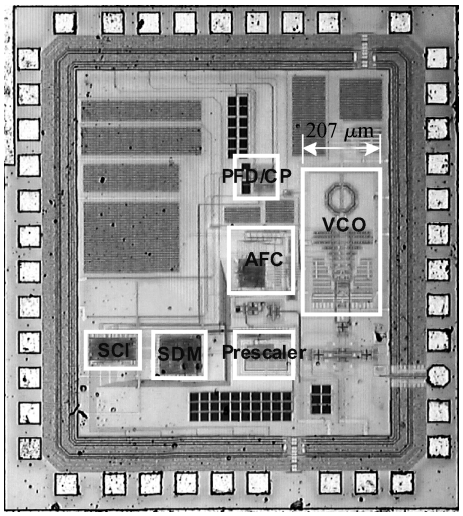

Fig. 7. Chip microphotograph.

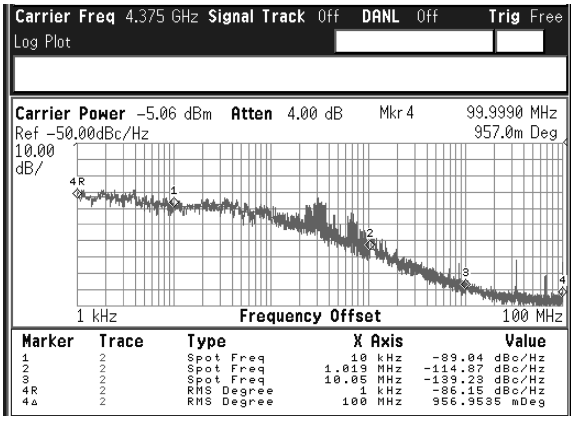

Fig. 8. The measured FS phase noise at 4.375 GHz.

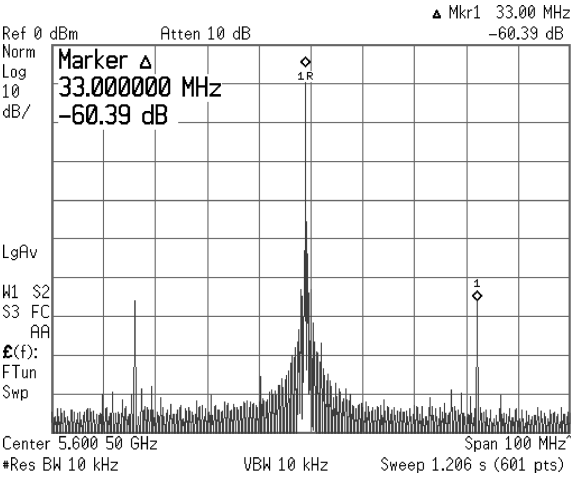

Fig. 9. The measured FS output spectrum at 5.6 GHz.

3.4. Sigma–delta modulator

For a high-order SDM, the spurious energy is whitened and shaped to high-frequency noise, which can be removed by low-pass loop filter (LPF). But high order SDM needs high order LPF. Considering above factors, a third-order single-loop SDM is used in this design.

4. Experimental results

The synthesizer chip was designed and implemented in a 0.13 μm CMOS process. The chip area including the pads is 1.26×1.44 mm^2, while the active area is about 0.36 mm^2. A die photograph of the test chip is shown in Fig. 7. The chip consumes 39.6 mW in the 10 GHz band.

The frequency synthesizer's performance is measured using divide-by-2 circuit. The reference clock is derived from an off-chip 33 MHz crystal oscillator. Figure 8 shows the measured FS phase noise at 4.375 GHz. The frequency synthesizer's integrated phase noise is less than 1°, the in-band phase noise is –89 dBc/Hz at 10 kHz offset and the out-band phase noise is –114.8 dBc/Hz at 1 MHz offset with a 4.375 GHz carrier. Figure 9 shows the measured spectrum indicating the reference spurs are –60.3 dBc at 33 MHz offset frequency with a 5.6 GHz carrier. Table 1 summarizes the FS performance and gives a comparison with a few published results. Compared to those similar synthesizers this work performance is competitive on phase noise and spur.

5. Conclusions

An 8.75–11.2 GHz ΣΔ Frac-*N* frequency synthesizer for multi-mode zero-IF transceiver application has been presented. It was fabricated using a standard 0.13 μm CMOS technology. Measurement results show that the frequency synthesizer's integrated phase noise is less than 1° with a 4.375 GHz carrier, and the reference frequency spur is below –60 dBc.

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