Multimode high-resolution DPWM for RF class-D amplifiers*

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Abstract: This paper describes a multimode high-resolution digital pulse width modulator. This modulator, based on a novel hybrid structure, not only has a programmable duty cycle but also realizes phase modulation. A 576 ps pulse resolution is achieved based on a 13.56 MHz switching frequency for near field communication. Fabricated in a SMIC 0.18-μm EEPROM CMOS process, the total area of modulator is only 130 $\times$180 μm^2. Measurement results validate the multi-mode modulation function and high pulse resolution.

Key words: (D)PWM; modulator; class-D amplifier; AM; PM
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1. Introduction

Pulse-width-modulation (PWM) is a technique for controlling analog circuits with a digital signal in which the duty cycle of a square wave is modulated to encode a specific input signal using a pulse-width modulator. PWM is employed in a wide variety of applications, ranging from measurement and communication to power control and conversion. As the critical block in an RF class-D amplifier, PWM provides two crucial advantages. The first one is that it encodes a signal into a few discrete levels, with the information represented in pulse duty ratios or variable phase. This coding characteristic permits energy to be delivered by switching among a small number of discrete power sources. The second advantage is the ability to recover the signal from its discrete-level form with a passive filter. However, the practical implementation of PWM is a very challenging task because of the following conflicting requirements: high resolution, low power consumption and small silicon area occupied by the PWM.

The implementation of PWM includes analog and digital methods. Although the analog PWM modulators[1,2] have a good linearity, they are susceptible to interference and have bad control flexibility. Compared with analog PWM, the advantage of digital PWM (DPWM) is excellent programmability and better noise immunity. The direct implementation of a digital pulse width modulator includes the use of two methods: counter-based structures[3] and delay-line-based structures[4]. In counter-based DPWM, the required external clock frequency $2^N f_{sw}$ (N and f_{sw} are the desired bit resolution and switching frequency respectively) would be very challenging and it would take a significant amount of power, while delay-line-based DPWM reduces the clock frequency to the switching frequency at the cost of a large digital multiplexer (2^N : 1) and a large delay-line (at least 2^N delay units). In recent years, it has been reported that some hybrid DPWM structures[5–7] have made tradeoffs between the high clock frequency requirements and large hardware requirements. However, multimode modulation with amplitude modulation (AM) and phase modulation (PM) is absent in these structures, which limits the DPWM application to RF. Especially under a near field communication (NFC) application[8], the system usually needs to use different modulation modes to satisfy different communication data rates. Furthermore, the differential PWM waveforms required in most RF class-D amplifiers are also hard to implement in these structures.

In this paper, a novel multimode DPWM with discretely adjustable phase for RF class-D amplifiers is proposed. This modulator uses an analog ring-oscillator with a 2^{N_L}(N_L is the least significant bit (LSB)) delay cell to generate versatile delay clocks and make up the pulse waveforms by frequency division and combinatorial logic. A look-up table is employed to realize the multi-mode control for class-D amplifiers. The proposed architecture and the operation principle are presented. Circuit design and measurement results are also shown.

2. System architecture

Figure 1 shows the block diagram of proposed DPWM modulator in a class-D amplifier system. The modulator is

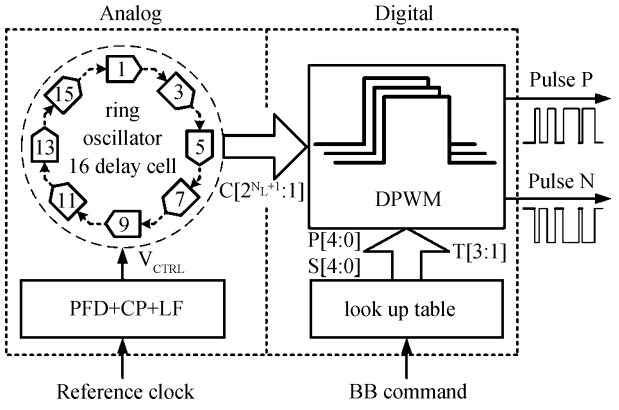

Fig. 1. Diagram of proposed DPWM modulator. The analog part includes a phase frequency detector (PFD), a charge pump (CP), a loop filter (LP) and a ring oscillator. The digital part includes DPWM unit and look up table.

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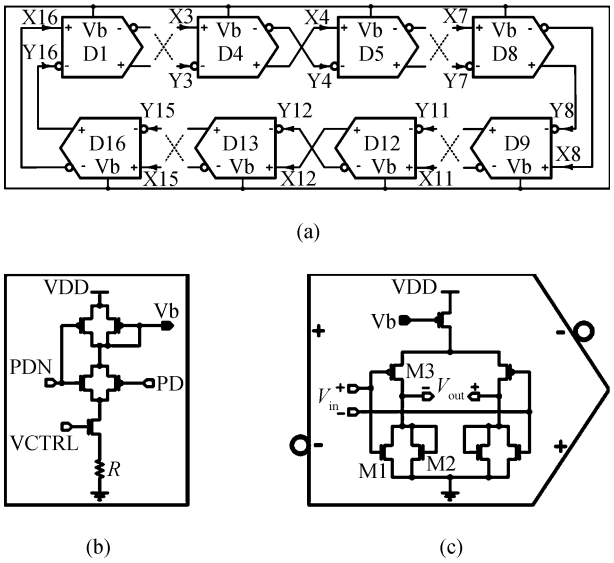


Fig. 2. Ring-oscillator. (a) Ring. (b) Input stage. (c) DCSL delay cell.

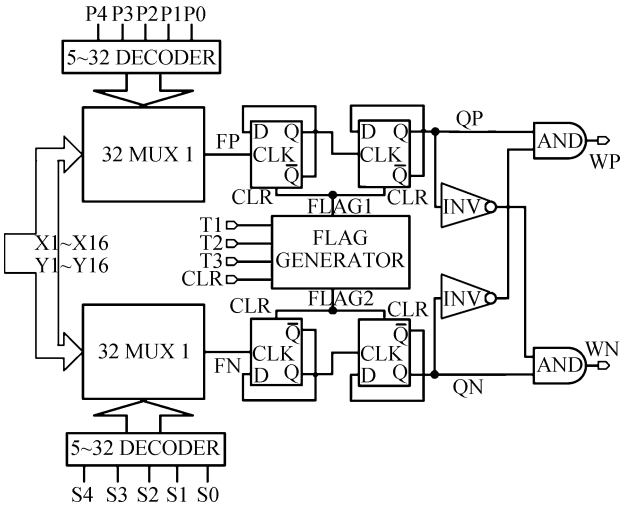


Fig. 3. Digital pulse width modulator.

mainly composed of a differential ring-oscillator and a DPWM unit. The ring-oscillator with 2^{N_L} delay cell offers 2^{N_L+1} clocks with $\pi/2^{N_L}$ phase shifts for DPWM, which generates the discretely adjustable pulse width. The relation between oscillator frequency (f_{sys}) and switching frequency is $f_{sys} = 2^{N-N_L} f_{sw}$ (N is 6 and N_L is 4 in this design). Compared with counter-based DPWM and delay-line-based DPWM, a trade-off between the system clock frequency and the scale of the delay-line is made. In addition, the DPWM accepts the AM or PM command from the look-up table, and translates it into one or more differential PWM driving waveforms for the class-D power amplifier. The adoption of a look-up table improves the control flexibility by programmable EEPROM or other memory inner chip. Based on the phase-locked loop (PLL), this modulator can provide variable switching frequency based on the external reference clock.

3. Circuit implementation

3.1. Multi-phase ring oscillator

Since a PLL oscillator is a required block in most RF systems, sharing the oscillator with other blocks can effectively improve the system power efficiency and reduce chip area. Figure 2(a) shows the 32-phase (X1–X16 and Y1–Y16) ring-oscillator based on a 16-stage differential current steering logic (DCSL) cell. The frequency of ring-oscillator incorporating this cell can be varied by more than four orders of magnitude with less than a twofold variation in the amplitude[9]. An input stage translating control-voltage into bias-current is shown in Fig. 2(b). The structure of the individual delay cell is shown in Fig. 2(c). The delay cell has the property of an inverter when the dimension of M1 is much larger than M2. It consumes very low power (8 μA under 54.24 MHz). The output voltage rise-time (t_{LH}) and fall-time (t_{HL}) can be derived according to the time of charging and discharging the capacitance of the next stage. Therefore, the frequency of oscillator can be expressed as

$$f_{\text{oscillator}} = \frac{1}{t_{\text{delay}}} = \frac{2}{t_{\text{LH}} + t_{\text{HL}}} \approx \frac{1}{C_{\text{out}}} \times \left\{ \frac{V_{\text{th}}}{2I_{\text{bias}}} + \sqrt{\frac{1}{2\mu_n C_{\text{ox}} I_{\text{bias}} (W/L)_1}} \times \left[1 + \frac{1}{2} \sqrt{\frac{(W/L)_2}{(W/L)_1}} \right] \right\}, \quad (1)$$

where C_{out} is the total output capacitance of delay cell, V_{th} is the threshold voltage of NMOS transistor and I_{bias} is the biasing current of delay cell. Equation (1) shows the oscillation frequency is nearly proportional to bias current, so an approximate linear VCO gain versus bias current can be achieved.

3.2. Digital pulse width modulator

The proposed DPWM circuit with 6-bit resolution is shown in Fig. 3. The left part is two 32 : 1 multiplexers which select clock signals from X1–X16 and Y1–Y16, while the right part generates the pulse width waveforms by dividing the selected clocks and combining them. The 1 : 4 divider is reset by the flag generator before each PWM occurs. All control signals (P0–P4, S0–S4 and T1–T3) are given by the look-up table.

A timing diagram for the DPWM is shown in Fig. 4. FP and FN are successively selected from X1–X16 and Y1–Y16. QP and QN are generated from the 1 : 4 frequency division of FP and FN, respectively. Controlled by the reset signals (FLAG1 and FLAG2), QP and QN generate pulses WP and WN, whose widths are determined by the phase differences between the leading edges and trailing edges of QP and of QN.

Due to the NAND operation between QP and QN, the time differences between QP and QN will become different pulse-widths. Through combining the versatile clocks, a multimode modulation with AM and PM is implemented in the DPWM. On the one hand, a range of pulse-width between $1/2^{N+1} f_{sw}$ and $1/2 f_{sw}$ is given according to the smallest phase-shift in the clock group. The smallest pulse width of 576 ps and the largest pulse width of 36.87 ns are obtained based on a 13.56 MHz switching frequency and the 6-bit resolution in this design. On

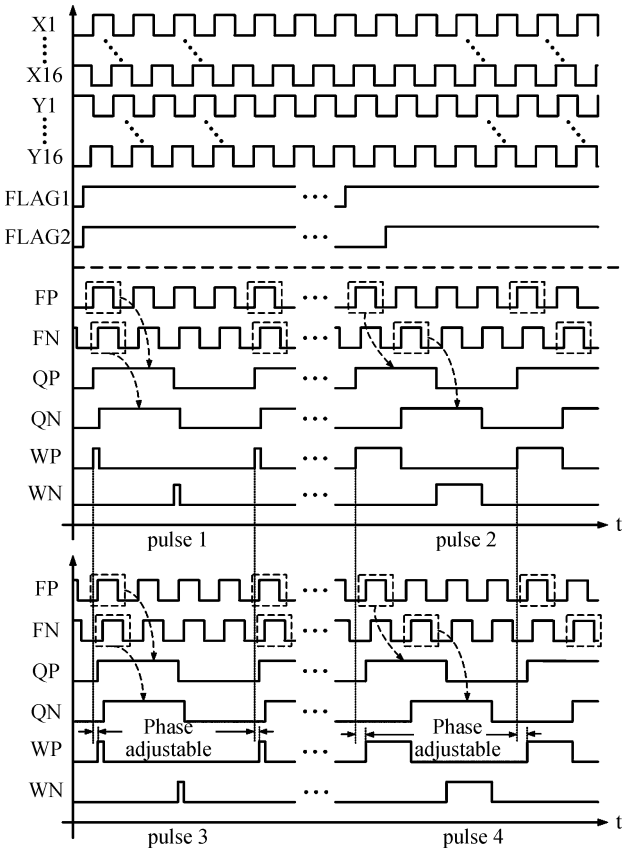


Fig. 4. Timing diagram of DPWM.

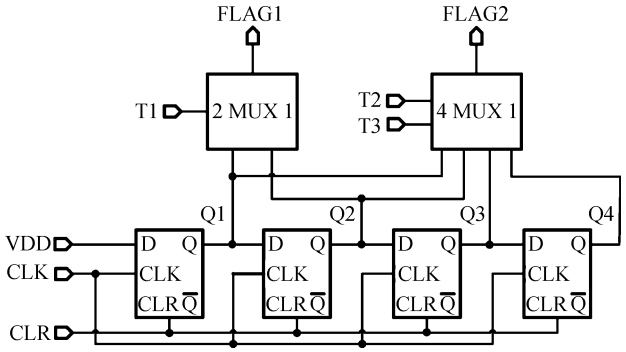


Fig. 5. Flag generator.

the other hand, the phase of pulse width is discontinuously adjusted by changing FP and FN. The range of adjustable phase is from $\pi/64$ to π. A typical π-phase adjustment is called binary phase shift keying (BPSK). Therefore, through continuously switching selected clocks and control signals, mixed modulation with AM and PM is realized in this DPWM.

As shown in Fig. 4, different pulse-widths pulse 1 (pulse 3) and pulse 2 (pulse 4) are generated by giving different FLAG1 and FLAG2, while pulse 1 (pulse 2) and pulse 3 (pulse 4) have the same pulse width but different starting phases.

Figure 5 shows the flag generator, which generates four reset signals with one clock-cycle delay in turn. The timing diagram is shown in Fig. 6.

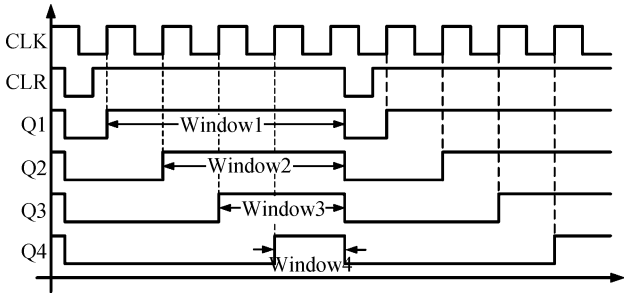
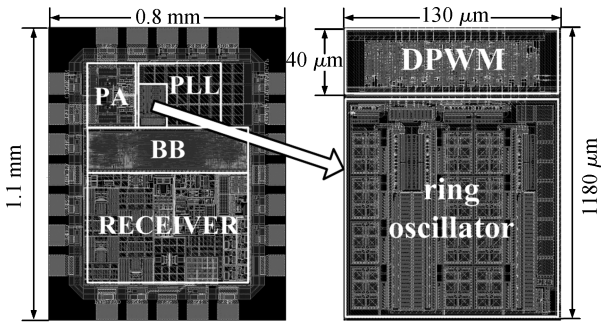
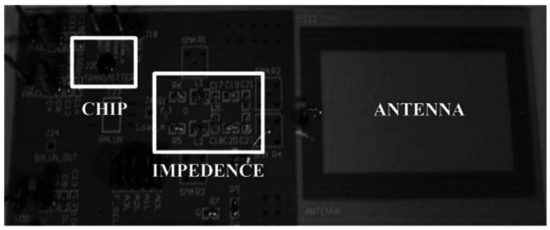


Fig. 6. Flag timing diagram.



(a)



(b)

Fig. 7. (a) Micrograph of PWM modulator. (b) PCB for test.

4. Experiment results

The RF chip was designed and fabricated in a 0.18 μm EEPROM 2P4M CMOS process. As shown in Fig. 7(a), the total area of the modulator is about 130×180 μm^2, of which the DPWM is only 130×40 μm^2. A printed circuit board (PCB) with a copper antenna (100×70 mm^2) was manufactured for an RF interface test. Software connected to the chip through a serial port is used to switch between different modulation modes during the measurement.

In order to observe the multimode operation of the DPWM, pulse-width waveforms are scanned by observing the class-D amplifier output signal from the antenna. Figure 8(a) shows the RF signal in on/off keying (OOK) mode, while amplitude shift-keying (ASK) with 10% modulation index is shown in Fig. 8(b). Figure 8(c) shows the load modulation of the subcarrier, in which the frequency of subcarrier is 4 times the data rate of system. The BPSK mode is shown in Fig. 8(d). In addition to the central frequency, there are two side bands with a $f_{sw}/16$ frequency distance from the central frequency. $f_{sw}/16$ corresponds to the data rate of system. Figure 8(e) shows the measured phase resolution. Limited by testing error and dis-

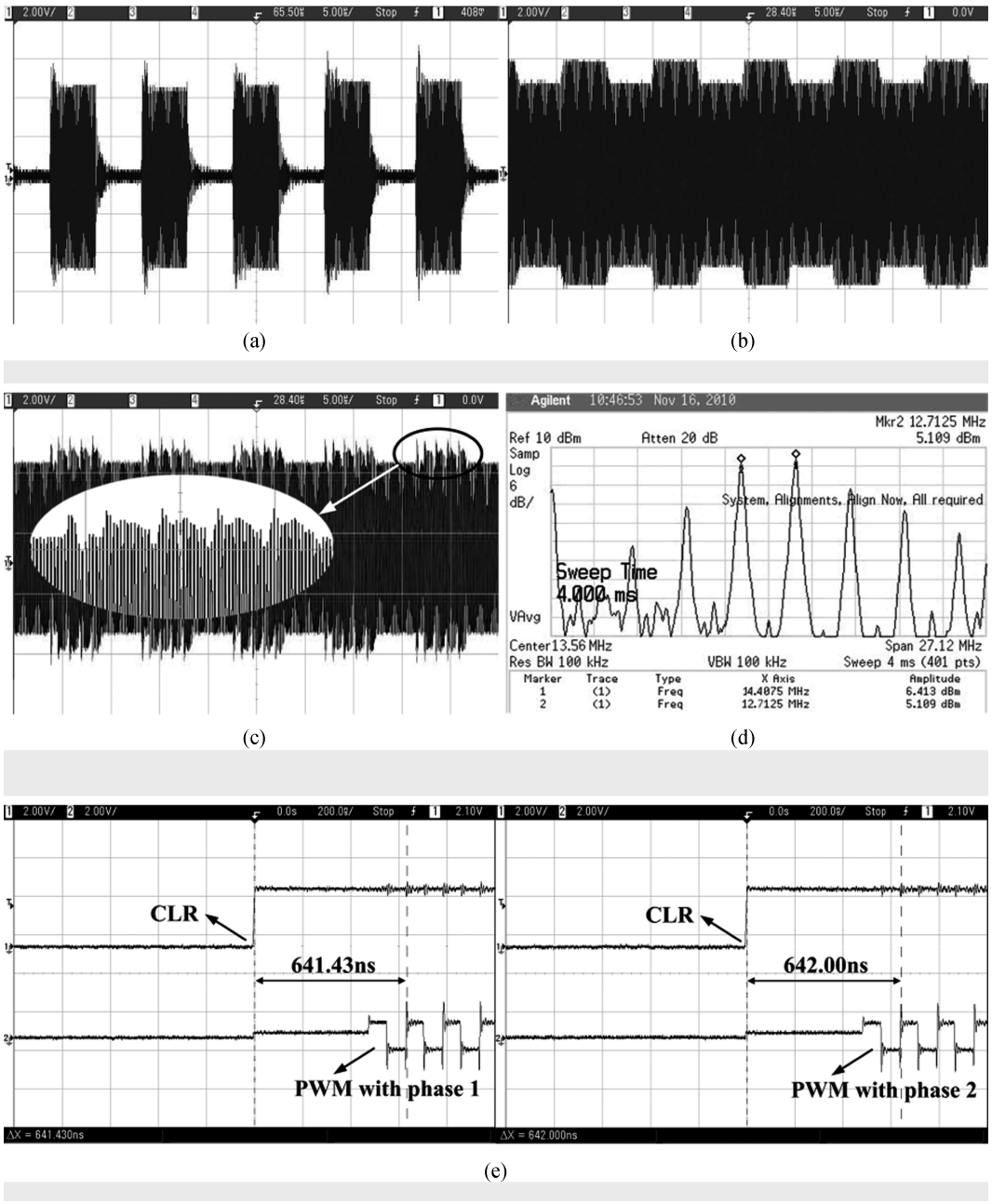


Fig. 8. Measurement results. (a) OOK modulation. (b) 10% ASK modulation. (c) Subcarrier load modulation. (d) BPSK modulation. (e) Phase resolution.

Table 1. Compared results with reference articles.

Parameter	Ref. [5]	Ref. [7]	This work
Multimode	No	No	Yes
Delay cell scale	64	32	16
Switching frequency (MHz)	4	0.781	13.56
Oscillator frequency (MHz)	128	25	54.24
Pulse width resolution (ns)	0.977	1.25	0.57

play precision, the CLR signal in flag generator is used as the reference signal. The measured resolution of 570 ps is similar to our theoretical design.

Finally, Table 1 compares this design with partly reference articles.

5. Conclusion

This paper presents a multimode high-resolution DPWM based on a novel hybrid structure. This modulator not only generates pulse width modulation, but also realizes phase modulation using discontinuously adjustable phase shifts. This modulator realizes the multimode method with high switching frequency, low oscillator frequency and high pulse resolution. Fabricated in a SMIC 0.18-μm EEPROM CMOS process, the total area of modulator is only 130 $\times$ 180 μm^2. Measured results demonstrate the multi-mode modulation and a 570 ps pulse resolution based on a13.56 MHz switch frequency using

this design.

References

[1] Kaboli S, Moayedi A, Oraee H. Application of random PWM technique for reducing the high frequency harmonics in class-D amplifier. IET Conference on Power Electronics, Machines and Drives, 2008: 406

[2] Nielsen M, Larsen T. An RF pulse width modulator for switch-mode power amplification of varying envelope signals. Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2007: 277

[3] Wei G Y, Horowitz M. A fully digital, energy-efficient, adaptive power-supply regulator. IEEE J Solid-State Circuits, 1999, 34(4): 520

[4] Dancy A P, Chandrakasan A P. Ultra low power control circuits for PWM converters. IEEE PESC, 1997, 1: 21

[5] O'Malley E, Rinne K. A programmable digital pulse width modulator providing versatile pulse patterns and supporting switching frequencies beyond 15 MHz. IEEE APEC, 2004, 1: 53

[6] Foley R, Kavanagh R, Marnane W, et al. Multiphase digital pulsewidth modulator. IEEE Trans Power Electron, 2006, 21(3): 842

[7] Yousefzadeh V, Takayama T, Maksimovi D. Hybrid DPWM with digital delay-locked loop. IEEE Workshops on Computers in Power Electronics, 2006: 142

[8] Standard ECMA-340. Near field communication interface and protocol (NFCIP-1). ECMA International, December 2002

[9] Razavi B. Design of analog CMOS integrated circuits. McGraw-Hill Higher Education, 2001: 520