Gate length dependence of the shallow trench isolation leakage current in an irradiated deep submicron NMOSFET

Liu Zhangli(刘张李)[1,2,†], Hu Zhiyuan(胡志远)[1,2], Zhang Zhengxuan(张正选)[1], Shao Hua(邵华)[1], Chen Ming(陈明)[1,2], Bi Dawei(毕大炜)[1], Ning Bingxu(宁冰旭)[1,2], and Zou Shichang(邹世昌)[1]

[1]State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China
[2]Graduate University of the Chinese Academy of Sciences, Beijing 100049, China

Abstract: The effects of gamma irradiation on the shallow trench isolation (STI) leakage currents in a 0.18 μm technology are investigated. NMOSFETs with different gate lengths are irradiated at several dose levels. The threshold voltage shift is negligible in all of the devices due to the very thin oxide thickness. However, an increase in the off-state leakage current is observed for all of the devices. We believe that the leakage is induced by the drain-to-source leakage path along the STI sidewall, which is formed by the positive trapped charge in the STI oxide. Also, we found that the leakage is dependent on the device's gate length. The three-transistor model (one main transistor with two parasitic transistors) can provide us with a brief understanding of the dependence on gate length.

Key words: oxide trapped charge; parasitic transistor; shallow trench isolation; total ionizing dose
DOI: 10.1088/1674-4926/32/6/064004 **EEACC:** 2570

1. Introduction

Changes in microelectronic materials and device structures have resulted in very significant changes to integrated circuit technologies in recent years. The sharp decrease of total ionizing dose (TID) effects in the thin gate oxides of MOS transistors was initially shown by Saks and co-workers in publications dating back to 1984 and 1986[1, 2]. They predicted that technology scaling would reduce a MOSFET's susceptibility to radiation induced damage in gate oxides. This is due to the fact that, to first order, the defect buildup in gate oxides scales with T_{ox}[3]. The radiation tolerance of thin oxides is further enhanced by the increased likelihood of positive charge annihilation or compensation by tunneling electrons from adjacent materials[4]. Radiation tests have shown that thin gate oxides are virtually unaffected by total ionizing irradiation up to multi-Mrad(SiO_2) levels.

Shallow trench isolation (STI) is becoming the dominant isolation technology for commercial deep submicron CMOS processes. Although the gate oxide becomes thinner and less sensitive to TID irradiation, the STI oxide does not scale down correspondently[5]. As a result, radiation induced charge trapping in the STI oxide still leads to macroscopic effects such as a drain-to-source leakage current and ultimately limits the radiation tolerance of CMOS circuits[6–9]. Gate length and width have a great influence on the TID response of an NMOS transistor. In Ref. [10], the authors found an important effect of gate length on the radiation induced threshold voltage shift due to the thick oxide (40 nm). In Refs. [11, 12], TID effects of 0.25 μm and 0.18 μm devices were investigated, respectively.

In this contribution, we will further analyze gate length dependence on the total ionizing effect for a deep submicron transistor. In particular, we will present an experimental study coupled with the three-transistor model to understand the radiation response of parasitic transistors.

2. Experiment detail

All devices were fabricated in 0.18 μm CMOS technology. STI was introduced and the trench oxide thickness is about 390 nm. The gate oxide is 3 nm. Different transistor sizes were chosen: W/L = 10 μm/10 μm, 10 μm/0.5 μm, 10 μm/0.18 μm. All the samples were ceramic packaged. The operating voltage is 1.8 V.

Irradiation experiments were carried out at the Xinjiang Technical Institute of Physics & Chemistry at the Chinese Academy of Sciences using a ^{60}Co γ source, typically at a dose rate of 200 rad(Si)/s. During radiation exposure, the gate of the devices was biased at 1.8 V with all other terminals grounded. The temperature was monitored and kept at room temperature. Electrical measurements were obtained prior to irradiation and after step stress irradiations up to 100, 200, 250, 300, 400, and 500 krad(Si). Transfer (I_{ds}–V_{gs}) characteristics were measured in linear region (V_{ds} = 50 mV) for all devices. These I–V curves were taken within half an hour following exposure.

3. Results and discussion

3.1. I_{ds}–V_{gs} versus TID

Figure 1 shows a series of transfer I–V curves measured on different sizes of transistor irradiated in steps up to 500 krad(Si). As shown in Fig. 1(a), after a total dose radiation level of 250 krad(Si) for W/L = 10 μm/10 μm

† Corresponding author. Email: liuzhangli@mail.sim.ac.cn
Received 28 December 2010, revised manuscript received 31 January 2011

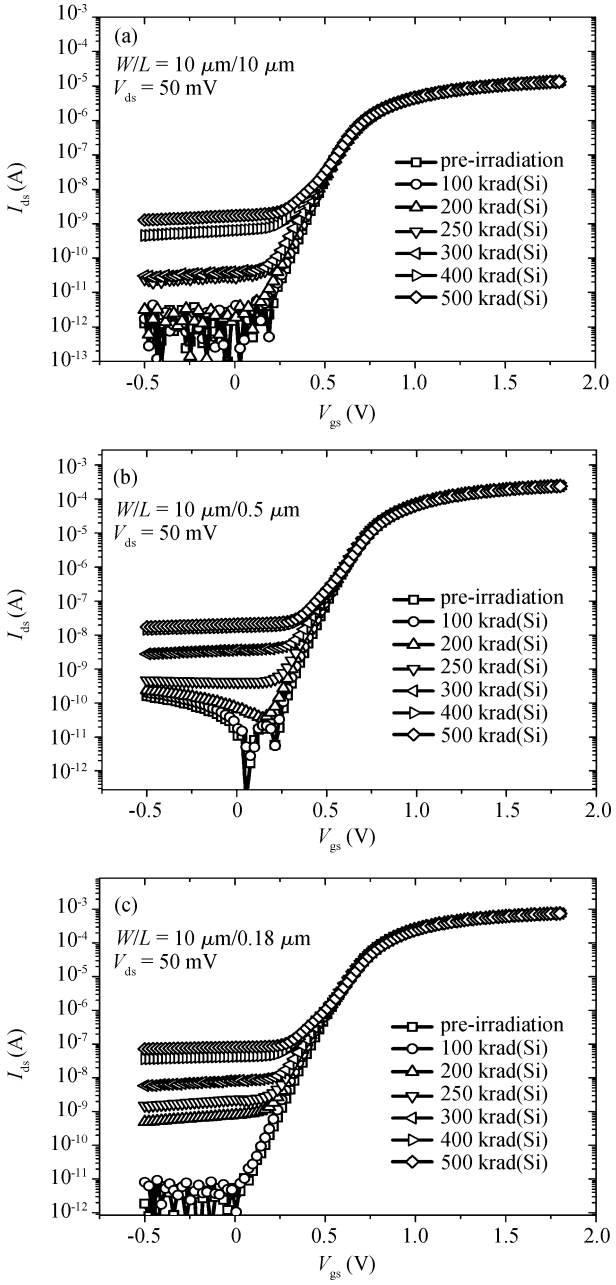

Fig. 1. I_{ds}–V_{gs} characteristics as a function of dose for the transistor with (a) $W/L = 10\ \mu$m/10 μm, (b) $W/L = 10\ \mu$m/0.5 μm and (c) $W/L = 10\ \mu$m/0.18 μm.

transistor, a significant increase in off-state leakage current is observed. The leakage current curve shows weak gate control, which means that the leakage path is at a deep depth along the STI sidewall[13]. When the total ionizing dose accumulated to 500 krad(Si), the drain current at $V_{gs} = 0$ V is approximately 3 orders of magnitude higher than the corresponding pre-irradiation value. For the other two transistor sizes, a sharp increase of leakage current is observed at 200 krad(Si). Up to a dose level of 500 krad(Si), the leakage is 10^{-8} A for transistor with $W/L = 10\ \mu$m/0.5 μm, and 10^{-7} A for the transistor with $W/L = 10\ \mu$m/0.18 μm. As shown in Fig. 2, the off-state leakage current (I_{ds} @ $V_{gs} = 0$ V) was extracted for all transistor sizes as a function of dose level. The positive charge trapped in the

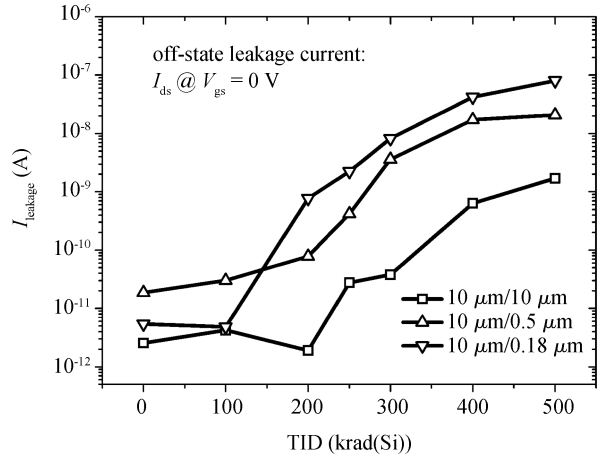

Fig. 2. Evolution of the leakage current with TID for different transistor sizes.

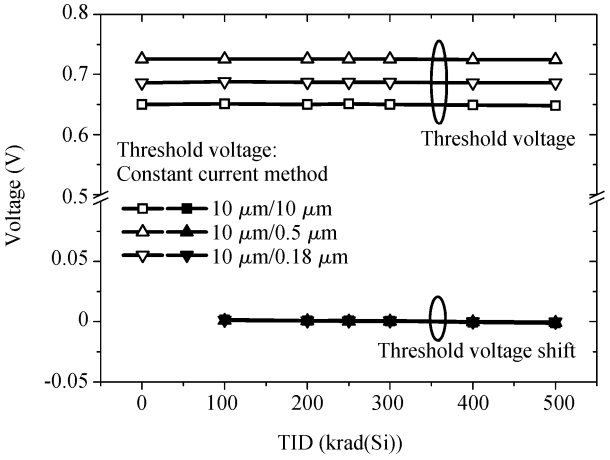

Fig. 3. Threshold voltage evolution with TID for different size transistors.

lateral STI oxide formed a conductive channel through which leakage the current could flow between the source and drain, and the parasitic lateral transistors could turn on[14]. We can see that, the shorter length of transistor, the larger increase of the off-state leakage. The large off-state leakage leads to more pronounced characteristic degradation, such as large power consumption and an increase of static current.

As shown in Fig. 3, a negligible threshold voltage shift was observed for transistors with different sizes. The transistor's gate oxide is about 3 nm. It is well known that the total oxide trapped charge is proportional to thickness. However, the most important deviation from the t_{ox}^2 dependence occurs in very thin oxides[3], where tunnel annealing eliminates, or at least neutralizes, trapped charge near the interface. The point is that for thin oxides, this annealing process occurs at both interfaces and accounts for all or nearly all of the trapped oxide charge. For thin-enough oxides, the two tunneling fronts meet in the center of the oxide, leaving no net positive oxide charge[4]. That is to say, a negligible threshold voltage shift is observed for the device after irradiation. This leaves isolation oxide as the main remaining total dose problem, which we will discuss in detail below.

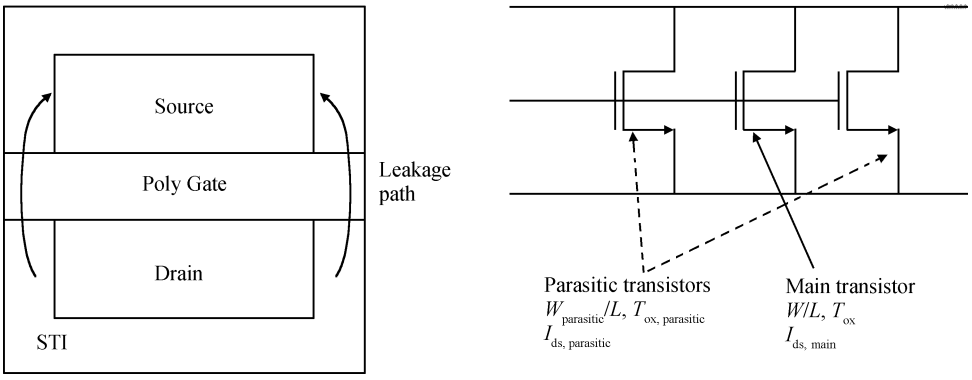

Fig. 4. Drain-to-source leakage path in an NMOS transistor, circuit model and relevant parameters.

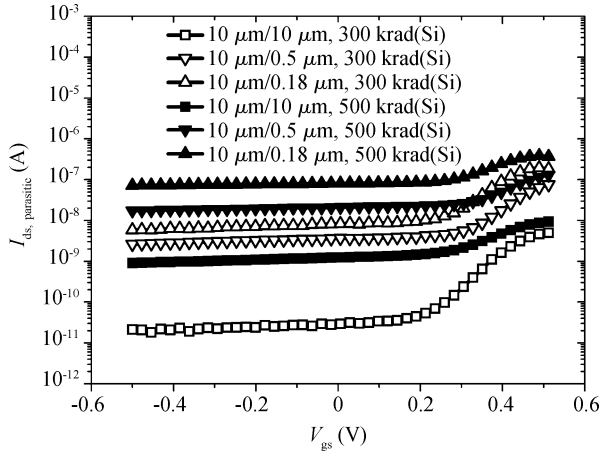

Fig. 5. Drain current $I_{ds,\ parasitic}$ of lateral parasitic transistors as a function of V_{gs} at a dose level of 300 and 500 krad(Si).

3.2. Three transistor model

Figure 4 provides a view of an NMOS after total ionizing dose radiation with two parasitic leakage paths, which can be modeled by two NMOS in parallel with the main transistor device controlled by the thin gate oxide. The three MOSFETs in Fig. 4 have the same gate length, which is the draw length of the device. The two parasitic transistors have a gate width $W_{parasitic}$ and an effective gate oxide thickness $T_{ox,\ parasitic}$, which depend on the portion of the interface at the STI sidewall. A portion of the interface at the STI sidewall gets inverted due to the dose level of radiation and charge buildup in the isolation oxide. The total drain current Ids of the NMOS is given by the sum of the drain current of the main transistor and the two parasitic transistors, $I_{ds} = I_{ds,\ main} + I_{ds,\ parasitic}$, since there is a contribution from two edges of the STI under the poly gate. Under the reasonable assumptions that the static characteristics of the main transistor are particularly unaffected by ionizing radiation and that the parasitic transistors give a negligible contribution before irradiation[15], it is possible to study the electrical properties from its drain current $I_{ds,\ parasitic}$ obtained by subtracting pre-irradiation $I_{ds,\ pre}$ from the total I_{ds} measured after irradiation. The $I_{ds,\ parasitic}$–V_{gs} curves at dose of 300 and 500 krad(Si) are briefly shown in Fig. 5. The drain current of the parasitic transistor is larger for shorter length transistors, and increase with total ionizing dose. As the $W_{parasitic}$ is basically equal for the three types of device during irradiation, the leakage current is inverse proportional to the gate length. The leakage has weak dependence on the gate bias, which means that the leakage path is at a deep depth along the STI sidewall.

4. Conclusion

In conclusion, the total ionizing dose effect of a deep submicron transistor with different gate lengths was studied in this work. We found that the threshold voltage shift induced by the gate oxide is negligible, owing to the thin oxide thickness. The main characteristic degradation is a large increase of off-state leakage, which is attributed to the leakage path formed along the STI sidewall. A larger increase of off-state leakage was observed for a shorter length transistor. By extracting the I–V curves of the parasitic transistor, we can obtain a brief understanding of the device radiation response dependence on gate length.

References

[1] Saks N S, Ancona M G, Modolo J A. Radiation effects in MOS capacitors with very thin oxides at 80 K. IEEE Trans Nucl Sci, 1984, 31(6): 1249

[2] Saks N S, Ancona M G, Modolo J A. Generation of interface states by ionizing radiation in very thin MOS oxides. IEEE Trans Nucl Sci, 1986, 33(6): 1185

[3] Boesch H E, McGarrity J M. Charge yield and dose effects in MOS Capacitors at 80 K. IEEE Trans Nucl Sci, 1976, 23(6): 1520

[4] Benedetto J M, Boesch H E, McLean F B, et al. Hole removal in thin gate MOSFET's by tunneling. IEEE Trans Nucl Sci, 1985, 32(6): 3916

[5] Barnaby H J. Total ionizing dose effects in modern CMOS technologies. IEEE Trans Nucl Sci, 2006, 53(6): 3103

[6] McLain M, Barnaby H J, Holbert K E, et al. Enhanced TID susceptibility in sub-100 nm bulk CMOS I/O transistors and circuits. IEEE Trans Nucl Sci, 2007, 54(6): 2210

[7] Barnaby H J, Mclain M, Esqueda I S. Total ionizing dose effects on isolation oxides in modern CMOS technologies. Nuclear Instruments and Methods in Physics Research B, 2007, 261: 1142

[8] Esqueda I S, Barnaby H J, Alles M L. Two dimensional methodology for modeling radiation-induced off-state leakage in CMOS technologies. IEEE Trans Nucl Sci, 2005, 52(6): 2259

[9] Faccio F, Barnaby H J, Chen X J, et al. Total ionizing dose effects in shallow trench isolation oxides. Microelectron Reliab, 2008,

48: 1000

[10] Djezzar B, Smatti A, Amouche A, et al. Channel length impact on radiation induced threshold voltage shift in NMOSFET's devices at low gama rays radiation doses. IEEE Trans Nucl Sci, 2000, 47(6): 1872

[11] Meng Zhiqin, Hao Yue, Tang Yu, et al. Total ionizing dose effects of deep submicron nMOSFET devices. Chinese Journal of Semiconductors, 2007, 28(2): 241 (in Chinese)

[12] Wang S H, Lu Q, Wang W H, et al. The improvement on total ionizing dose (TID) effects of the ultra-deep submicron MOSFET featuring delta doping profiles. Acta Phys Sin, 2010, 59(3): 1970 (in Chinese)

[13] Youk G U, Khare P S, Schrimpf R D, et al. Radiation enhanced short channel effects due to multi-dimensional influence from charge at trench isolation oxides. IEEE Trans Nucl Sci, 1999, 46(6): 1830

[14] Schwank J R, Shaneyfelt M R, Fleetwood D M, et al. Radiation effects in MOS oxides. IEEE Trans Nucl Sci, 2008, 55(4): 1833

[15] Re V, Manghisoni M, Ratti L, et al. Impact of lateral isolation oxides on radiation-induced noise degradation in CMOS technologies in the 100-nm regime. IEEE Trans Nucl Sci, 2007, 54(6): 2218