CMOS highly linear direct-conversion transmitter for WCDMA with fine gain accuracy*

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Abstract: A highly linear, high output power, 0.13 μm CMOS direct conversion transmitter for wideband code division multiple access (WCDMA) is described. The transmitter delivers 6.8 dBm output power with 38 mA current consumption. With careful design on the resistor bank in the IQ-modulator, the gain step accuracy is within 0.1 dB, hence the image rejection ratio can be kept below −47 dBc for the entire output range. The adjacent channel leakage ratio and the LO leakage at 6.8 dBm output power are −44 dBc @ 5 MHz and –37 dBc, respectively, and the corresponding EVM is 3.6%. The overall gain can be programmed in 6 dB steps in a 66-dB range.

Key words: WCDMA; UMTS; transmitter; direct conversion; CMOS
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1. Introduction

Technology development within mobile communications is seeking a low cost full chip solution. One possible way to address the problem is to eliminate expensive off-chip components and to use fewer on-chip blocks. For transmitter design, direct-up-conversion (DUC) architecture is a good candidate for the low cost design. CMOS technology is popular nowadays for its low cost and high integration level. Obviously, a direct conversion CMOS transmitter is a good choice.

This paper presents a highly linear and high output power transmitter for wideband code division multiple access (WCDMA) based on DUC architecture to meet 3GPP protocol requirements. The circuit is implemented in a 0.13 μm process with multiple supply voltage. It delivers a high output power while still leaving large headroom on linearity for the external PA. A 66 dB dynamic range with high gain step accuracy is achieved using only two design blocks, hence lowering the gain control requirement on the baseband blocks.

2. System design

2.1. System architecture

Figure 1 shows the block diagram of a direct conversion WCDMA transmitter. The HPSK modulated signal is provided by the digital baseband and converted to an analog signal by DAC. The signal is then processed by the successive low past filter to filter out the image and clock spurs. This clean analog signal is delivered to the I/Q modulator and up-converted to the carrier frequency. Then the RF signal is amplified by the driver amplifier and further amplified by an external PA. Since WCDMA is frequency division duplex (FDD), the transmitter and receiver work simultaneously. Hence the noise of the transmitter will deteriorate the receiver performance, especially the noise figure. A sound acoustic wave (SAW) filter can effectively lower the noise seen by the receiver and limit the deterioration to an acceptable level. In order to avoid the LO-pulling problem, an I/Q divider is used to generate a quadrature LO signal.

Considering the 3 dB loss of the duplexer and SAW, and 23 dB normal gain of the external PA, the maximum output power at the driver amplifier should be at least 5 dBm to meet the class 3 output power requirement specified in the 3GPP protocol[1].

2.2. System consideration

In 3GPP protocol, there are several specifications needed to be satisfied. The linearity is specified by an adjacent channel leakage ratio (ACLR), while modulation accuracy is specified by the term error vector magnitude (EVM). Unlike the GSM systems, the variable envelope modulation employed increases the spectral efficiency but requires linear amplification to ensure the modulation accuracy in WCDMA. This section includes detailed discussion on these specifications.

2.2.1. Gain control scheme

In code division multiple access (CDMA) communication, multi-users share the same frequency channel. The signal is

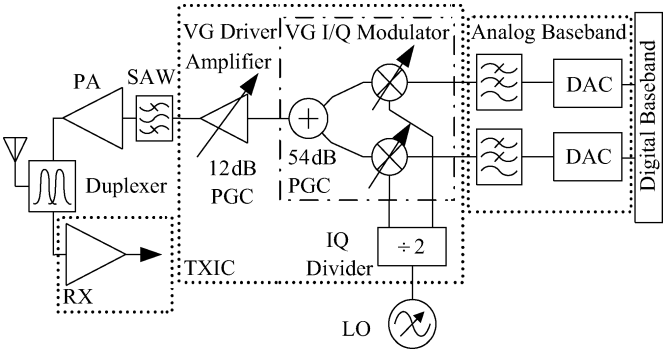

Fig. 1. Block diagram of a direct conversion transmitter.

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valuable only for a specific user while treated as noise for others. But if the signal power for a certain user is too large, the noise floor of the whole channel increases and hence deteriorates the SNR of the other users. Therefore, the 3GPP protocol placed a strict requirement on power control. For the Power Class 3 requirement[1], the dynamic range of output power is 74 dB, ranging from –50 to 24 dBm. The gain step is 1 dB with 0.5 dB step accuracy, which is a great challenge in the prevalent CMOS process.

In order to fulfill this large control range, it is quite reasonable to distribute the gain control to each block. Meanwhile, the combination of coarse control and fine control will make the realization easier. The gain step for RF blocks, such as driver amplifier and I/Q modulator, is set to 6 dB for coarse gain control while the 1 dB step is implemented in the analog baseband where the accuracy is much easier to guarantee. Since the gain for the external PA is usually fixed, the RF gain control will be totally implemented in the driver amplifier.

In the proposed system, the I/Q modulator has a 54 dB gain range and the driver amplifier has a 12 dB gain range. The whole transmitter provides 66 dB gain range with a 6 dB gain step, relaxing the gain control requirement on the analog baseband and hence eliminating one VGA to save the power and chip area.

2.2.2. Linearity consideration

In the WCDMA communication system, the uplink signal is an HPSK modulated signal, which has a PAR of around 3.1 dB. It requires linear amplification, so the linearity of the system is crucial. In the 3GPP protocol, the adjacent channel leakage ratio (ACLR) is used to benchmark the linearity performance of the system. The ACLR is defined as the power leaked into the adjacent channel compared to the power in the main channel. The leaked power is mainly attributed to the third order inter-modulation (IMD3) and will deteriorate the SNR in the adjacent channel. When working in a strong nonlinear region, the fifth or even higher order inter-modulation will induce power leakage into the alternate channel, which is two channels away from the main channel. According to 3GPP protocol, the ACLR should be less than –33 dBc @ 5 MHz and –43 dBc @ 10 MHz.

Since PA is the main contributor to the nonlinearity, at least 10 dB headroom is reserved for it, which means that the ACLR at the driver amplifier output should be less than –43 dBc @ 5 MHz and –53 dBc @ 10 MHz. As stated earlier, the ACLR is introduced mainly by the IMD3 and other inter-modulation terms. As a reference, the relationship between OIP3 and ACLR can be given[2],

$$\mathrm{ACLR} = 2(P_{\mathrm{out}} - \mathrm{OIP_3}) - 9 + 0.85(\mathrm{PAR} - 3). \quad (1)$$

From Eq. (1), the $\mathrm{OIP_3}$ of the TXIC, should be at least 22 dBm in order to get 5 dBm linear output power with a −44 dBc ACLR. Using the Friis equation, the OIP3 of driver amplifier and mixer can be derived separately.

The designed mixer has good linearity, which benefits from the highly linear voltage to current conversion module. So the ACLR degradation is mainly induced by the driver amplifier stage. The IM3 cancelling is performed at a large output power in the designed driver amplifier. So the ACLR can still reach the standard even though the OIP3 of the system is lower than the value as Eq. (1) required.

2.2.3. EVM consideration

The error vector magnitude (EVM) is usually used to benchmark the quality of the modulated signal in digital communication systems. It measures the distortion both in magnitude and phase. The EVM degradation is caused by a lot of factors, including the inter-modulation, IQ imbalance, phase noise and dc offset. Each factor will dominate under different conditions.

For high and moderate output power, the main contributor to a large EVM is the image signal caused by IQ imbalance in the LO and baseband signal.

Assume the ideal IQ output signal can be expressed in Eq. (2),

$$f_{\mathrm{TX}}(t) = \cos\phi(t)\cos(\omega_{\mathrm{c}}t) - \sin\phi(t)\sin(\omega_{\mathrm{c}}t). \quad (2)$$

Considering the phase and gain imbalance on LO and BB signals, the real output IQ modulated signal should be written as

$$f_{\mathrm{TX}}(t) = \cos\phi(t)\cos(\omega_{\mathrm{c}}t) - (1+\delta)\sin[\phi(t)+\varepsilon]\sin(\omega_{\mathrm{c}}t + \sigma). \quad (3)$$

The IQ magnitude difference is denoted by δ, and ε stands for the phase offset on the baseband IQ signal. σ denotes the IQ phase offset in the LO signal. Based on the above equation, the image suppression can be modeled by Eq. (4)[3].

$$\mathrm{IMG_s} = 10\lg\frac{1 - 2(1+\delta)\cos(\varepsilon - \sigma) + (1+\delta)^2}{1 + 2(1+\delta)\cos(\varepsilon + \sigma) + (1+\delta)^2}. \quad (4)$$

The EVM contributed by the image product can be expressed by Eq. (5).

$$\mathrm{EVM_{img}} = \sqrt{10^{\mathrm{IMG_s}/10}}. \quad (5)$$

A −40 dBc image suppression will contribute only 1% EVM. So the image rejection ratio should be kept below −40 dBc to guarantee a good EVM performance.

For low output power, LO leakage induced by DC-offset are dominant ones. Assume the DC offset in baseband signal is Δ_{dc}, the term carrier suppression denoted by C_{s} is defined as

$$C_{\mathrm{s}} = 10\lg\frac{P_{\mathrm{CFT}}}{P_{\mathrm{TX}}} = 20\lg\frac{V_{\mathrm{CFT\_rms}}}{V_{\mathrm{TX\_avg}}}, \text{where } V_{\mathrm{CFT\_rms}} = \frac{\Delta_{\mathrm{dc}}}{\sqrt{2}}. \quad (6)$$

P_{CFT} and P_{TX} denote the power of the feed-through carrier signal and output signal separately. $V_{\mathrm{CFT\_rms}}$ and $V_{\mathrm{TX\_avg}}$ denote the root mean square value of the magnitude of the corresponding signal. And the contribution to the EVM is described in Eq. (7).

$$\mathrm{EVM_{CFT}} = \sqrt{10^{C_{\mathrm{S}}/10}}. \quad (7)$$

For the –20 dBm output, a 5 mV DC offset may deteriorate the EVM to 16%. Hence a calibration circuit is necessary. When the output power is very low, such as –50 dBm, noise will also contribute to the degradation of the EVM. But in this situation, there's no requirement on the EVM so the noise contribution can be neglected.

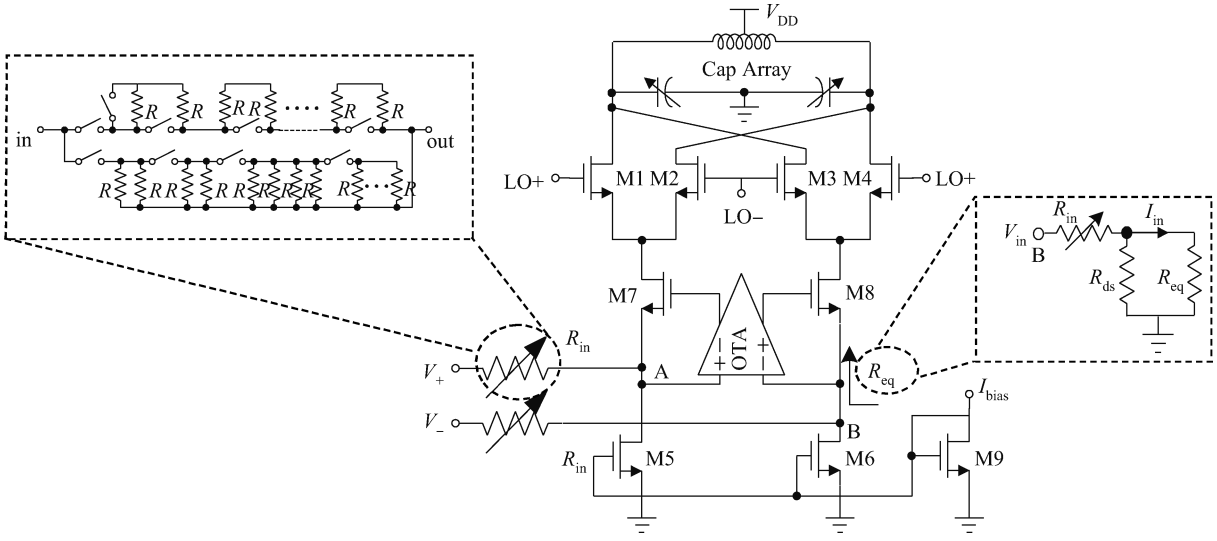

Fig. 2. Mixer and specific sub-block.

2.2.4. Noise consideration

In a FDD system like WCDMA, RX and TX work simultaneously. The power in the TX output is usually several orders of magnitude larger than the RX input signal. The TX noise floor may be comparable to the RX input and even overwhelm it. Hence a duplexer is usually used to provide isolation from the TX to RX channel, which is around 50 dB. In order to avoid too much degradation in NF performance in RX, the TX output noise floor at the RX port of the duplexer should be less than –162 dBc/Hz[4].

In the proposed transmitter, the analog baseband and modulator are providing attenuation rather than gain and only the driver amplifier has the gain. So the noise generated in the modulator is critical for the total output noise. The noise floor of the modulator at 190 MHz deviation from the carrier frequency should be no more than 1 nV/$\sqrt{\text{Hz}}$.

3. Circuit implementation

The TXIC includes a driver amplifier, an I/Q modulator and an I/Q divider. The supply voltage is 1.2 V for the I/Q modulator and divider, and 3.3 V for driver amplifier. Thick oxide devices are adopted in the driver amplifier.

3.1. I/Q modulator

The I/Q modulator consists of two identical mixers that process the I and Q signals. Figure 2 shows a schematic of the mixer. The circuit is an active mixer based on the Gilbert cell with some modifications[5]. The input voltage signal is turned into the current signal through the input resistors R_{in} instead of G_m of the input transistor that is used in the conventional Gilbert cell. Equation (8) shows the single-end analysis of the voltage to current conversion process. In order to make a linear conversion, the resistance R_{eq} seen at nodes B in Fig. 2 should be small enough compared to the input resistance of R_{in}.

$$I_{in} = \frac{V_{in}}{R_{in} + R_{eq}//R_{ds}}. \tag{8}$$

R_{ds} represents the output resistance of M5 and M6. Transistors M7 and M8 together with the OTA form a G_m-boosting structure.

$$R_{eq} = \frac{1}{(1 + A_V)\, g_{m7,8}}. \tag{9}$$

A_V stands for the voltage gain of the OTA. The OTA is implemented using a recycling folded cascode amplifier[6]. Compared to the traditional folded cascode amplifier, it provides a larger GBW with the same current. A 60 dB gain within the signal bandwidth will lower the R_{eq} small enough and hence achieve a good linearity.

The proposed input resistor array is carefully designed to provide a 54 dB control range with less than 0.1 dB error. As shown in Fig. 2, it is a parallel combination of two subnetworks: one is composed of a parallel unit resistor while the other is of series one. Except for providing conventional attenuation, the resistor array has some other advantages in optimizing the gain step accuracy. Generally, the resistance of the parallel network is low, providing small attenuation, and the series one provides large attenuation. But the accuracy problem suffers from the on-resistance of switches, especially for the small attenuation situation. Since the total resistance is low then, the switch resistance may be large enough compared with the input array. It hence introduces great errors in the gain step accuracy, which may be as large as 0.5 dB. In order to satisfy the accuracy requirement, both parallel and series networks are used. The parallel network provides the main attenuation while the series network functions as a fine tuning module on the gain. As Equation (10) shows, if R_{seri} is fairly large compared to R_{para}, a great change in R_{seri} will only lead to a tiny variation in R_{in}. In this design, 6 dB variation in R_{seri} corresponds to a variation of around 0.1 dB in R_{in}.

$$R_{in} = R_{seri}//R_{para}. \tag{10}$$

Furthermore, the single sideband performance like image rejection ratio (IRR) also benefits from the resistor array. The resistor array can compensate for the non-ideal effect in manufacture and layout with a 0.1 dB step and hence the IRR can be reduced to a very low level.

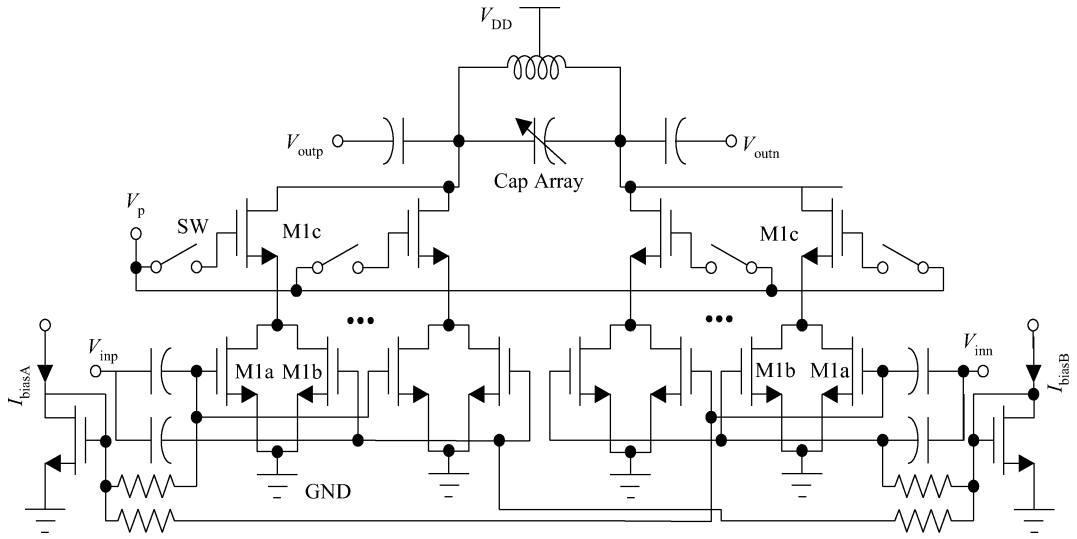

Fig. 3. Driver amplifier.

Besides the gain control requirement, the noise is also a tough challenge for low power design. The major noise contributor is the bias transistors of M5 and M6, which contribute about 80% of the total noise. This is proportional to the g_m since $i_{ds}^2 = 4KTg_m$. Lower noise is achieved by a smaller W/L ratio hence a larger overdrive voltage. Under the 1.2 V supply voltage, the drain voltage of M5 can be only around 250 mV. So the W/L ratio of M5 cannot be too small, which will drive the current source into the linear region. Another contributor is the switch pair, which contributes noise during the transition time from on to off. One convenient solution is to shorten the transition time, which requires a strong clock signal.

3.2. Driver amplifier

The driver amplifier is focused on the good linearity with relatively low ACLR, especially for a large output signal. It is realized by cancelling the IM3 product at a large output power. It also provides a gain control range of 12 dB.

The structure of the driver amplifier is shown in Fig. 3. It is a class AB amplifier realized using the parallel AB structure[7]. Compared to traditional class AB amplifier, the structure can provide linearity optimization over a specific input region and hence be more flexible.

The amplifier is sliced into a number of identical cells to provide different gains. For high gain mode, all slices are turned on and consume the largest power. For the other gain settings, some of the slices are shut down. To achieve a 6 dB gain control step with a small step error, careful simulation is done to decide on the number of slices.

The input transistor is divided into two parts, Ma and Mb, with different DC biases.

$$I = I_{dc} + G_m v_{gs} + \frac{G_m'}{2!} v_{gs}^2 + \frac{G_m''}{3!} v_{gs}^3 + \cdots, \qquad (11)$$

where $G_m = \frac{dI}{dV_{gs}}$, $G_m' = \frac{d^2I}{d^2V_{gs}}$, $G_m'' = \frac{d^3I}{d^3V_{gs}}$.

Equation (11) and Figure 4 show the Taylor expansion of the I–V characteristic of a transistor. The coefficient of the 3rd order term, G_m'', toggles from negative to positive with different DC biases.

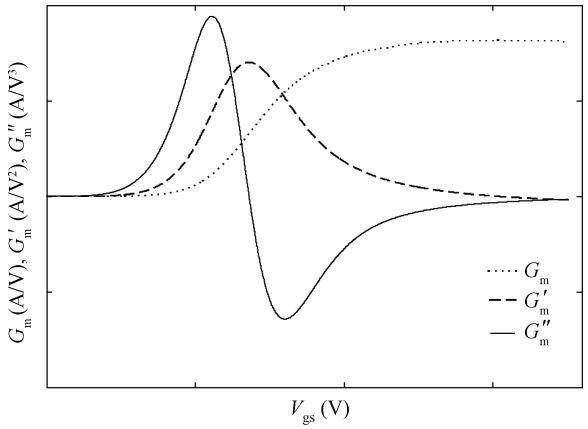

Fig. 4. Expansion coefficient versus bias voltage.

With careful design on the bias voltage and W/L aspect ratio, IM_3 generated from Ma could be cancelled out by the one from Mb and reduce the IM_3 to a very tiny value at a certain bias region. Usually, one is biased near the Class A region while the other is biased near the Class AB or Class C region[7].

In order to deliver 5 dBm of output power, the supply voltage is chosen to be 3.3 V. The cascade transistor Mc improves the reverse isolation and functions as a switch to control the activity of each slice. Considering the RF signal is around 2 GHz, the gate length of input transistor is chosen to be the minimum value of the process and the cascade transistor is a thick oxide transistor.

4. Experimental results

The designed transmitter has been fabricated by a 0.13 μm CMOS process. The die area is 2.2 × 1.3 mm^2. A micrograph of the complete transmitter IC is shown in Fig. 5.

Both single tone and two-tone measurement are adopted to evaluate the chip performance. The system specifications specified in the protocol are also measured by applying a QPSK modulated signal as the input.

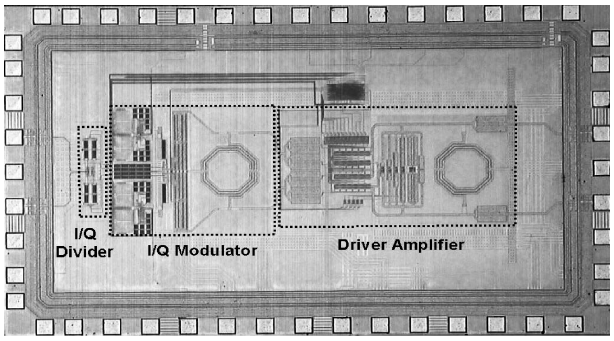

Fig. 5. WCDMA transmitter chip micrograph.

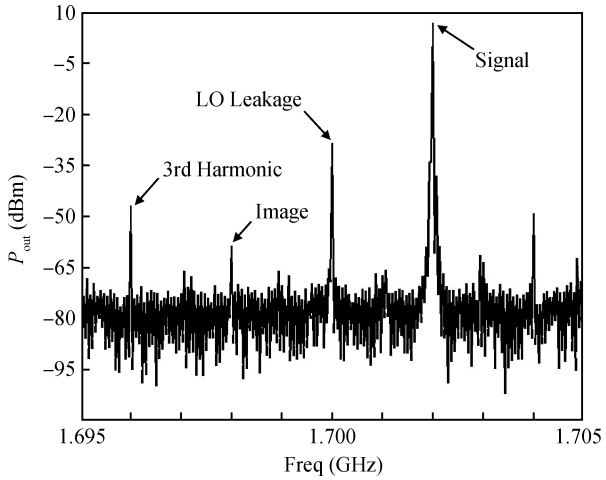

Fig. 6. Measured single sideband performance.

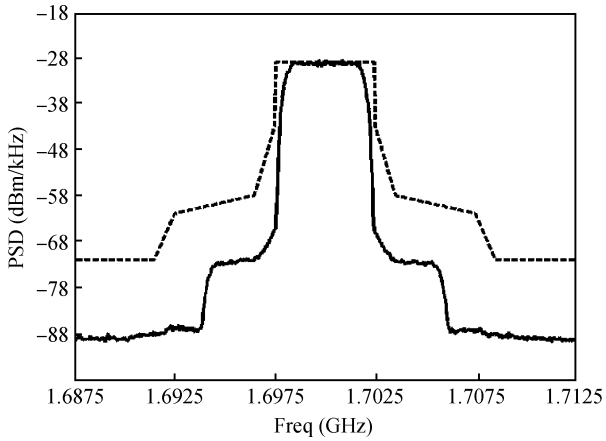

Fig. 7. Measured WCDMA output signal versus UMTS emission mask.

Figure 6 shows the output spectrum of the single sideband test. The output power is 6.8 dBm and the image is –55 dBm. The IRR can be kept below –47 dBc for the entire output range. The LO leakage is around –30 dBm and will be smaller when the gain of the driver amplifier becomes smaller.

Figure 7 shows the WCDMA output signal together with the UMTS emission mask. The measured adjacent channel leakage ratio is −44 dBc at 5 MHz offset when delivering 6.8 dBm output power, leaving 11 dB headroom for the external PA. The measured OIP3 is more than 19 dBm, indicating good linearity.

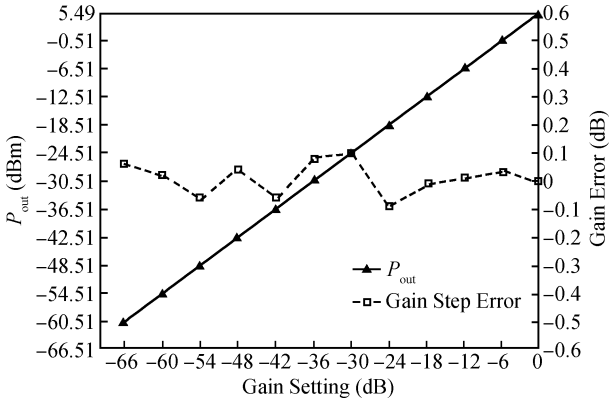

Fig. 8. Measured gain step accuracy versus gain setting.

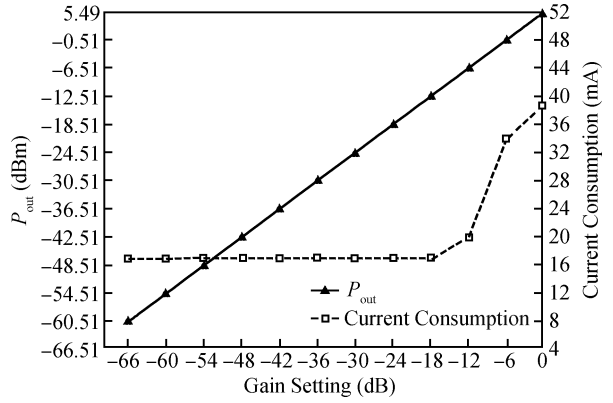

Fig. 9. Current consumption versus gain setting.

The gain step error with different gain settings is shown in Fig. 8. With the help of the fine tuning input resistor bank, the step error is kept under 0.1 dB covering the 66 dB control range, which shows good gain accuracy. Figure 9 shows the current consumption of the whole system.

The summary for the chip performance is shown in Table 1. A comparison with two similar circuits is also presented.

5. Conclusion

A linearly high output power transmitter for WCDMA is presented. The system adopts multi-gate techniques to optimize linearity at large output power and hence achieves a good ACLR with −44 dBc at 6.8 dBm. When the power is back-off, the ACLR will drop below −50 dBc, which indicates good linearity and leaves large headroom for the external PA. The system also achieves 3.7% EVM at the maximum output power. A 66-dB dynamic range with a 6 dB step gain control function is realized and the step accuracy is within 0.1 dB, thanks to the specific designed resistor array. The image rejection ratio is below −47 dBc for the entire output range and the LO leakage is −37 dBc @ 6.8 dBm output power.

References

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Table 1. Performance summary and comparison.

Parameter	Ref. [5]	Ref. [8]	This work
Technology	130 nm CMOS	180 nm SiGe BiCMOS	130 nm CMOS
Supply voltage (V)	1.5	1.8	1.2/3.3
Max output power (dBm)	2.5	0	6.8
ACPR @ 5 MHz (dBc@dBm)	−38 @ 2.5	−38 @ 0	−44 @ 6.8
EVM (%)	4.3	5	3.7
LO leakage (dBc@dBm)	−35 @ 2.5	−38	−37 @ 7
Image (dBc)	−38	—	−47
OIP3 (dBm)	19	—	19.2
Power (mA@dBm)	45 @ 2.5 (LPF included)	53 @ 0	38 @ 7

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