Modeling and characterization of shielded low loss CPWs on 65 nm node silicon*

Wang Hongrui(王洪瑞)†, Yang Dongxu(杨东旭), Zhang Li(张莉), Zhang Lei(张雷), and Yu Zhiping(余志平)

Institute of Microelectronics, Tsinghua University, Beijing 100084, China

Abstract: Coplanar waveguides (CPWs) are promising candidates for high quality passive devices in millimeter-wave frequency bands. In this paper, CPW transmission lines with and without ground shields have been designed and fabricated on 65 nm CMOS technology. A physical-based model is proposed to describe the frequency-dependent per-unit-length L, C, R and G parameters. Starting with a basic CPW structure, the slow-wave effect and ground-shield influence have been analyzed and incorporated into the general model. The accuracy of the model is confirmed by experimental results.

Key words: CMOS; CPW; shield; model
DOI: 10.1088/1674-4926/32/6/064009 **EEACC:** 1310

1. Introduction

In recent years, there has been an increased interest in the design of SiGe and CMOS circuits for millimeter-wave (mm-wave) applications, such as high-speed wireless communications at 60 GHz and automobile radar at 24 GHz and 77 GHz[1]. The passive devices used for impedance matching networks, power combiners and dividers, and filters are essential in RF systems. On-chip transmission lines with a well-defined current return path and good length-scalability become more and more attractive in mm-wave circuit design.

From the perspective of a circuit designer, the main concerns on a transmission line are mainly characteristic impedance (z_c), electrical wavelength (λ) or phase constant (β), and quality factor (Q). Compared with microstrip lines, which usually have a low z_c due to limited distance between the top and lowest metal, coplanar waveguides (CPW) have a larger z_c because the gap between the signal and ground metals can be adjusted to a large extent. Wavelength is also a issue in terms of chip area occupation. Slow wave technique is introduced to reduce wave velocity and correspondingly increase the phase shift at a given line length and frequency[2, 3]. It can be implemented by inserting periodical metal slots beneath CPW lines. Quality factor is one of the important parameters for RF and mm-wave designs because it is directly related to insertion loss, noise figure and signal distortion. In deep submicrometer CMOS processes, standard coplanar waveguides typically suffer from losses as high as 1–2 dB/mm at 10 GHz, due largely to dielectric loss effects in the low-resistivity silicon substrate. Several substrate shielding methods for passive devices, such as transmission lines, inductors and transformers, have been developed to suppress the penetration of electric fields into the silicon substrate[4]. However, at the same time, these metal shields introduce additional conductive losses due to an eddy current effect and an increased per-unit-length capacitance, leading to a low characteristic impedance and quality factor.

In this work, a physical-based model for three types of transmission line, including basic CPW, floating-slot slow-wave CPW (FSCPW), and grounded CPW (GCPW) is presented, taking into account the slow wave effect, ground shield influence and skin effect. The model has been validated through experiments on CMOS 65 nm technology.

2. BEOL and CPW structure description

The on-chip transmission lines are fabricated in 65 nm bulk CMOS technology. The substrate is 200-μm-thick silicon with a resistivity of about 10 Ω·cm. The back end of the process has seven copper metal layers (5 thin + 2 thick), as shown in Fig. 1(a). The dielectric material SiO_2 is filled between the metal layers. An ultra thick top metal (UTM) with a thickness of 3.4 μm and a distance of 4.6 μm from the substrate can be utilized to implement low loss passive devices and the lowest metal m1 is used as shield. Three types of CPW are designed using this top metal, as shown in Fig. 2 and their die photographs are shown in Fig. 1(b).

(a) Basic CPW. Normal CPW without shields.

(b) Floating slot slow-wave CPW (FSCPW). Periodical slot-type metal shields are arranged beneath the CPW at a direction orthogonal to the current-flowing direction in the signal conductor.

(c) Grounded CPW (GCPW). Mesh-type ground shield using m1 is placed under the CPW line. The ground shield is connected to the side ground conductor with metals and vias to form a half-surrounded structure.

3. Analytical model for on chip CPWs

The derivation of the CPW model is based on a quasi-TEM assumption, which is valid up to a hundred giga Hz[5]. So the transmission line can be fully characterized by its frequency dependent per-unit-length R, L, G, C parameters. Based on

* Project supported by the State Key Development Program for Basic Research of China (No. 2010CB327404).
† Corresponding author. Email: hr-wang06@mails.tsinghua.edu.cn
Received 31 December 2010, revised manuscript received 15 February 2011

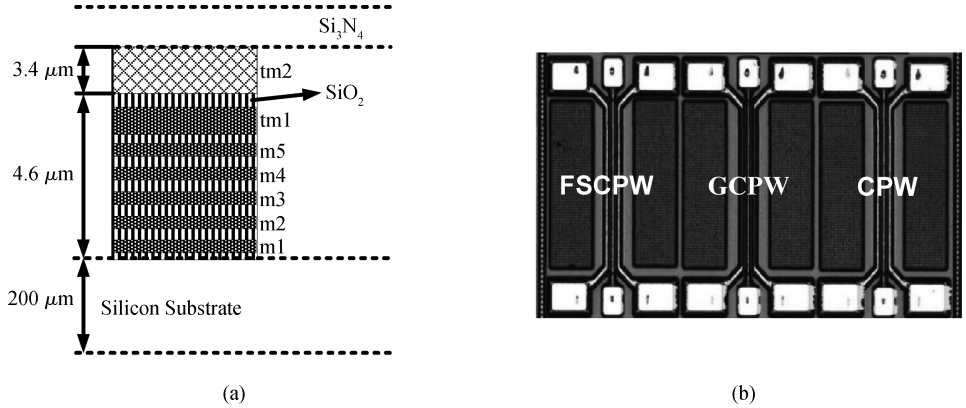

Fig. 1. Fabrication illustration. (a) Simplified cross section of 65 nm technology stack. (b) Chip photographs of the three types of fabricated CPWs.

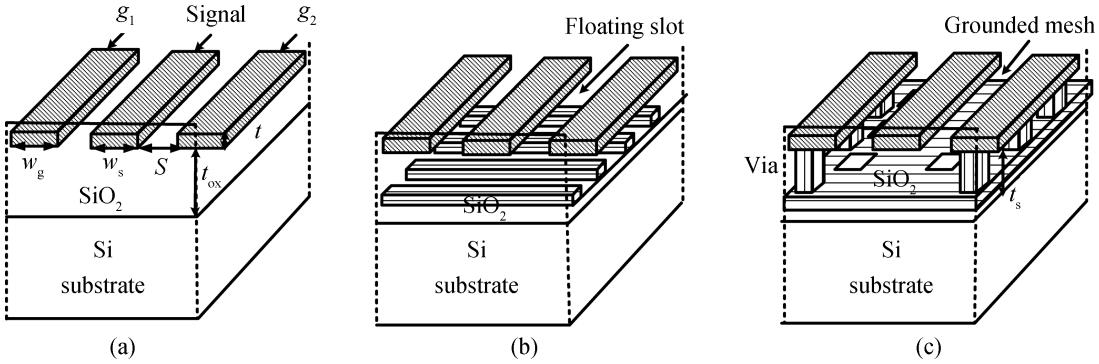

Fig. 2. CPW transmission line structures. (a) Basic CPW. (b) Floating slot slow-wave CPW (FSCPW). (c) Grounded CPW (GCPW).

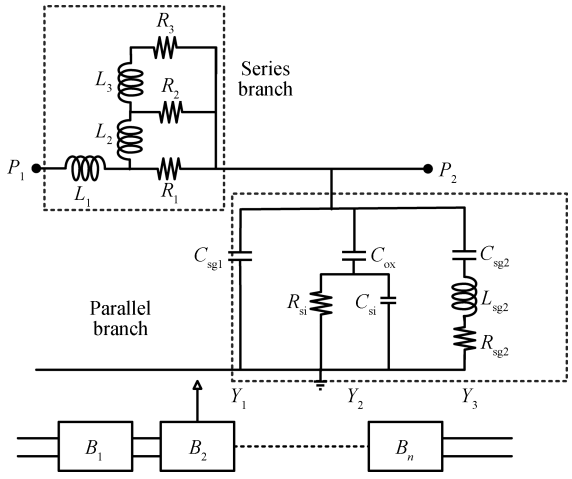

Fig. 3. The proposed CPW equivalent circuit model.

this observation, we propose our model as a number of cascaded blocks, each of which is comprised with a series branch and a parallel branch, as shown in Fig. 3.

3.1. Basic CPW

3.1.1. Series branch

The series branch is comprised of an L_1 and an R–L ladder to describe both DC and high frequency series inductance and resistance. The partial inductance concept is used to collect the total per-unit-length L:

$$L_{\mathrm{dc}} = L_{\mathrm{s}} + 2\left(\frac{L_{\mathrm{g1}}}{4}\right) - 4\left(\frac{M_{\mathrm{sg1}}}{2}\right) + 2\left(\frac{M_{\mathrm{g1g2}}}{4}\right), \quad (1)$$

where L_i denotes self-partial inductance and M_{ij} represents the mutual partial inductance between conductor i and j. The per-unit-length self and mutual inductances can be calculated by simplified Greenhouse formulas (2) and (3), which have been validated for rectangular planar inductors[6].

$$L = 2l\left(\ln\frac{2l}{w+t} + 0.5 + \frac{w+t}{3l}\right), \quad (2)$$

$$M = 2l\left(\ln\frac{2l}{\mathrm{GMD}} - 1 + \frac{\mathrm{GMD}}{l}\right), \quad (3)$$

where l is the length of the CPW, w and t are width and thickness of the conductor, and GMD is the geometric mean distance between two conductors[6]. The per-unit-length DC resistance can be obtained by the following expression, where σ_{m} is the metal conductivity.

$$R_{\mathrm{dc}} = \frac{l}{\sigma_{\mathrm{m}} w_{\mathrm{s}} t} + \frac{l}{2\sigma_{\mathrm{m}} w_{\mathrm{g}} t}, \quad (4)$$

where w_{s} and w_{g} are the width of signal and ground conductor, and t is the thickness of the top metal. At high frequencies, both the skin effect and the proximity effect will push the current to the edges of the conductors, leading to a higher resistance and lower inductance. The inductance approaches a limit at an

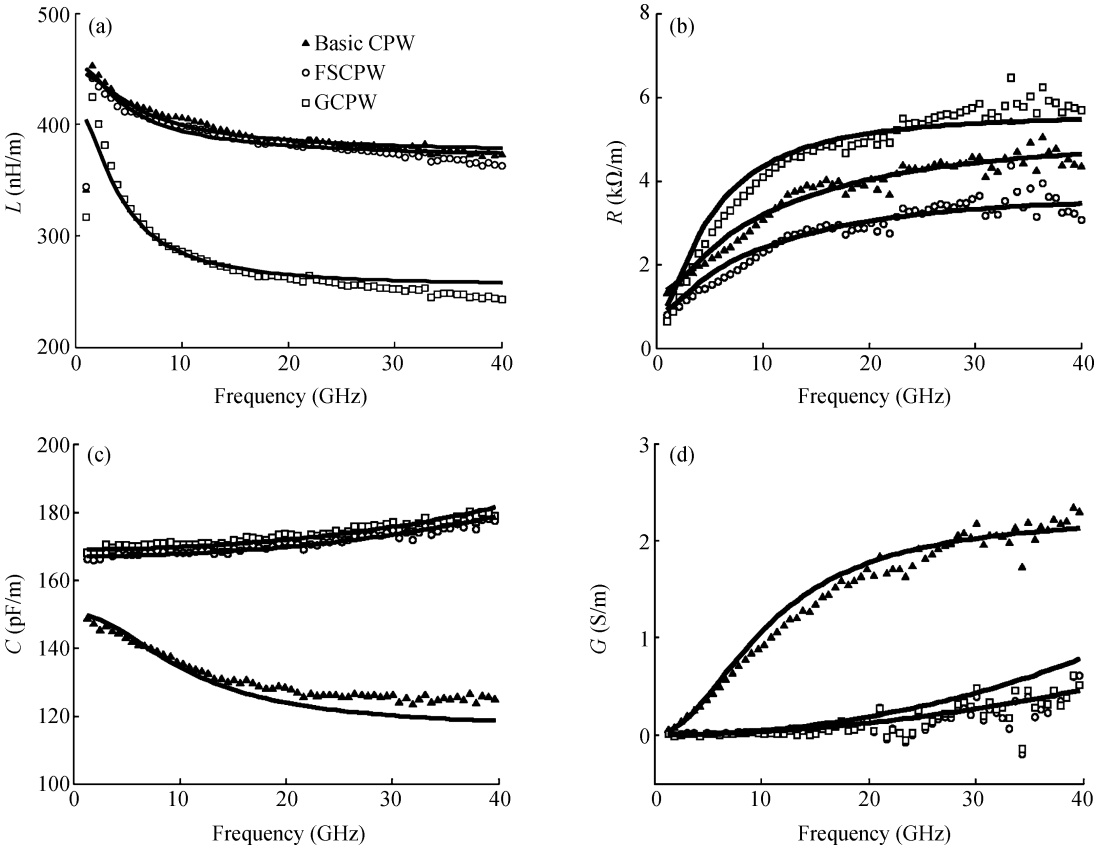

Fig. 4. Comparison between the experimental data (symbol) and the proposed model (line) of per-unit-length parameters. (a) L. (b) R. (c) C. (d) G.

infinite frequency while the resistance will increase continually with a square-root relationship with frequency. The R and L of a rectangular conductor at the maximum operation frequency ($f_{\max}$) can be calculated by the following expression:

$$R_{\rm hf} = \frac{l}{2t\sigma\delta_{\max}}, \quad \delta_{\max} = \sqrt{\frac{1}{\pi\mu\sigma f_{\max}}}, \tag{5}$$

$$L_{\rm hf} = L_{\rm dc} - L_{\rm int}, \tag{6}$$

where $L_{\rm int}$ is the internal inductance, which can be calculated by the empirical polynomial expression proposed in Ref. [7].

After both the DC and high frequency values are obtained, a ladder network is constructed to model the frequency dependence of L and R. The components of the network can take the following relationship:

$$K_{\rm RP} = R_3/R_2 = R_2/R_1, \tag{7}$$

$$K_{\rm LP} = L_3/L_2. \tag{8}$$

As pointed by Kim[8], a ratio of 0.315 between $\frac{L_{\rm int}}{L_1}$ and $\frac{R_1}{R_{\rm dc}}$ is chosen. The remaining parameter can then be determined.

3.1.2. Parallel branch

The parallel branch contains three admittance parts:

Y_1: capacitance between the signal and side ground conductors $C_{\rm sg1}$.

Y_2: capacitance between the signal conductor and the ground shield $C_{\rm sg2}$ in series with shielding resistance $R_{\rm sg2}$ and inductance $L_{\rm sg2}$.

Y_3: capacitance between the signal conductor and the substrate $C_{\rm ss}$ in series with substrate capacitance $C_{\rm si}$ and resistance $R_{\rm si}$.

For basic CPW without shield, we need only consider Y_1 and Y_3. $C_{\rm sg1}$ is calculated by adding capacitance between the metal sidewalls to the zero-thickness capacitance, which can be obtained by conformal mapping[9]. The Y_3 part, which is a C–R–C oxide-substrate three element model, has been widely studied. It is calculated by the method proposed by Zheng[10].

3.2. FWCPW

3.2.1. Series branch

Floating shields do not carry conduction current because they are arranged as floating slots orthogonal to the wave direction. So the magnetic distribution is the same as that of the basic CPW.

3.2.2. Parallel branch

Unlike basic CPWs, it has additional coupling from signal conductor to the ground shield metal. The coupling capacitance is obtained by the formula proposed by Meijs and Fokkema[11].

$$C_{\rm sg2} = \varepsilon_0\varepsilon_{\rm r}\left\{\frac{w_{\rm s}}{t_{\rm s}} + 0.77 + 1.06\left[\left(\frac{w_{\rm s}}{t_{\rm s}}\right)^{0.25} + \left(\frac{t}{t_{\rm s}}\right)^{0.5}\right]\right\}, \tag{9}$$

where $t_{\rm s}$ is the thickness of the dielectric between the top metal and the shielding metal, and t is the thickness of the top metal. It is observed in experimental data that for FSCPW

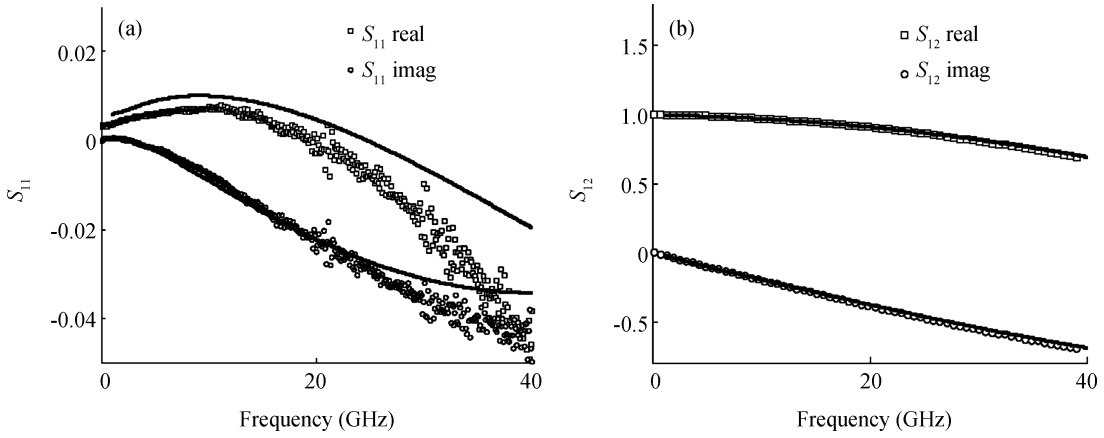

Fig. 5. Measured (a) phase constant and (b) attenuation loss.

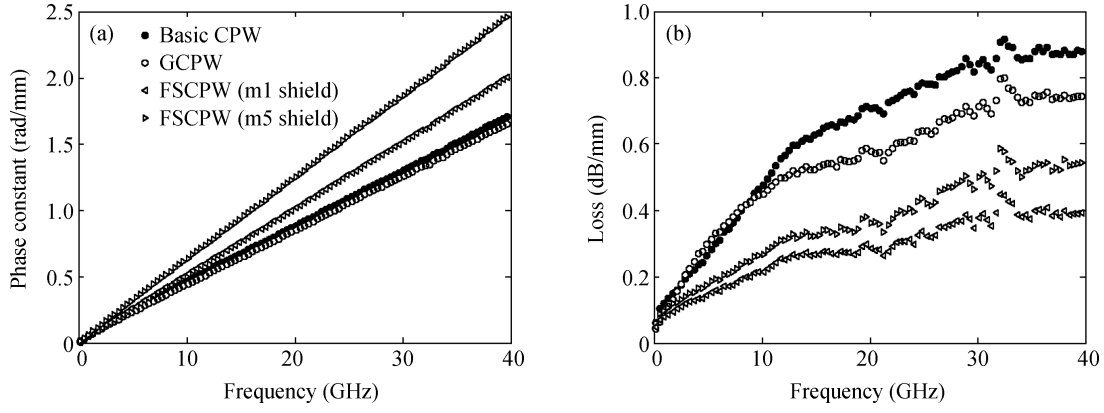

Fig. 6. Measured (a) quality factor and (b) characteristic impedance.

and GCPW, the per-unit-length capacitance slightly increases with frequency, which is different from basic CPWs. It may be caused by the small inductance along the narrow shielding metal strips. Here we model the strip inductance and resistance with semi-empirical expressions as $L_{sg2} = \mathrm{kl}\cdot\mathrm{fl}/(\mathrm{fw}\cdot\mathrm{ft})$, $R_{sg2} = \mathrm{kr}\cdot\mathrm{fl}/(\mathrm{fw}\cdot\mathrm{ft})$, where kr and kl are empirical parameters, fl, fw and ft are the length, width and thickness of the metal strip.

In fact, due to incomplete shielding provided by the metal slots, there is still a part of the electric lines of force entering the substrate. Therefore, the effective admittance is a weighted average between Y_2 and Y_3.

$$(Y_2 + Y_3)_{\mathrm{eff}} = \eta^{\alpha} Y_2 + (1-\eta)^{\alpha} Y_3, \tag{10}$$

where $\eta = \mathrm{fw}/(\mathrm{fw}+\mathrm{fs})$ is the duty cycle of the metal slots and α is a empirical parameter.

3.3. GCPW

3.3.1. Series branch

Unlike the FWCPW, the ground shield will conduct current and affect the effective inductance and resistance. Therefore, the shielding conductor g_3 should be taken into account.

$$L_{\mathrm{dc}} = L_{\mathrm{s}} + \sum_{i=1}^{3} k_{\mathrm{g}i}^2 L_{\mathrm{g}i} - 2\sum_{i=1}^{3} k_{\mathrm{g}i} M_{\mathrm{sg}i} + 2\sum_{i=1}^{3}\sum_{j=1}^{i-1} k_{\mathrm{g}i} k_{\mathrm{g}j} M_{\mathrm{g}i\mathrm{g}j}, \tag{11}$$

where $k_{gi} = A_{gi} / \sum_{i=1}^{3} A_{gi}$, A_{gi} is the area of cross section of the conductor g_i.

3.3.2. Parallel branch

The capacitive coupling between the signal and ground shield, and the substrate of the GCPW is similar to FSCPWs. So the calculation method for FSCPWs also applies here.

4. Experimental validation

The designed structures have been fabricated on 65 nm technology. Open-short de-embedding techniques have been applied to these measurement data to eliminate the influence of probe pad parasitics and to extract the intrinsic CPW line characteristics. Then, the S parameters are converted to an ABCD-parameter. The characteristic impedance and propagation constant are calculated from ABCD parameters. Next, the per-unit-length parameters L, R, C and G are extracted. Thus, these measured parameters are compared to those obtained by our proposed model, as shown in Fig. 4. All the lines have a length of 400 μm. A comparison of the S parameters of the FSCPW is shown in Fig. 5. The basic CPW line has a signal/ground width of 10 μm / 20 μm, with a 10 μm gap while the other types have a signal/ground width of 10 μm / 45 μm, with the same gap. The floating metal has a length/width/gap of 120 μm / 1 μm / 1 μm. It can be seen that the model fits the measured data well up to 40 GHz.

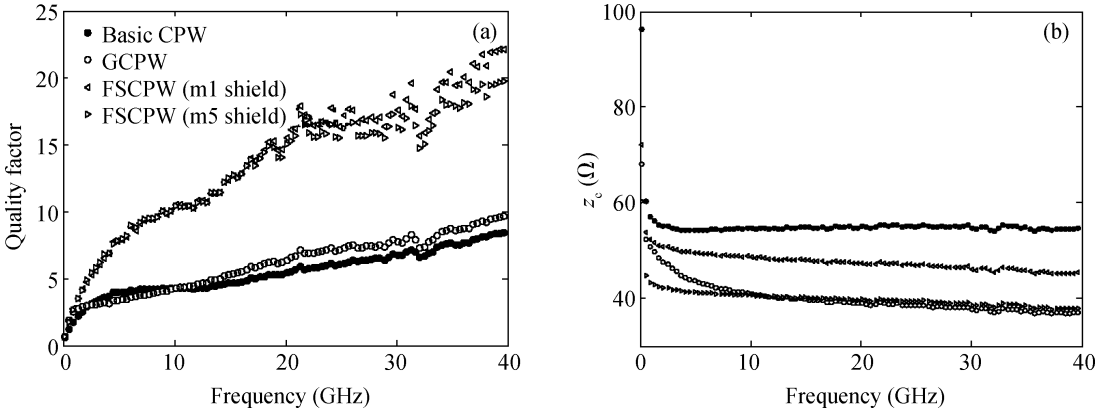

Fig. 7. Comparison between the measured S parameters (symbol) and modeled (line) (a) S_{11} and (b) S_{12}.

In addition, the performance differences between different structures are compared and analyzed. Figure 6(a) shows the measured phase constant versus frequency. Compared with a basic CPW, the slow wave CPW increased β about 33% with m1 as floating shield, and further improved about 66% with m5 as floating shield. The attenuation loss is 0.9 dB/mm, 0.75 dB/mm, 0.58 dB/mm, and 0.39 dB/mm for the basic CPW, GCPW, FSCPW(m5 shield) and FSCPW(m1 shield) at 40 GHz, respectively, as shown in Fig. 6(b). Quality factor, which is defined as $\beta/2\alpha$, is a fairer merit with which to judge the overall tradeoff between attenuation loss and the effective permittivity constant. As shown in Fig. 7(a), the floating shield improves the quality factor from 9 to 23 at 40 GHz, while the grounded shield only improves it slightly, at about 10%. Using m1 as shield shows better performance than m5 at higher frequency. Finally, as expected, there is a slight reduction of characteristic impedance for FWCPWs and GCPWs due to more capacitive coupling (Fig. 7(b)). However, this degradation can be compensated by making the gap between the signal and ground conductors larger.

5. Conclusion

A systematic methodology for modeling integrated CPW on silicon substrate up to millimeter wave frequencies is presented. The model is built on physical mechanisms, taking into account of skin effect, slow wave effect, substrate coupling and ground shielding influence. The values are obtained based on geometric and technology parameters. The CPW structures with and without ground shields were fabricated on 65 nm technology. Good agreement is observed when the experimental data is compared to the model. In addition, the experimental results show that CPW lines with floating shields can improve the quality factor by about 150%, wave constant 30% to 60%, with only about a 10% decease in characteristic impedance.

Acknowledgment

The authors would like to thank SMIC for chip fabrication and measurements.

References

[1] Komijani A, Hajimiri A. A wideband 77-GHz, 17.5-dBm fully integrated power amplifier in silicon. IEEE J Solid-State Circuits, 2006, 41(8): 1749

[2] Kim W, Swaminathan M. Characterization of co-planar silicon transmission lines with and without slow-wave effect. IEEE Trans Adv Packag, 2007, 30(3): 526

[3] Lai I C H, Fujishima M. High-Q slow-wave transmission line for chip area reduction on advanced CMOS processes. Proc IEEE-ICMTS, 2007:192

[4] Mangan A M, Voinigescu S P, Yang M T, et al. Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits. IEEE J Solid-State Circuits, 2006, 41(5): 1183

[5] Sayag A, Ritter D, Goren D. Compact modeling and comparative analysis of silicon-chip slow-wave transmission lines with slotted bottom metal ground planes. IEEE Trans Microw Theory Tech, 2009, 57(4): 840

[6] Greenhouse H M. Design of planar rectangular microelectronic inductors. IEEE Trans Parts Hybrids Packag, 1974, PHP-10(2): 101

[7] Chen H, Fang J. Modeling of impedance of rectangular crosssection conductors. Proc IEEE Conf Electr Performance Electron Packag, 2000: 159

[8] Kim S, Neikirk D P. Compact equivalent circuit model for the skin effect. Proc IEEE MTT-S Int Microw Symp Dig, 1996, 3: 1815

[9] Milanovi V, Ozgur M, DeGroot D C, et al. Characterization of broad-band transmission for coplanar waveguides on CMOS silicon substrates. IEEE Trans Microw Theory Tech, 1998, 46(6): 632

[10] Zheng J, Hahm Y C, Tripathi V K, et al. CAD-oriented equivalent-circuit modeling of on-chip interconnects on lossy silicon substrate. IEEE Trans Microw Theory Tech, 2000, 48(9): 1443

[11] Meijs N V D, Fokkema J T. VLSI circuit reconstruction from mask topology. Integration, 1984, 2(2): 85