A sub-sampling 4-bit 1.056-GS/s flash ADC with a novel track and hold amplifier for an IR-UWB receiver*

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Abstract: A sub-sampling 4-bit 1.056-GS/s flash ADC with a novel track and hold amplifier (THA) in 0.13 μm CMOS for an impulse radio ultra-wideband (IR-UWB) receiver is presented. The challenge is in implementing a sub-sampling ADC with ultra-high input signal that further exceeds the Nyquist frequency. This paper presents, to our knowledge for the second time, a sub-sampling ADC with input signals above 4 GHz operating at a sampling rate of 1.056 GHz. In this design, a novel THA is proposed to solve the degradation in amplitude and improve the linearity of signal with frequency increasing to giga Hz. A resistive averaging technique is carefully analyzed to relieve noise aliasing. A low-offset latch using a zero-static power dynamic offset cancellation technique is further optimized to realize the requirements of speed, power consumption and noise aliasing. The measurement results reveal that the spurious free dynamic range of the ADC is 30.1 dB even if the input signal is 4.2 GHz sampled at 1.056 GS/s. The core power of the ADC is 30 mW, excluding all of the buffers, and the active area is 0.6 mm^2. The ADC achieves a figure of merit of 3.75 pJ/conversion-step.

Key words: flash ADC; sub-sampling; track and hold amplifier; resistive averaging technique; comparator; IR-UWB

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1. Introduction

Recent advances in wireless communication technologies have had a transformative impact on society and have directly contributed to several economic and social aspects of daily life[1]. The UWB system marks a major milestone in this progress. Since 2002, when the Federal Communication Commission (FCC) allowed the unlicensed use of UWB radio signals with low-power spectral density (–41.25 dBm/MHz) in the range of 3.1–10.6 GHz, UWB technology has again received great interest[1].

Low resolution giga sample/second ADCs are extensively used in wireless communication systems, such as UWB systems[2]. The most traditional architecture is supporting the multi band orthogonal frequency division multiplexing (OFDM) approach, such as in Fig. 1(a), which results in considerable complexity and power consumption in their implementation. The proposed sub-sampling IR-UWB receiver is shown in Fig. 1(b), which reveals obvious advantages in implementing cost and power-efficiency. In Fig. 1(b), there is no mixer in the UWB receiver, and the ADC down samples RF signals into digital code directly for baseband processing, which is a great challenge for the ADC with an ultra-high input signal. The process of sampling the input signal at a rate lower than the highest frequency components of the input signal, commonly referred to as sub-sampling, performs a function equivalent to that of mixing. In recent published works, there has been little research on the sub-sampling technique, which increases the difficulty of the work severely. Moreover, the THA in an ultra-high speed flash ADC always occupies most of the power consumption. It seems that few people have a good idea for dealing with this problem.

This paper gives the architecture of a flash ADC and discusses circuit design including a resistive averaging network, an interpolation technique, and a comparator array, especially the proposed THA.

2. Architecture

The simplified block diagram of the flash ADC in this work is shown in Fig. 2. A high pass filter (HPF) eliminates

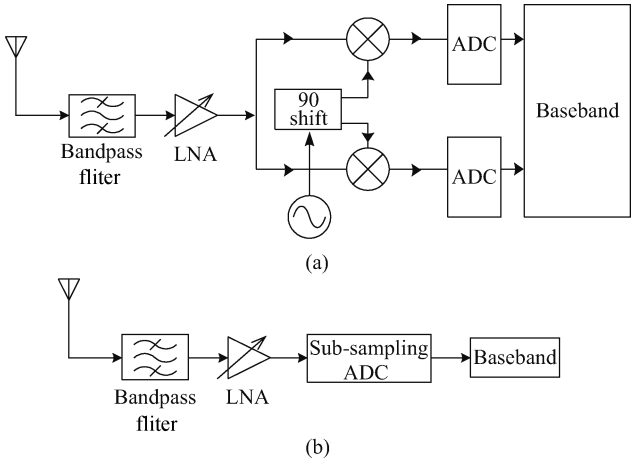

Fig. 1. UWB receiver architecture. (a) Traditional architecture. (b) Sub-sampling architecture.

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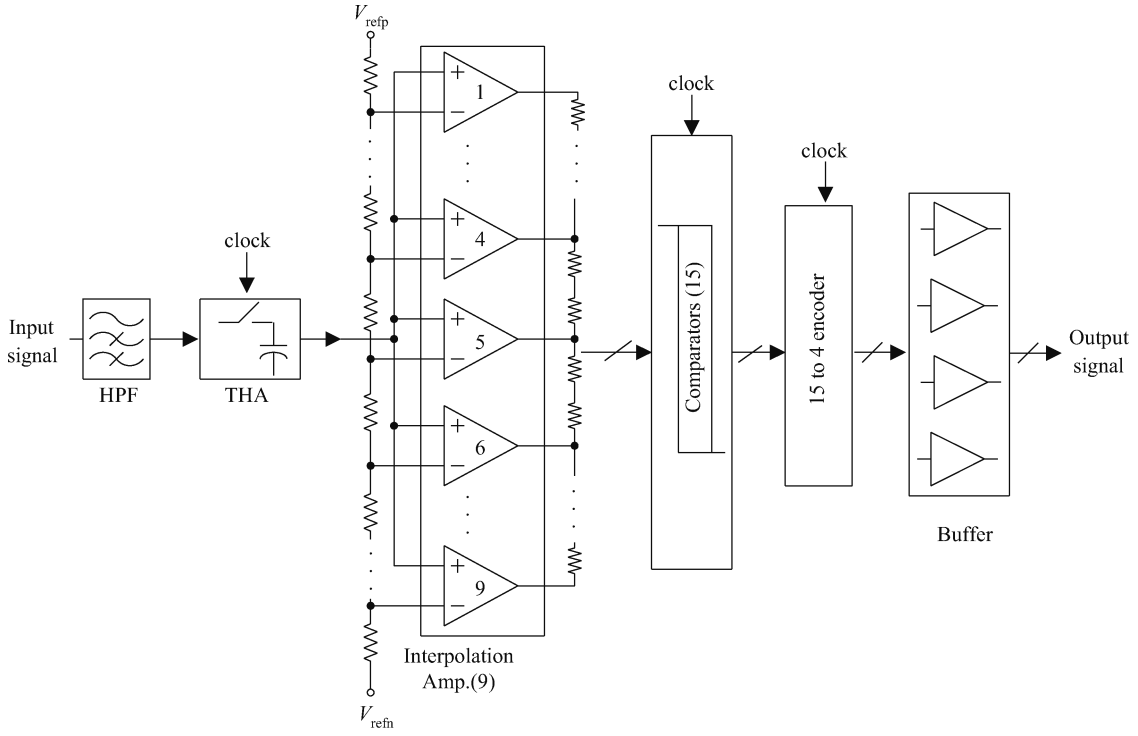


Fig. 2. Architecture of the ADC in this work.

the low frequency input signal and isolates the input signal to the THA. The performance of the HPF influences the input signal to some extent. The main design difficulty is to guarantee little degradation of the input signal in linearity. Due to the sub-sampling architecture, the THA is essential to hold the ultra-high frequency input signal. Then the input signal amplifies two times by nine preamplifiers in the interpolation network. Meanwhile, the resistive averaging technique is inserted into the interpolation network to relieve the random offset from noise aliasing. The interpolation technique reduces about half of the preamplifiers compared with its traditional counterpart. The first and the last preamplifiers in Fig. 2 are dummy ones to overcome the boundary threshold offset largely though it increases the power consumption of two preamplifiers. The output data of the comparator is thermal code, 15 to 4 encoder translates thermal code into binary code and buffer out.

The ultra-high speed ADC also has other architectures. For instance, Reference[3] gives a 500-MS/s 5-bit time-interleaved successive approximation register (SAR) ADC. However, the effective number of bits (ENOB) is less than 3 bits because increasing the number of time-interleaved channels is not favorable due to its random offset, timing mismatch and gain errors among channels. A 32-mW 1.25-GS/s 6-bit SAR ADC in 0.13 μm CMOS presented in Ref. [4] uses three capacitor network DACs to detect 2 bits per clock cycle. The hardware complexity has been greatly increased by about 3 times compared with normal SAR ADCs. A novel architecture in Ref. [5] reveals time-interleaved flash-SAR architecture, but it didn't give measurement results.

For the UWB system, it has already been demonstrated that only ADCs of 4 bits precision are sufficient for reception in both noise and interference limited regimes[3]. From Ref. [3], at 4 bits and below, the flash ADC architecture has better energy efficiency than its time-interleaved SAR counterpart. So we still insist on the traditional flash ADC in this work.

In Ref. [6], to our knowledge for the first time, a sub-sampling ADC with input signals above 4 GHz operating at a sampling rate of about 1 GHz. But Ref. [6] didn't give much consideration of the sub-sampling ADC. In this work, we analyze some problems in the sub-sampling structure. The most challenging part of the sub-sampling ADC is noise aliasing and square growth of phase noise on the sampling clock. The noise aliasing mainly results from the THA's ultra-high bandwidth until the input signal, which is proved to be about $2m$ larger than the Nyquist sample (here m is the rate of sub-sampling, defined as $m = f_{in}/f_s$, f_{in} is the input signal frequency, and f_s is the sampling clock frequency.). What's more, the sub-sampling technique worsens the impact of phase noise on the sampling clock. From Ref. [7], the phase noise power is amplified by m^2 due to the sub-sampling technique. In this ADC, $m = f_{in}/f_s = 4.2/1.056 = 4$, sampling a 4.2 GHz RF signal with a 1.056 GHz clock results in a 9 dB and 12 dB increase in noise aliasing power and phase noise power, respectively.

3. Circuit of flash ADC

3.1. Proposed THA with self-biased buffer

The noise aliasing mainly comes from the ultra-high bandwidth of the THA until to the input signal. The noise floor of the ADC is defined as

$$F_{NF} = -174\,\text{dBm} + \text{NF} + 10\lg \text{BW}. \quad (1)$$

BW is the bandwidth of the input signal 4.2 GHz, assuming that the noise figure (NF) of the system is about 20 dB. F_{NF} (noise floor) is –57 dBm (0.3 mV), a 9 dB increase compared

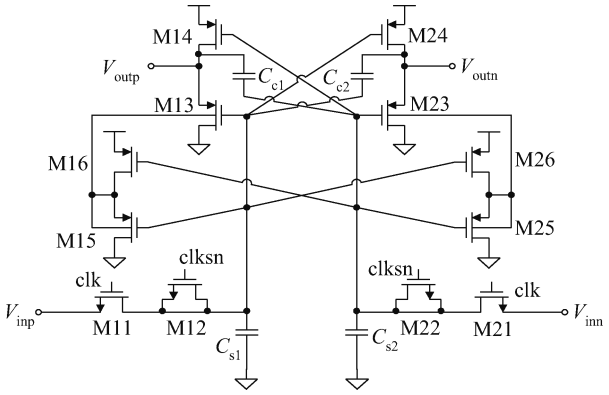


Fig. 3. Proposed THA with self-biased buffer.

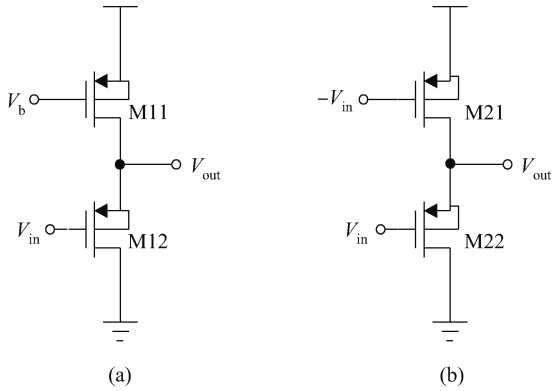


Fig. 4. (a) Traditional SF. (b) Proposed self-biased SF.

to the Nyquist type. The impact of phase noise equals the influence of clock jitter. To the ADC, the clock jitter should satisfy the formula

$$\Delta t < \frac{1}{2^{N+1}\pi f_{\text{in}}}. \tag{2}$$

N is the ENOB of the ADC. So $\Delta t < 2.3$ ps, which is the demand for the phase locked loop (PLL).

The THA is the most challenging part in sub-sampling the ADC. By holding the ultra-high speed analog sample, which further exceeds the sample clock static during digitization, the THA largely removes errors due to skews in clock delivery to a large number of comparators, limited input bandwidth prior to latch regeneration, signal-dependent dynamic nonlinearity, and the aperture jitter[8]. The proposed THA in this work is shown in Fig. 3.

The prototype of the proposed THA is from Ref. [9]. In the ultra-high speed THA, the most effective solution is a switch-capacitor scheme. The switches are implemented using single NMOS M11 M21. A MIM capacitor C_{s1} C_{s2} is used to hold the input signal. In an open-loop THA circuit, the trade-off between speed and accuracy often needs considerable attention. In the tracking mode, the THA acquisition time constant τ is given as

$$\tau = R_{\text{on}}C_{\text{s}} = \frac{C_{\text{s}}}{\mu_{\text{n}}C_{\text{ox}}(W/L)(V_{\text{GS}} - V_{\text{TH}})}, \tag{3}$$

where R_{on} is the turn-on resistance of the switch. Reducing the capacitance or increasing W/L can achieve a larger bandwidth. In the hold mode, the pedestal error ΔV_{P} due to the charge injection is given as

$$\Delta V_{\text{P}} = \frac{Q_{\text{ch}}}{2C_{\text{s}}} = \frac{WLC_{\text{ox}}(V_{\text{GS}} - V_{\text{TH}})}{2C_{\text{s}}}, \tag{4}$$

where Q_{ch} is the charge stored in the MOS transistor channel. This shows that the pedestal error can be reduced by increasing the capacitance just opposite the tracking mode.

To relieve the influence of charge injection, a dummy clock M12 M22 is placed in front of $C_{s1}C_{s2}$, respectively. M12 is half the size of M11 because about half of Q_{ch} is flow to the C_{s1} in the ultra-high situation.

In Ref. [9], the most fatal problem is the degradation in output signal due to the traditional source follower (SF). In Fig. 4(a), the gain of the traditional SF is

$$A_{\text{S.F.}} = \frac{g_{\text{m11}}R_{\text{o12}}}{1 + g_{\text{m11}}R_{\text{o12}}}. \tag{5}$$

If we want no degradation in signal, $g_{\text{m11}}R_{\text{o12}} \gg 1$ must be satisfied. In modern CMOS technology, SF always suffers severe degradation in amplitude due to limited gain. In most situations in flash ADC, the traditional SF is adopted and degradation in the signal will be made up in latter stage. This scheme will waste a large amount of power, especially in sub-sampling the ADC, which will consume $2m$ times (m is the sub-sampling rate mentioned above) power larger than the Nyquist ADC. To deal with this problem, we propose a novel SF with self-bias, as shown in Fig. 4(b). The gain of the proposed SF in Fig. 4(b) is

$$A_{\text{S.F.\_pro}} = \frac{g_{\text{m21}} + g_{\text{m22}}}{\dfrac{1}{R_{\text{o21}}} + \dfrac{1}{R_{\text{o22}}} + g_{\text{m21}}}. \tag{6}$$

In theory, if we set $g_{\text{m22}} = \frac{1}{R_{\text{o22}}} + \frac{1}{R_{\text{o21}}}$, which is easily realized in modern CMOS technology, there is no degradation in signal and we solve the problem in traditional SF.

The proposed SF will save about half of the power consumption in a traditional Nyquist ADC. Furthermore, in sub-sampling situations, the power consumption will decrease to $(1/4)m$ of the traditional counterpart.

Meanwhile, the output of small replica source followers M15 and M16 in Fig. 3 are used to bias the well of the main source followers M13. This has a linearity advantage over a SF with a well-to-source connection[9]. Moreover, it eliminates the load effect of the non-linear N-well capacitor of M13, which will worsen the bandwidth of the SF severely, especially in a sub-sampling situation. Capacitor C_{c} is replaced by a MOS transistor in reality, which relieves the random noise from the subsequent circuit. The simulation performance of the THA is shown in Fig. 5, which indicates that the ENOB of the THA circuit is still more than 8 bits even when the input signal reaches 4.8 GHz. Table 1 gives a comparison of the proposed THA with recently published work. From Table 1, the proposed THA shows obvious advantages in many ways, including effective resolution bandwidth (ERBW), power consumption and linearity.

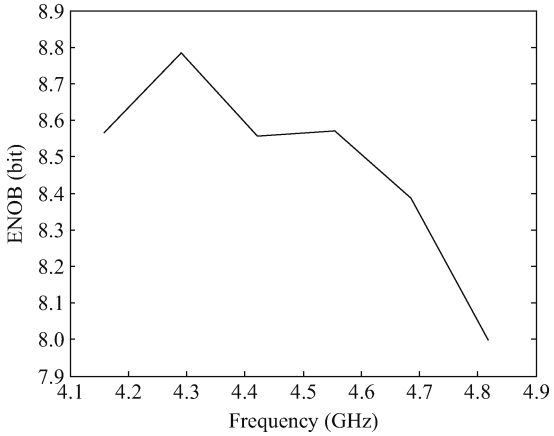


Fig. 5. ENOB of THA in the range of 4.1–4.8 GHz.

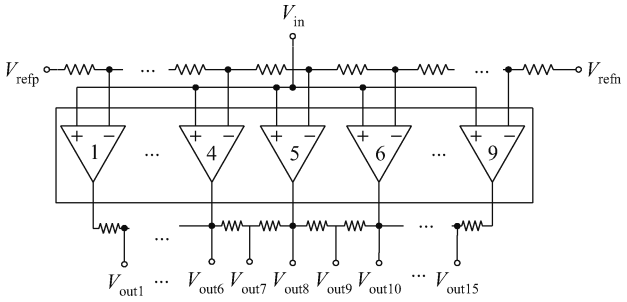


Fig. 6. Structure of preamplifier array.

Table 1. Comparison of proposed THA with others.

Ref.	Clock (GHz)	ERBW (GHz)	Power (mW)	SFDR (dB)
[10]	2	0.97	14.4	—
[11]	2	0.498	19.2	50.88
[4]	1.25	0.45	9.6	—
This work	1.056	4.2	6.5	54

3.2. Interpolation network and resistive averaging technique

Figure 6 gives the single-end structure of interpolation and resistive averaging network in this work and its differential form in the actual circuit. An interpolation network and resistive averaging technique are often used in flash ADC. The former is to reduce power consumption and the latter is to relieve random offset. However, there is always conflict between them. The interpolation is realized by inserting an extra reference between two adjacent preamplifiers, which reduces half of the power consumption of the preamplifier array. Reference [12] gives an optimum scheme between the interpolation network and the resistive averaging technique, and the gain of the pre-amplifier is set about 2. Due to the noise aliasing from the THA, the noise floor increases by about 9 dB. The resistive averaging technique in a sub-sampling situation is more important than the Nyquist type, so it needs deep consideration.

The essential of the resistive averaging technique is a spatial filter[13]. Figure 7 indicates the resistive averaging technique.

The resistor network in the upper part is modeled as a linear system or spatial filter. The lower part is viewed as an active stimulus, which is the source of the signal and offset. The spatial impulse response can be described as

$$h(n) = b^{-|n|}, \quad b = \exp(-|a\cosh(1 + R_1/2R_0)|) < 1. \tag{7}$$

Moreover, for a differential pair, the available input signal range guaranteeing linear transconductance is defined as the width of a rectangular signal window (W_{ZX}).

$$W_{ZX} = \frac{2\sqrt{2}V_{ov}}{LSB}, \tag{8}$$

where V_{ov} is the overdrive voltage of the MOS transistor. LSB is the least significant bit.

To the noise, it also has the width of the rectangular noise window (W_n). From Ref. [13], the error correction factor (ECF) is defined to give an optimum solution to design the spatial filter,

$$ECF \equiv \frac{\sigma(os)}{\sigma'(os)} = \frac{g'_m/g_m}{\sigma'(i_{os})/\sigma(i_{os})}. \tag{9}$$

σ and σ' are the equivalent input offset without and with resistive averaging, respectively. g_m and g'_m are the transconductance of the preamplifier without and with resistive averaging, respectively. To the preamplifier at $n = 0$,

$$g'_m(0) = \sum_{-(W_{ZX}-1)/2}^{(W_{ZX}-1)/2} g_m(n)h(0-n) = g_m \sum_{-(W_{ZX}-1)/2}^{(W_{ZX}-1)/2} h(n). \tag{10}$$

After resistive averaging, the output offset current can be described as

$$i'_{os}(n) = \sum_{-(W_{ZX}-1)/2}^{(W_{ZX}-1)/2} i^2_{os}(n)h^2(0-n). \tag{11}$$

Assuming the output offset current of the preamplifier is the same, then

$$\frac{\sigma(i'_{os})}{\sigma'(i_{os})} = \sqrt{\sum_{-(W_{ZX}-1)/2}^{(W_{ZX}-1)/2} h^2(n)}. \tag{12}$$

From the above, we can get the ECF formula to differential nonlinearity (DNL) and integral nonlinearity (INL),

$$ECF_{DNL} = \frac{\sum_{-(W_{ZX}-1)/2}^{(W_{ZX}-1)/2} b^{|n|}}{\sqrt{\sum_{-(W_{ZX}-1)/2}^{(W_{ZX}-1)/2} b^{2|n-1|}(1-b)^2}}$$

$$= \frac{(1 + b(1 - 2b^{(W_{ZX}-1)/2}))/(1-b)}{\sqrt{b^{W_n-1} + (1-b)^2(1-b^{W_n-1})/(1-b^2)}}, \tag{13}$$

$$ECF_{INL} = \frac{\sum_{-(W_{ZX}-1)/2}^{(W_{ZX}-1)/2} b^{|n|}}{\sqrt{\sum_{-(W_{ZX}-1)/2}^{(W_{ZX}-1)/2} b^{2|n|}}}$$

$$= \frac{(1 + b(1 - 2b^{(W_{ZX}-1)/2}))/(1-b)}{\sqrt{(1 + b^2(1 - 2b^{W_n-1}))/(1-b^2)}}. \tag{14}$$

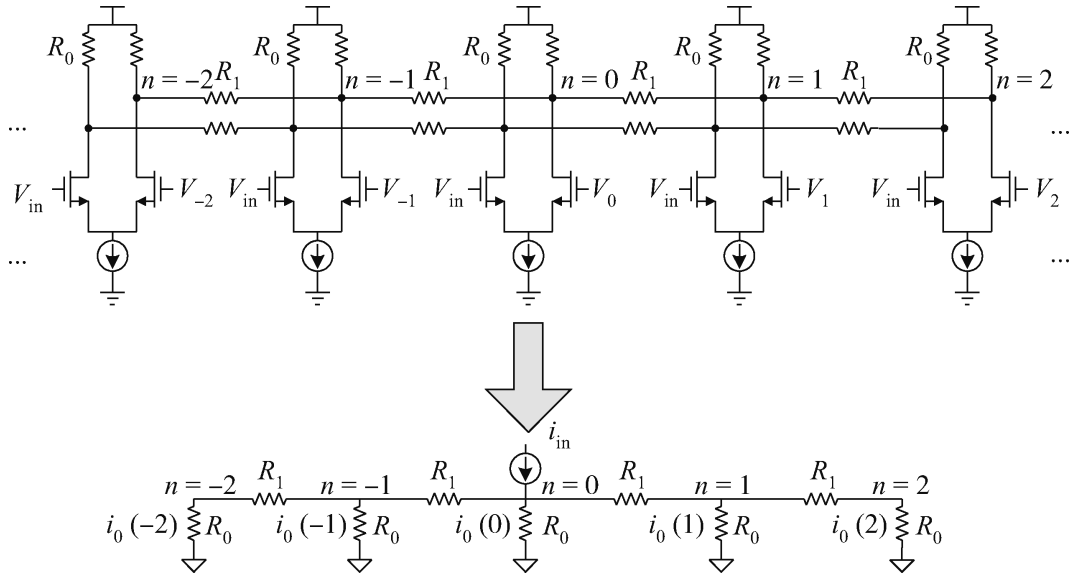


Fig. 7. Resistive averaging technique in flash ADC.

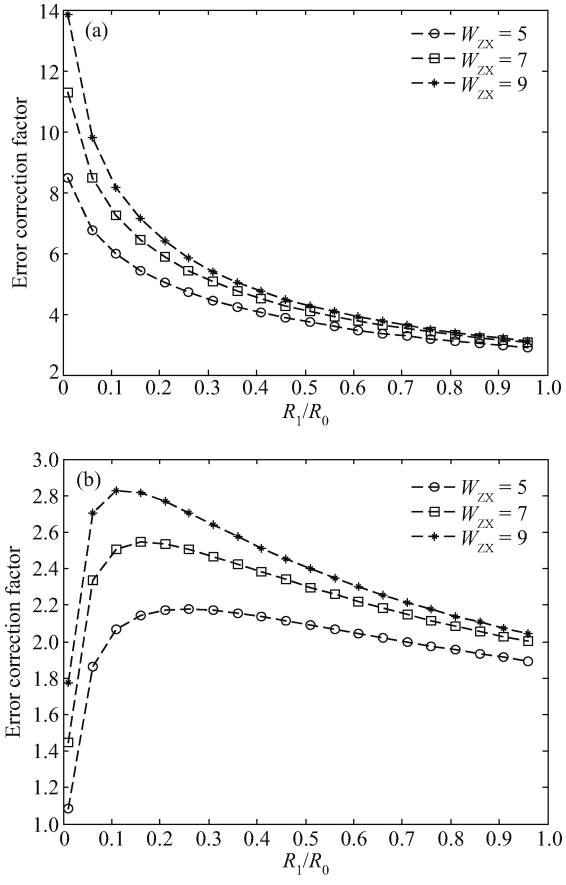


Fig. 8. Optimization of spatial filter. (a) ECF for DNL. (b) ECF for INL.

For the reason of noise aliasing, W_b can be regarded as infinite. b satisfies the exponent decay. The optimum scheme is obtained from Fig. 8.

Aiming at different widths of rectangular signal window, the proportion of R_1 and R_0 is given to realize an optimum solution. It is obvious that the resistive averaging technique is more effective to DNL than INL.

The discussion above just solves the problem of medial preamplifiers' random noise. The random noise of boundary preamplifiers will be excessively large. So we add two dummy ones at the boundary, as in Fig. 6.

3.3. Comparator with zero-static power dynamic offset cancellation technique

Seldom in the ultra-high speed situations is the real-time calibration used because of limited clock period. However, in the sub-sampling occasion, we have to adopt real-time calibration to overcome noise aliasing. A novel comparator in Ref. [14] achieves low-offset voltage without a pre-amplifier and quiescent current in Fig. 9. Furthermore, the overdrive voltage of the input MOS transistor can be optimized to lower offset owing to its independence of input common voltage and threshold voltage. The three stack of transistors in Fig. 9 largely reduces the voltage headroom compared with a traditional latch comparator. This structure can work in low-voltage deep-submicron CMOS technology. Figure 10 gives the timing scheme for the proposed comparator in Ref. [14].

In region 1, ϕ_1 turns on, the threshold of the input transistor M1 and M2 store in the C_{c-} and C_{c+}, respectively,

$$V_{os1} \approx V_{cmi} - V_{th1} - V_b, \quad V_{os2} \approx V_{cmi} - V_{th2} - V_b, \quad (15)$$

where V_{os1} and V_{os2} are the voltage of capacitors C_{c-} and C_{c+}, respectively. V_{cmi} is the common voltage of the comparator. is the threshold voltage of the input transistor. In region 2, the input signal is fed into the comparator. Region 3 is the comparison stage, in which the offset is canceled.

$$V_{od1} = V_{gs1} - V_{th1} = V_{cmi} + \Delta V_{in} - V_{os1} - V_{th1} = \Delta V_{in} + V_b, \quad (16)$$

$$V_{od2} = V_{gs2} - V_{th2} = V_{cmi} - \Delta V_{in} - V_{os1} - V_{th1} = -\Delta V_{in} + V_b. \quad (17)$$

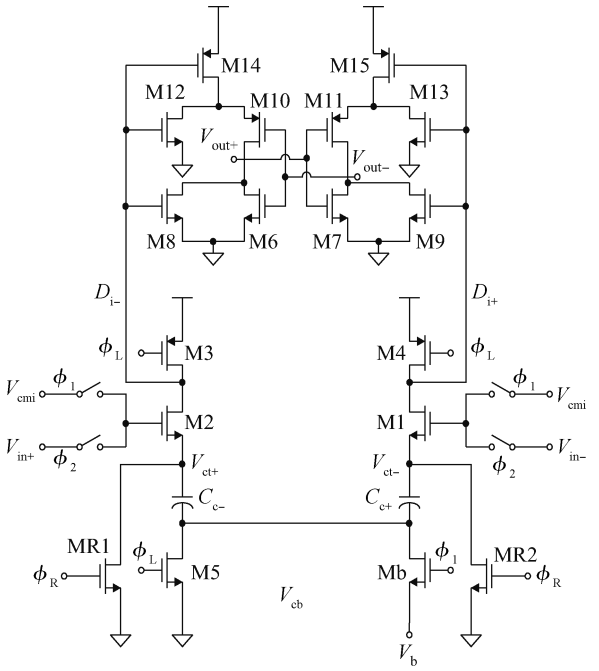


Fig. 9. Comparator with dynamic offset cancellation.

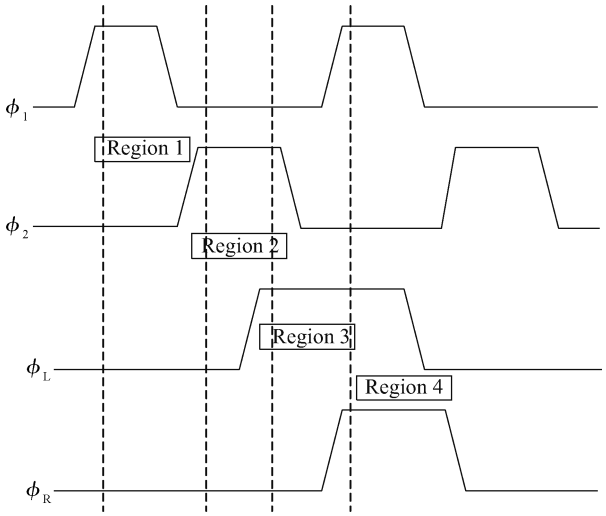


Fig. 10. Timing scheme of comparator.

V_{od} is the overdrive voltage of transistor. ΔV_{in} is the input signal. The mismatch of threshold voltage is cancelled because the overdrive voltage of the transistor does not depend on the threshold voltage of transistor. What's more, the overdrive voltage of the transistor isn't affected by the input common voltage. The last state is the reset stage in region 4, in which the offset canceling capacitors and C_{c-} are C_{c+} reset.

Using the structure can reduce the offset below 4 mV. However, the most serious drawback of the comparator in Ref. [14] is complex clock timing, which is sensitive to process, voltage and temperature (PVT) variation, especially in ultra-high speed ADCs whose available clock period is very limited. Surely we can use a pre-amplifier plus OOS (output offset storage) scheme, but the power consumption will increase largely due to the sub-sampling application. This is why in an ultra-high speed ADC, not to mention a sub-sampling application, the offset consideration is often relieved through larger LSB. The offset of the latch is about tens mV and noise aliasing further amplifies the random noise. The LSB of the ADC in this work is 12.5 mV because of the input signal limited in the UWB receiver. So we must pay attention to the offset that arises from the latch. At last, the novel comparator in Ref. [14] is still used in this work for the reason of compromise in power consideration and offset restraint, but the available clock period is only a quarter of their counterparts. The complex clock timing is realized through careful design of the inverter delay. The fixed phase relationship between clocks is based on the unit delay of an inverter, which limits the comparator to only work at the sample rate of 1.056 GHz. The dimension of the transistor is optimized to abide further clock skew through all process corners.

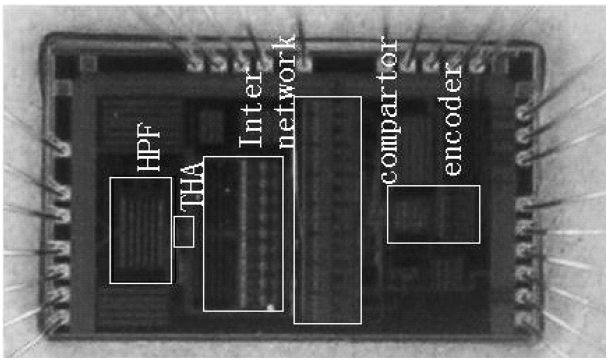


Fig. 11. Die microphotograph.

4. Experimental results

The proposed ADC is manufactured in a SMIC 0.13 μm CMOS process. The total area is 2.4 mm^2 including pads. The microphotograph of the die is depicted in Fig. 11. To reduce the supply noise and the off-chip printed circuit board (PCB) noise, large on-chip bypass capacitors realized with MOS transistors and MIM capacitors are included wherever space allows.

Due to the limitations of the test environment, the output digital data are further sub-sampled at 70.4 MS/s by a logic analyzer. Just as the discussion in part 2, the phase noise power is amplified by m^2 due to the sub-sampling technique. Sub-sampling from Off-chip introduces more phase noise than we expected, which influences the high frequency performance. Figure 12 gives the performance of the input signal at different frequencies at a sample rate of 1.056 GS/s. SFDR remain about 30 dB until a 4.28 GHz input signal, then drops to 28.7 dB at a 4.3 GHz input signal. The signal to noise and distortion rate (SNDR) exceeds 18 dB until a 4.25 GHz input signal, then decreases to 16.8 dB at a 4.3 GHz input signal. The balun we used to generate the differential input signal is a band pass component, which limits the test from a low frequency input signal. Figure 13 shows the fast Fourier transform (FFT) spectrum when the input signal is 4.2 GHz sampled at 1.056 GS/s. The resultant SFDR and SNDR are 30.1 dB and 18.75 dB, respectively. Figure 14 shows the DNL and INL performance sampled at 1.056 GHz. They lie in the range of –0.32 to 0.6 LSB and –0.52 to 0.66 LSB, respectively. The total power of the ADC excluding all consumption in the buffers is 30 mW.

Table 2. Performance summary and comparison.

Ref.	Ref. [15]	Ref. [16]	Ref. [17]	Ref. [11]	Ref. [6]	This work
Process (μm)	0.18 CMOS	0.13 CMOS	0.18 CMOS	0.13 CMOS	0.18 CMOS	0.13 CMOS
Sample rate (GS/s)	1.35	1	4	2	1	1.056
ERBW (GHz)	0.65	0.5	1	< 1	5.8	4.2
SFDR (dB)	32	—	19	—	—	30.1
DNL/INL	< 0.48/0.44	1.1/1.1	—	—	0.25/0.17	0.6/0.66
Power (mW)	68	112	34m	124	10.6	30
FoM (pJ/conv.-step)	5.3	3.5	4.8	9.8	0.8	3.75

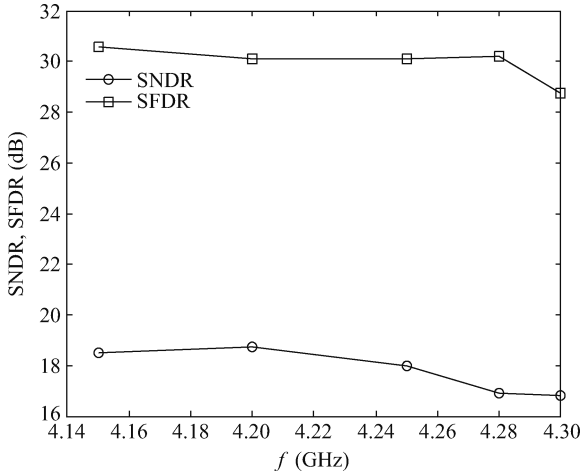


Fig. 12. Performance of ADC in different input signals.

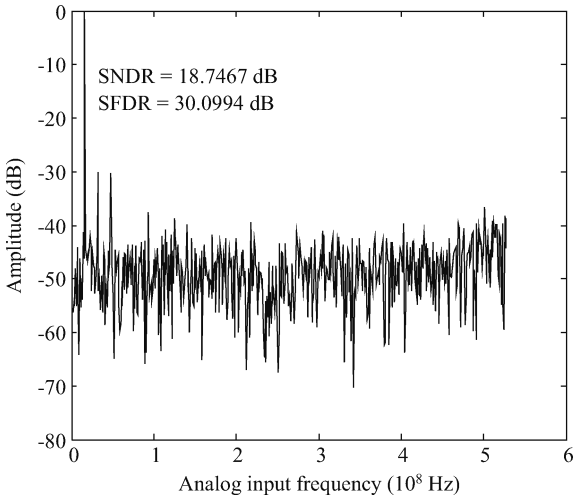
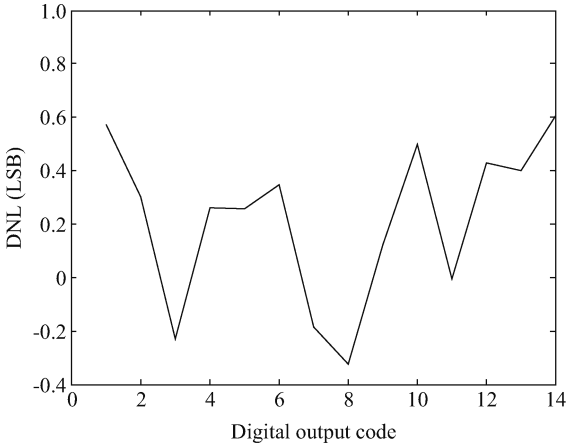


Fig. 13. FFT spectrum of a 4.2 GHz input signal sampled at 1.056 GS/s.

We define the figure of merit (FoM) as

$$\text{FoM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \min(\text{fclk}, 2\text{BW})}. \tag{18}$$

Table 2 gives a comparison between this work and recently published work, which reveals that the performance of the proposed ADC shows some advantages in both power consumption and ERBW.



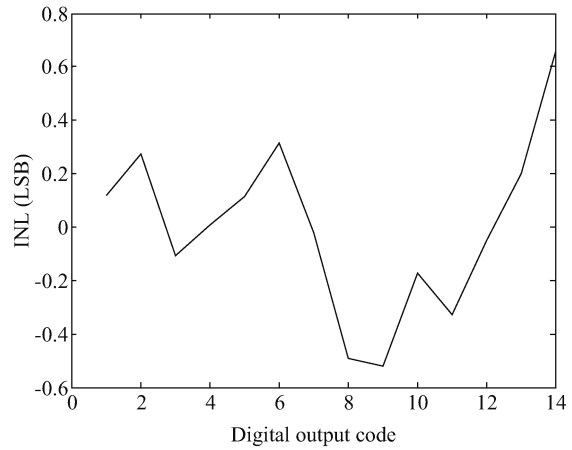


Fig. 14. Plot of DNL and INL.

5. Conclusion

An ultra-high speed, low resolution 0.13 μm CMOS ADC based on sub-sampling flash architecture for an IR-UWB receiver has been presented. The challenge in the sub-sampling structure is carefully discussed and given considerable attention. In the circuit implementation, the THA with a self-biased buffer is proposed to enhance linearity and power-efficiency and comparator with a dynamic offset cancellation technique that was optimized to decrease the power consumption and offset. The measured performance indicates that the optimization strategies are efficient in the sub-sampling structure. The proposed sub-sampling ADC fulfils 30.1 dB SFDR at an input signal of 4.2 GHz, making it suitable for an IR-UWB receiver.

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