A new high voltage SOI LDMOS with triple RESURF structure*

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Abstract: A novel triple RESURF (T-resurf) SOI LDMOS structure is proposed. This structure has a P-type buried layer. Firstly, the depletion layer can extend on both sides of the P-buried layer, serving as a triple RESURF and leading to a high drift doping and a low on-resistance. Secondly, at a high doping concentration of the drift region, the P-layer can reduce high bulk electric field in the drift region and enhance the vertical electric field at the drain side, which results in uniform bulk electric field distributions and an enhanced BV. The proposed structure is used in SOI devices for the first time. The T-resurf SOI LDMOS with BV = 315 V is obtained by simulation on a 6 μm-thick SOI layer over a 2 μm-thick buried oxide layer, and its R_{sp} is reduced from 16.5 to 13.8 m$\Omega\cdot$cm^2 in comparison with the double RESURF (D-resurf) SOI LDMOS. When the thickness of the SOI layer increases, T-resurf SOI LDMOS displays a more obvious effect on the enhancement of BV^2/R_{on}. It reduces R_{sp} by 25% in 400 V SOI LDMOS and by 38% in 550 V SOI LDMOS compared with the D-resurf structure.

Key words: SOI LDMOS; double resurf; triple resurf; REBULF; breakdown voltage
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1. Introduction

RESURF technology has been widely used in order to obtain a high breakdown voltage and low on-resistance in a lateral double-diffused metal–oxide–semiconductor field-effect-transistor (LDMOSFET). D-resurf and T-resurf structures have been realized in the bulk silicon LDMOS to reduce on-resistance[1−5]. However, the T-resurf structure has not been reported to be applied to SOI LDMOS before and the optimization of P-buried layer has not been discussed yet. The P-layer can reduce bulk electric field in a high doping concentration in the drift region and enhance the vertical electric field at the drain side, which results in uniform bulk electric field distributions and an enhanced BV. The P-type buried layer can be easily implemented by using ion implantation without an extra process compared with the D-resurf structure.

2. Structure and mechanism

The cross section of a T-resurf SOI LDMOS is shown in Fig. 1. t_s and N_d are the thickness and doping concentration of the SOI layer. t_p, L_p and N_p are the thickness, length and doping concentration of the P-buried layer, respectively. t_M represents the distance from the top of the P-buried layer to the surface. The field plate here is used to avoid premature breakdown.

Figure 2 shows the electric field and potential distributions of D-resurf and T-resurf SOI LDMOSFETs. BV represents the breakdown voltage and R_{sp} represents the specific on-resistance. Figure 2(a) indicates that the vertical location (i.e. t_M) of the P-layer has great influence on the bulk electric field distributions. At the optimal doping concentration N_d = 7×15 cm^{-3} for a T-resurf SOI LDMOS with $t_M = 1.5$ μm, D-resurf has a high electric field peak E_0 in the interface of the P-top and N-drift region. However, T-resurf ($t_M = 1.5$ μm) has two lower electric field peaks E_1 and E_2, which results in a reduced bulk electric field and the electric field concentration effect disappears. This effect is similar to the effects of REBULF technology[6−8]. Moreover, the value of E_1 and E_2 is almost the same as the interface electric field E_{I12}, so a uniformly distributed bulk electric field is obtained in the SOI layer. This field distribution modulates the electric field at the drain side, leading to an enhanced average bulk field and thus an improved BV, as seen in Fig. 2(b). When $t_M = 3$ μm, the T-resurf structure has just one high electric field peak E_3. This shows that the electric field peak approaches the bottom of the SOI layer. Moreover, the interface electric field of T-resurf ($t_M = 3$ μm) is much lower than that of T-resurf ($t_M = 1.5$ μm) at the drain

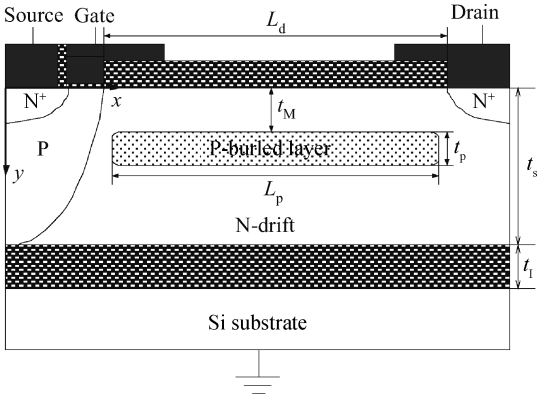

Fig. 1. Schematic cross sections of a T-resurf SOI LDMOS.

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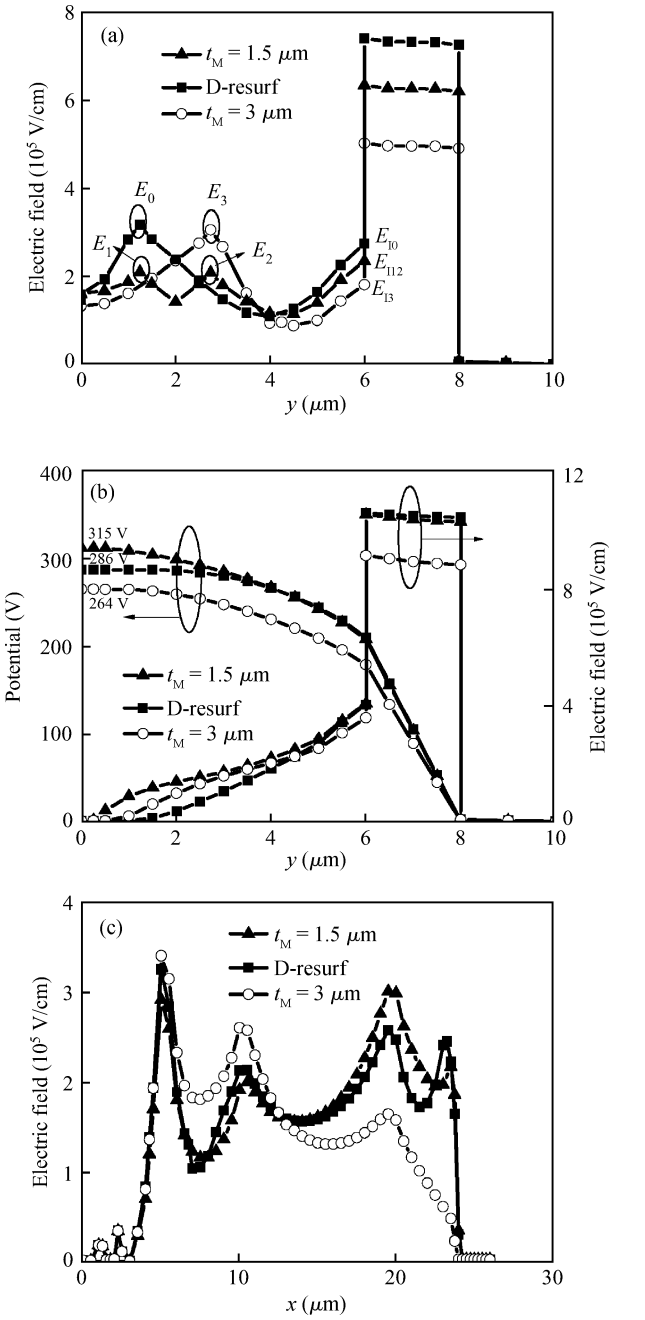

Fig. 2. Electric field and potential distributions of D-resurf and T-resurf structures ($t_s = 6\,\mu$m, $t_I = 2\,\mu$m, $L_d = 20\,\mu$m, $L_p = 17\,\mu$m, $t_p = 1\,\mu$m). (a) Vertical electric field along $x = 15\,\mu$m ($L_d/2$) in SOI layer. (b) Electric field and potential distributions at the drain. (c) Electric field distributions in the x-direction at the surface.

side, so the BV is decreased. The surface electric field is shown in Fig. 2(c). The vertical location of the P-layer has an obvious modulation effect on the surface field. T-resurf with $t_M = 1.5\,\mu$m has the lowest electric field at the source side and highest electric field at the drain side. The doping concentration of the drift region can be therefore the highest.

Figure 3 shows the off-state and on-state characteristics of D-resurf and T-resurf SOI LDMOSFETs. In Fig. 3(a), R_{sp} of T-resurf with $t_M = 1.5\,\mu$m decreases to 13.8 mΩ·cm^2 from 16.5 mΩ·cm^2 of D-resurf LDMOS with the same BV = 315 V; or the BV of T-resurf increases from 286 V of D-resurf

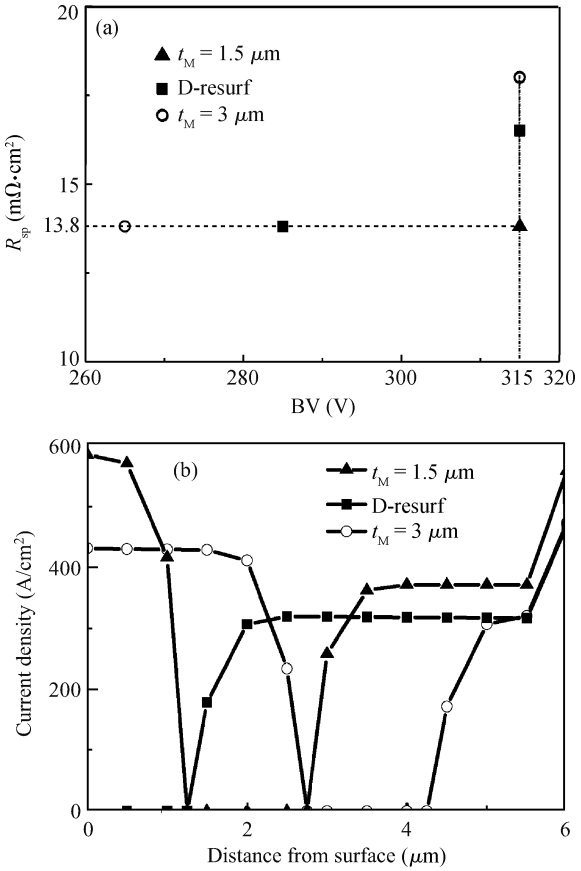

Fig. 3. Off-state state and on-state characteristics comparison of D-resurf and T-resurf SOI LDMOS. (a) Comparison of specific on-resistance versus breakdown voltage of D-resurf and T-resurf SOI LDMOS ($t_s = 6\,\mu$m, $t_I = 2\,\mu$m, $L_d = 20\,\mu$m, $L_p = 17\,\mu$m, $t_p = 1\,\mu$m). (b) On-state vertical current density along $x = L_d/2$ in SOI layer ($V_G = 15$ V and $V_D = 1$ V, the BV = 315 V).

structure to 315 V when two devices have the same $R_{sp} = 13.8$ mΩ·cm^2. The current density in the vertical direction at the on-state is given in Fig. 3(b). T-resurf with $t_M = 1.5\,\mu$m has the largest current density above and below the P-layer compared with the other two structures.

3. Results and discussion

The parameters of P-buried layer are optimized with the 2-D simulator MEDICI. It can be observed from Fig. 4(a) that the T-resurf structure with $t_M = 1.5\,\mu$m has the highest N_d of 7×15 cm^{-3} at the maximal BV, which results in a 16% decrease in R_{sp} compared with optimized $N_d = 5.6 \times 15$ cm^{-3} of the D-resurf structure. Figure 4(b) shows the dependence of BV and R_{sp} on different t_M. The best T-resurf optimal area is $1\,\mu\text{m} < t_M < 1.5\,\mu$m.

Figure 5 shows the dependence of BV and R_{sp} on L_p. Theoretically, N_p should be increased to maintain the charge balance when the value of L_p is low. However, according to the SOI RESURF condition (the D-resurf model is used to approximate the T-resurf structure herein)[9], N_p should not be too high in order to fully deplete, which causes a decreased in N_d as shown Fig. 5(a). Hence, a narrower P-buried layer has a smaller optimized N_d to maintain the BV of 315 V and the R_{sp}

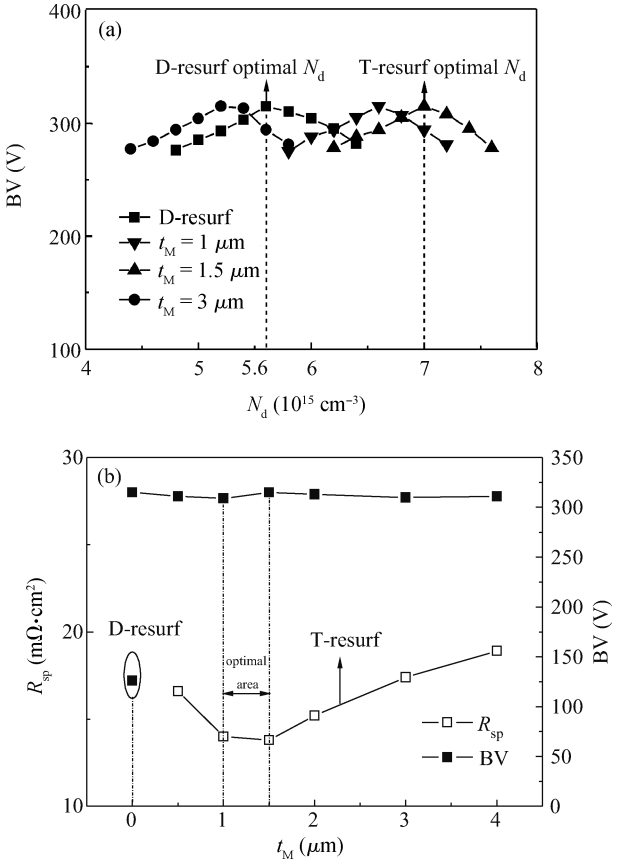

Fig. 4. Influence of t_M on BV and R_{sp} ($t_s = 6\,\mu$m, $t_I = 2\,\mu$m, $L_d = 20\,\mu$m, $t_p = 1\,\mu$m, $L_p = 17\,\mu$m). (a) Sensitivity of BV and R_{sp} with N_d for different t_M. (b) Dependence of BV and R_{sp} on different t_M. The best T-resurf optimal area is obtained here.

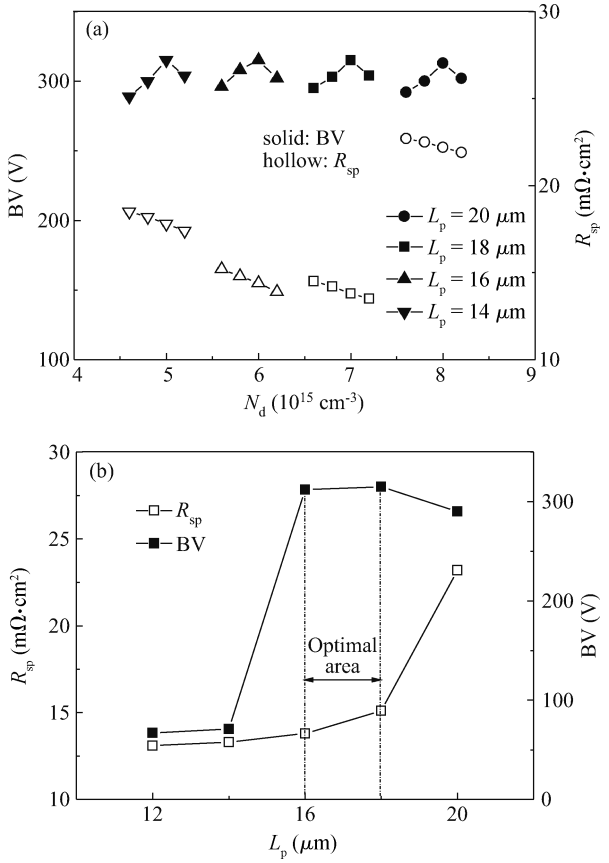

Fig. 5. Dependence of BV and R_{sp} on L_p (the middle of the P layer is at $x = 15\,\mu$m which is also the middle of the drift region. $t_p = 1\,\mu$m, $t_M = 1.5\,\mu$m). (a) Sensitivity of BV and R_{sp} with N_d for different L_p. (b) Dependence of BV and R_{sp} on L_p at the same $N_d = 7 \times 10^{16}$ cm^{-3}. The best T-resurf optimal area is obtained here.

is increased. But when $L_p > 18\,\mu$m, the R_{sp} increases dramatically because the JFET resistance near the source becomes the main element of R_{sp}[10]. Figure 5(b) indicates the influence of L_p. When 16 μm < L_p < 18 μm, the optimal T-resurf area is obtained.

In general, T-resurf with optimal t_M can reduce the bulk electric field in a high drift region doping and enhance electric field at the drain side, which results in a uniform bulk electric field distributions and a high FOM of BV^2/R_{on}. This also applies to the SOI LDMOS with $t_s > 6\,\mu$m. The vertical electric field distributions at the drain side are compared in Fig. 6 at $t_s = 6$, 10 and 20 μm. When t_s increases, the SOI layer sustains more proportion of the BV and the modulation effect of P-layer is more apparent. T-resurf with $t_s = 20\,\mu$m has the same critical electric field as D-resurf structure but the BV is increased by 118 V due to the enhanced bulk electric field, while T-resurf with $t_s = 10\,\mu$m and $t_s = 6\,\mu$m is increased by 68 V and 29 V, respectively. Figure 7 shows the phenomenon. At the same BV for the D-resurf and T-resurf structures, T-resurf has higher N_d and N_p as seen in Fig. 7(a). T-resurf also has higher $(N_{d,T} - N_{d,D})/N_{d,D}$ for a larger t_s value. Figure 7(b) shows the dependence of BV and R_{sp} on t_s. T-resurf structure reduces R_{sp} by 25% in 400 V SOI LDMOS and reduces R_{sp} by 38% in 550 V SOI LDMOS, compared with D-resurf structure.

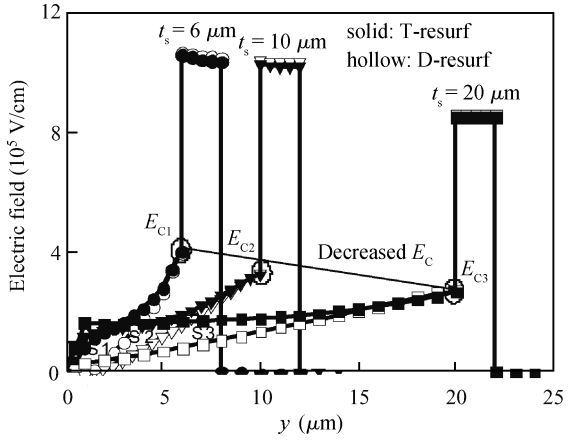

Fig. 6. Comparison of D-resurf and T-resurf electric field at the drain side when $t_s = 6$, 10 and 20 μm ($t_I = 2\,\mu$m, $t_p = 1\,\mu$m). The doping concentration of drift region is $N_d = 7 \times 15$ cm^{-3} for $t_s = 6\,\mu$m, $N_d = 3.4 \times 15$ cm^{-3} for $t_s = 10\,\mu$m, $N_d = 1.2 \times 15$ cm^{-3} for $t_s = 20\,\mu$m (each N_d is T-resurf optimal doping concentration) and the lateral dimension is designed to meet the vertical breakdown conditions.

4. Conclusion

A novel T-resurf SOI LDMOS structure has been proposed. This structure has been reported in SOI LDMOS and

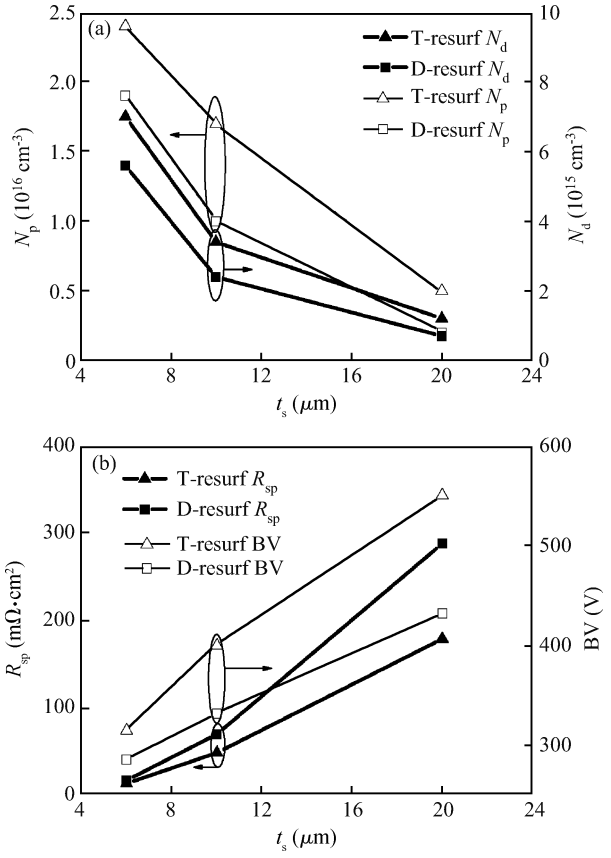

Fig. 7. Comparison of R_{sp}, BV and N_d, N_p versus t_s of D-resurf and T-resurf SOI LDMOS for $t_s = 6$, 10 and 20 μm ($t_I = 2$ μm, $t_p = 1$ μm). (a) Dependence of N_d and N_p on t_s. (b) Dependence of BV and R_{sp} on t_s. The lateral dimension is designed to meet the vertical breakdown conditions.

the optimization of P-buried layer has been investigated for the first time. The buried P-layer can reduce bulk electric field in drift region in a high doping concentration and enhance electric field at the drain side, which results in a uniform bulk electric field distributions and an enhanced BV. The T-resurf structure provides the on-resistance reduction of 16%, 25% and 38% compared with D-resurf structure in 315 V, 400 V and 550 V SOI LDMOS, respectively.

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