Design of a high performance CMOS charge pump for phase-locked loop synthesizers*

Li Zhiqun(李智群)[1, 2, †], Zheng Shuangshuang(郑爽爽)[1, 2, 3], and Hou Ningbing(侯凝冰)[1, 2]

[1]Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China
[2]RFIC and System Engineering Research Center of the Ministry of Education of China, Southeast University, Nanjing 210096, China
[3]School of Integrated Circuits, Southeast University, Nanjing 210096, China

Abstract: A new high performance charge pump circuit is designed and realized in 0.18 μm CMOS process. A wide input ranged rail-to-rail operational amplifier and self-biasing cascode current mirror are used to enable the charge pump current to be well matched in a wide output voltage range. Furthermore, a method of adding a precharging current source is proposed to increase the initial charge current, which will speed up the settling time of CPPLLs. Test results show that the current mismatching can be less than 0.4% in the output voltage range of 0.4 to 1.7 V, with a charge pump current of 100 μA and a precharging current of 70 μA. The average power consumption of the charge pump in the locked condition is around 0.9 mW under a 1.8 V supply voltage.

Key words: charge pump; current mismatch; rail-to-rail operational amplifier; phase-locked loop
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1. Introduction

Charge-pump phase-locked-loops (CPPLLs) are widely used in modern wireless communication systems, due to advantages such as their larger system gain, faster frequency detecting reactions, larger range acquisition and a perfect zero static phase error. In a typical CPPLL system, a phase frequency detector (PFD) is used to generate a phase difference between two input signals. Then it outputs a logical signal to control the charging or discharging current of the charge pump (CP). The output current of the CP is transformed into a voltage controlling the voltage controlled oscillator (VCO) through a loop filter (LF). An ideal CPPLL model has a perfect zero input phase error, but taking the mismatch into account, certain phase error is introduced in practical circuits. That means the matching precision of CP is directly related to the phase error of the whole PLL system. In addition, the setting time of CPPLLs is related to the precharging current[1, 2]. Much research has been done to improve CP performance. The CP structure[3] achieves high current matching precision by using an operational amplifier, but has the limitation of a low precharging current. An adaptive architecture[1] based on two complicated tuning loops achieves a fast settling time but adds difficulties to the design and consumes more power.

Compared with traditional CP structures, the CP proposed in this paper achieves higher current matching precision in a wide output voltage range and has higher precharging current. This CP is designed and fabricated in 0.18 μm CMOS process.

2. Design of charge pump circuit

A block diagram of a CPPLL synthesizer system is illustrated in Fig. 1. There are five main blocks in this diagram: PFD, CP, LF, VCO and frequency divider. Among them, the CP consists of two switched current sources that pump charge into or out of the LF according to the output signal from the PFD. I_1 is a charging current or a UP current whereas I_2 is identified as a discharging current or a DOWN (DW) current, they are nominally equal[1].
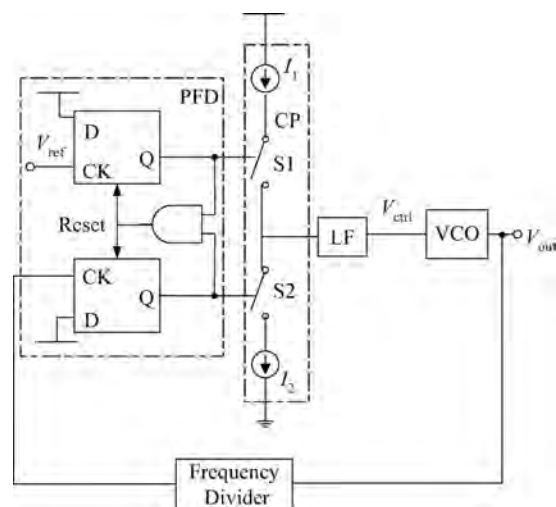
PFD/CP has three working states, listed in Table 1.

Fig. 1. Typical CPPLL synthesizer system.

Table 1. Three states of PFD/CP.

STATE	S1	S2	Vctrl
UP	On	Off	Rise/Charge
HOLD	Off	Off	Hold /Lock
DW	Off	On	Fall/Discharge

2.1. Non-ideal effects in CMOS charge pump

In practical circuits, the non-ideal behavior of MOS switches and other components bring about charge injection and clock feedthrough. Those errors cause periodic ripples on the control line, which introduce phase noise and spurious tones in the VCO output. The total phase error $\Delta\Phi_{\text{tot}}$ caused by these non-idealities can be approximated as[3−5]:

$$\Delta\Phi_{\text{tot}} = 2\pi(\Delta\Phi_{\text{leakage}} + \Delta\Phi_{\text{mismatch}} + \Delta\Phi_{\text{timing}})$$
$$= 2\pi\left(\frac{I_{\text{leakage}}}{I_{\text{cp}}} + \frac{\Delta i}{I_{\text{cp}}}\frac{t_{\text{on}}}{T_{\text{ref}}} + \frac{\Delta t_{\text{delay}} \times t_{\text{on}}}{T_{\text{ref}}^2}\right), \quad (1)$$

where I_{cp} is the rating current of CPs, I_{leakage} is the leakage current, T_{ref} is the reference cycle time, t_{on} is the turn-on time of the PFD and Δi and Δt_{delay} refer to the mismatching of current and timing respectively.

First of all, the leakage current effect can be ignored because the average level of I_{leakage} is at a magnitude of pA[3], compared with the CP current 100 μA in this design. T_{ref} is related to the system parameter, which is fixed once the whole system is designed. In addition, t_{on} should be minimized under the condition of ensuring that the CP is switched on and avoiding the dead-zone in the PFD/CP. Δt_{delay} can be lowered by decreasing the connection delay between the logical output of PFD and the CP switches. The symmetry of the layout affects Δt_{delay}. Therefore, minimizing Δi should be taken into more consideration for reducing the phase error $\Delta\Phi_{\text{tot}}$.

The resulting reference spurs for a third-order PLL can be approximated as[4]

$$P_{\text{r}} = 20\lg\frac{Nf_{\text{bw}}\Delta\Phi}{\sqrt{2}f_{\text{ref}}} - 20\lg\frac{f_{\text{ref}}}{f_{\text{p1}}}, \quad (2)$$

where N is the division ratio of the divider, f_{bw} is the loop bandwidth and f_{pl} is the frequency of the pole in the loop-filter. Equation (2) shows that the spurs can be reduced by lowering the loop phase error $\Delta\Phi$, decreasing the loop bandwidth f_{bw} or increasing the reference frequency f_{ref}. In this design, $\Delta\Phi$ is the main factor to be dealt with.

From the analysis above, the conclusion can be drawn that Δi is directly related to the phase error and the reference spurs of the whole PLL system. Minimizing Δi will introduce better PLL performance. Therefore, finding how to reduce the mismatch of current Δi is the key target of CP design.

2.2. Consideration of charge pump design

Current mismatching refers to the magnitude difference of charging and discharging currents. There are three main factors causing these mismatches.

(1) Asymmetry of the current sources of the charging and discharging LF;

(2) Current source mismatches caused by different output voltages;

(3) Current pulses occurring randomly once the UP/DW switches are turned on.

The first two factors can be reduced by applying one common current source for the UP/DW current. To further study the error introduced by non-ideal MOS switches, more considerations should be discussed: charge injection and clock feedthrough[2].
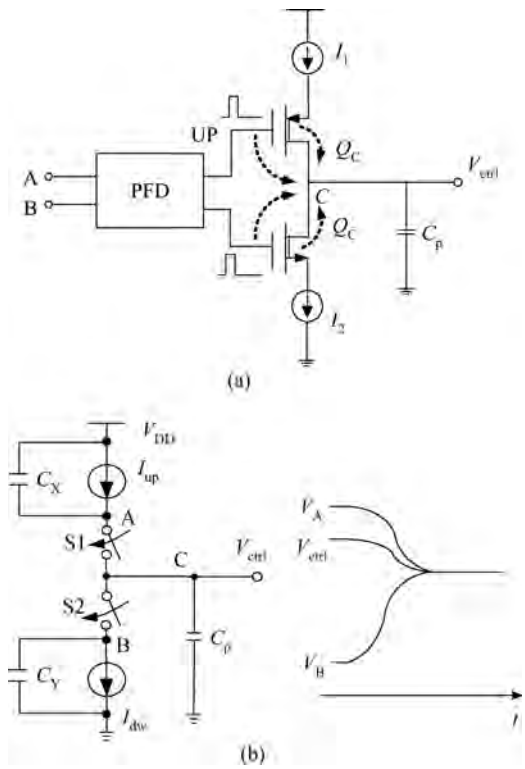

Fig. 2. Mismatching in the CP. (a) Error caused by charge injection and clock feedthrough. (b) Charge sharing between C_{p} and capacitances C_{X} and C_{Y}.

Charge injection is a phenomenon that arises due to the leakage of charge into a capacitive node during the turn off of a switch that is connected to that node[6]. As illustrated in Fig. 2(a), here we are only concerned with the capacitive node C with load capacitance C_{P}, with two MOS switches connected. When the switches turn off, the charge remaining in the channel will inject into C_{P} and cause a ripple on the output voltage (V_{ctrl}). Clock feedthrough means that the MOS switch couples the clock transitions to the load capacitor C_{p} through its gate–drain parasitic capacitor, depicted in Fig. 2(a).

Charge injection and clock feedthrough will add onto V_{ctrl} directly, causing the phase error to worsen. According to research, this interference is proportional to the value WLC_{OX}, where W and L are the width and length of the MOSFET, respectively. Therefore, a smaller sized MOS switch is recommended in order to reduce the effects of clock feedthrough and charge injection.

In addition to clock feedthrough and charge injection, charge sharing is another crucial problem that can lead to current mismatching. Charge sharing originates from the finite capacitance at the current sources. As revealed in Fig. 2(b), A and B represent the current source terminals of the charge pump, respectively, while C is the node of the load terminal. When the switches S1 and S2 are both off, neither the current source nor the current sink outputs the current, thus the voltage at the node A is charged to V_{DD}, whereas B is discharged to ground. As a result, the voltages of the terminals A, B and C are different. The switches are then turned on again, the charges on C_{p} are redistributed to the parasitic capacitances of the current source and current sink, leads to ripples on the output voltage of C_{P}
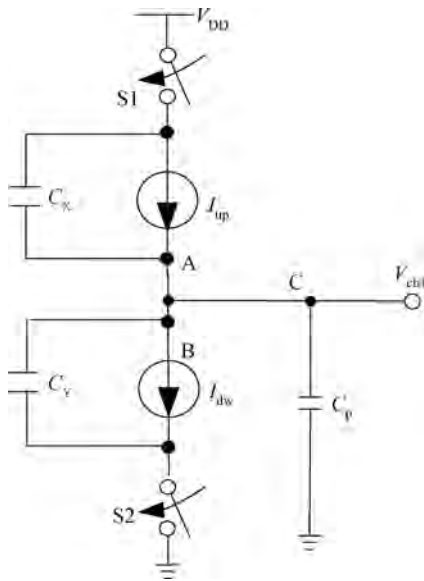
Fig. 3. Position of the switches in the proposed CP.

Fig. 4. Improved charge pump structure.

and directly causes serious jitters to the VCO.

In order to reduce the non-ideal effects, the position of switches should be carefully chosen[4]. In this design, we exchange the position of the switches and current sources. As shown in Fig. 3, current injection and clock feedthrough caused by switches will not directly influence the output voltage. In addition, the charge sharing phenomenon is also decreased since terminals A, B and C are at the same point. A conventional structure is to use a unit-gain operational amplifier to restrain charge sharing[7]. Moreover, an effective way to solve current mismatching is to apply the error operational amplifier to make currents I_{up} and I_{dw} match well and also offers the VCO a wide tuning scale[3].

2.3. Proposed charge pump

Based on the analysis above, an improved CP structure is shown in Fig. 4. Here, a rail-to-rail operational amplifier (A) is used to realize a good current matching within a large output voltage range.

In Fig. 4, M4 is a charge current switch of PMOS type positioned between V_{DD} and M5, whereas M12 is the discharge current switch of NMOS type positioned between ground and M10. This design of the switches will reduce the non-ideal effects discussed above. Furthermore, the switching speed is also accelerated since the switches are only connected to one transistor so there is less parasitic capacitance. A cascode current source is adopted for much steadier charge and discharge currents. This self-biasing cascode current mirror is composed of the resistor R and cascode devices M1–M2, M8–M10 and M9–M11. This current mirror ensures that the charge and discharge currents retain an exact value within a large range of control voltage V_{ctrl}. M6, M7, M9, M11 and M13 are used to form a replica circuit to guarantee that the charge current I_{up} and discharge current I_{dw} match well. The size of the transistors is: M6 = M4, M7 = M5, M9 = M8, M11 = M10 and M13 = M12.

With the cascode current mirror design, the current I_{dw}

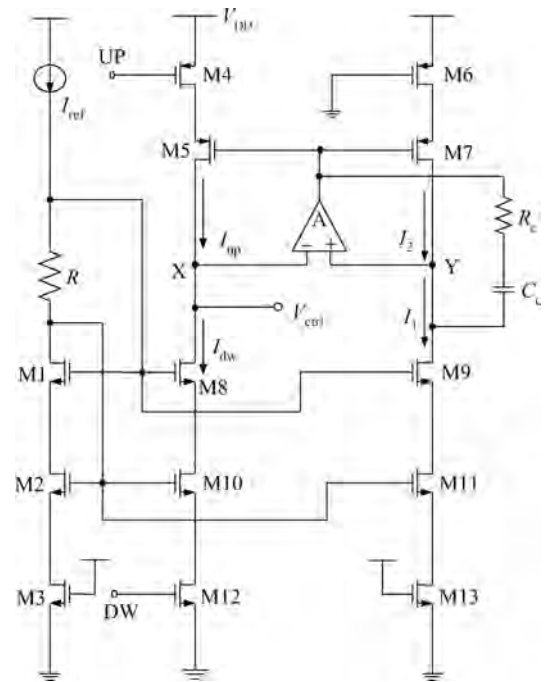equals to I_1, whereas I_1 is also equal to I_2 for the input current of the operational amplifier (A) is zero, so we can get $I_1 = I_2 = I_{dw}$. M5 is the charging current device. As shown in Fig.4, the gates of M5 and M7 are biased by the error amplifier. In addition, the voltages on the two points X and Y are directly adjusted to be same by the error amplifier, so that the current I_{up} is identical to the replica current I_2. With all these designs, the charge current I_{up} matches the discharge current I_{dw}. All the transistor gate lengths are designed to be large enough to avoid the effect caused by channel-length modulation.

As is known, the larger the range of V_{ctrl} offered to the VCO, the better the whole PLL system performs. In this case, a rail-to-rail operational amplifier is an ideal choice. The rail-to-rail operational amplifier shown in Fig. 5 is used in the proposed CP structure. The couples of input transistors are composed by a pair of NMOS devices and a pair of PMOS devices, so as to achieve a wider range of input voltage. The gain is assured to be high enough by using cascode output stage, for the operational amplifier's gain dominates the current matching precision of the CP.

In the proposed charge pump shown in Fig. 4, more attention should be paid to the connection of the operational amplifier, since it simultaneously brings a positive feedback loop and a negative feedback loop. Therefore stable analysis is required. In this design, Miller compensation of series connected C_c and R_c between the output and the error amplifier's positive port is used to keep the circuit stable.

Under a Cadence–Spectre RF simulation environment, the current matching characteristic simulation result of the CP shown in Fig. 4 is depicted in Fig. 6. From the simulation results, the charge and discharge currents are about 100 μA in the tuning voltage scale of 0.5 to 1.6 V. The current mismatch rate of the CP can remain within 0.01% in the span of 0 to 1.65 V. So the current mismatching problem has greatly improved.

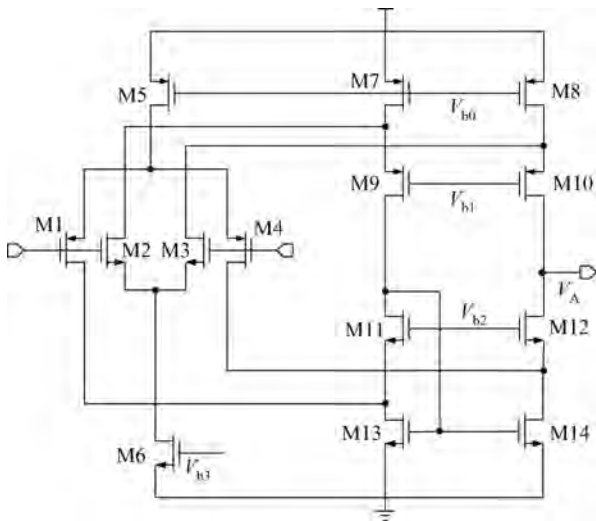However, the improved charge pump structure with a rail-

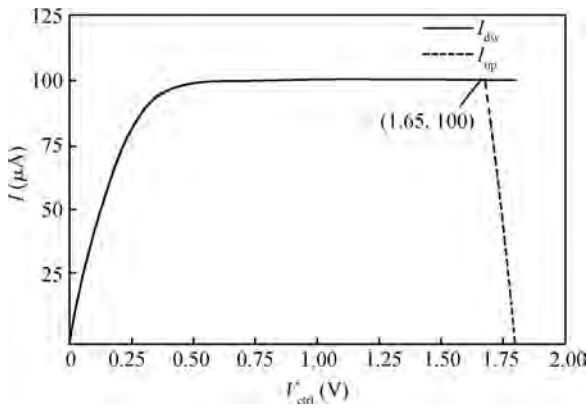Fig. 5. Rail-to-rail operational amplifier used in the CP.

Fig. 7. Proposed charge pump structure.

Fig. 6. Simulation result of the current matching characteristic of the improved CP.

Fig. 8. Simulation result of the current matching characteristic of the proposed CP.

to-rail operational amplifier will create an extra problem for CPPLLs. Considering the fast settling time performance of CP-PLLs, a large charge current at low V_{ctrl} is required. In other words, the larger the charge current at low V_{ctrl}, the faster the PLL locks. As shown in Fig. 6, when V_{ctrl} is near zero, I_{up} equals I_{dw} with a value near zero that will slow down the settling time of the PLL. A proposed CP structure to solve this problem is shown in Fig. 7.

In detail, M5 and M5′ in parallel make up the charging current devices, as do M7 and M7′ in the replica circuit. M14–M18 compose a biasing circuit for M5′ and M7′. The M16–M17 cascode devices are designed to provide a portion of the reference current I_{ref}. When V_{ctrl} is close to zero, M5′ provides the main initial charge current I_{up} whereas M5 contributes little because the operational amplifier (A) does not operate normally. The current matching characteristic of the proposed CP is shown in Fig. 8, which has the same high current matching precision as before. However, at the region of low output voltage, and different from Fig. 6, the charge current is about 65 μA, which guarantees a fast settling time performance of the CPPLLs.
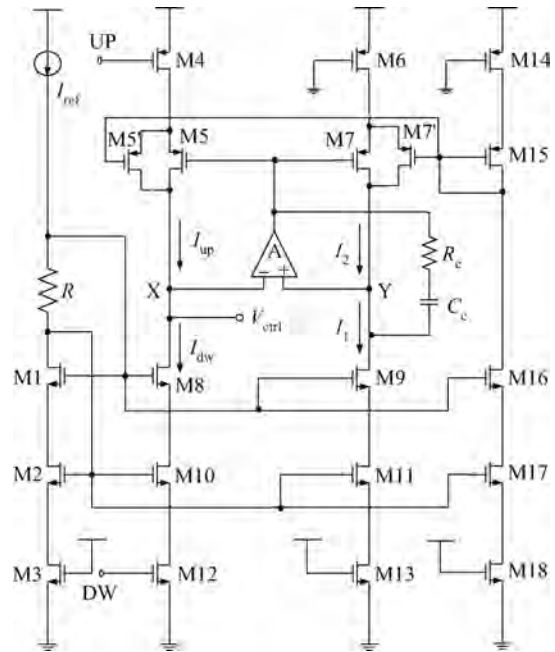
3. Layout design and test results

In the layout design of charge pumps, the symmetry of the current mirror is very important and directly affects the chip's performance. As a result, the common-centroid layout and additions of dummy devices are all used here to obtain better symmetry. The proposed CP has been fabricated in a 0.18 μm CMOS process by TSMC at the MPW Center, Institute of RF-& OE-ICs, Southeast University. A microphotograph of the chip is shown in Fig. 9. Its size is 0.2×0.18 mm^2. The current matching characteristic of the proposed CP has been tested on chip, as shown in Fig. 10. Comparing the test result with the simulation result shown in Fig. 8, we can draw the conclusion that the CP can keep the current mismatch within 0.4% in the output voltage range of 0.4 to 1.7 V. In addition, the charge and discharge currents are about 100 μA in the output voltage range of 0.5 to 1.6 V. The precharging current marked with a circle in the Fig. 10 is about 70 μA. The average power consumption of the CP in the locked condition, including the replica bias cir-
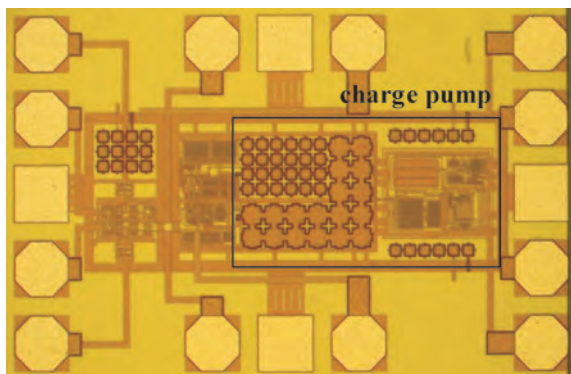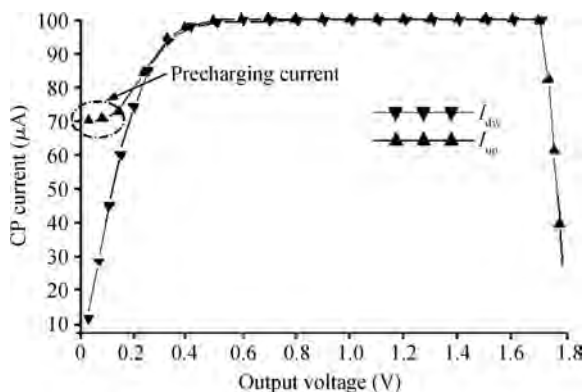
Fig. 9. Microphotograph of charge pump chip.

Fig. 10. Chip testing result of current matching characteristic of the proposed CP.

cuit and the rail-to-rail operational amplifier is around 0.9 mW under 1.8 V supply voltage. In other unlocked conditions, the average power consumption of the CP is less than 3.6 mW. All in all, for a charge pump current of 100 μA, the current mismatching of the proposed CP is much smaller and the power consumption is much lower than in the architectures reported in Refs. [3, 5].

4. Conclusion

This paper proposed a new structure of high performance CMOS charge pump for phase-locked loop synthesizer. According to the test results, with the help of cascode current mirror, rail-to-rail operational amplifier and the precharging current source, the proposed CP has a wide current match range, a high matching precision and a high pre-charging current. These performances will reduce the phase noise in a PLL significantly and speed up the settling time of a PLL. This CMOS charge pump structure can be applied in other CPPLLs with high performance.

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